



SMH4804 Power Down Sequencing

Preliminary

INTRODUCTION

It is often necessary to sequence the power down of DC-to-DC converters in a distributed power environment. Since the ON/OFF enable control for the DC-to-DC converters is found on the primary (–48V) power side of the converters, it would be very convenient to be able to implement power down sequencing as part of the hot swap solution.

One important power down sequence is the reverse order of the power up sequence, which is implemented in this Application Note. Of the several possible causes triggering the sequence, this Ap Note uses the Pin Detect (PD) signal. The signal could be generated via ejector switches on the card or from short pins on the backplane connector. The SMH4804 PD signals are active low. A very simple pin detect system can be implemented by shorting the pin detect inputs to –48V on the backplane. Alternatively, the detection could be made with reference to the secondary power ground and brought across the galvanic isolation to power sequence the supplies from the primary side.

Power down sequencing works by utilizing the Power Good Enable inputs (ENPGx). These signals are active high and have internal 50kΩ pull-up resistors. The ENPGx inputs are associated with Power Good outputs (PGx#) and are required to be active high in order to allow the sequencing of the PGx# outputs. ENPGA is associated with PG1# and it is required to be active in order for PG2#, PG3# and PG4# to be enabled. ENPGB is associated with PG2# and it is required to be active in order for PG3# and PG4# to be enabled. And ENPGC is associated with PG3# and it is required to be active in order for PG4# to be enabled.

APPLICATION CIRCUIT 1

Figure 1 illustrates an application circuit implementing power down sequencing for the SMH4804 hot swap controller. While the DC-to-DC converters are active, the PD input for the application circuit must be low (–48V). This turns off transistor Q6 and allows the ENPGx inputs to be enabled by their internal pull up resistors. As the card is removed from the backplane the short pin disengages first allowing transistor Q6 to discharge the ENPGx input nodes. The discharge will be governed by the RC time constant on each input: no RC for ENPGC, C5/R13 for ENPGB, C6/R14 for ENPGA, C7/R15 for Forced Shut-down (FS#).

The FS# input can control the power down of the PG1# output. The EN/TS input (200kΩ pull-up) could also be used, or the pin detect inputs (with some circuit modifications). Using the FS# input allows the power supplies to come up regardless of feedback from the secondary. If the pin detect signal is coming from the secondary side, power for the optocoupler is available to get the signal from the secondary to the primary side. If the signal is not active after a fixed time period the primary side will be shut down by the SMH4804.

The time constants for the power down sequencing should be made small enough so that it is complete before the card is completely disengaged from the backplane. If this is not done the DC-to-DC converters will not have turned off before the power connector disengages which might result in power connector arcing.

The time constants for charging C5, C6, and C7 through the internal pull-up resistors must be considered as well since the enable signals must be present when the SMH4804 sequences the supplies on power up. This is not a great concern since the power down delay is much quicker than the power up delay.



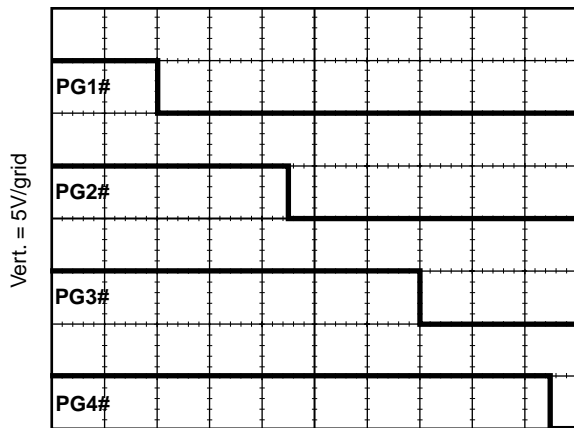
TIMING SEQUENCES

Figure 2 illustrates the power up sequence for the SMH4804 with a 5ms programmed delay between PGx# outputs. The outputs are active low.

Figures 3 and 4 illustrate the power down sequence with a 1ms delay between power good outputs. The passive values shown in the schematic (Figure 1) were used to generate this delay. In both Figures channel 2 represents Power Good 2, channel 3 represents Power Good 3, and channel 4 represents Power Good 4. In figure 3, channel

1 illustrates the Pin Detect signal — note that it is almost coincident with the rise of Power Good 4. In figure 4, channel 1 represents Power Good 1.

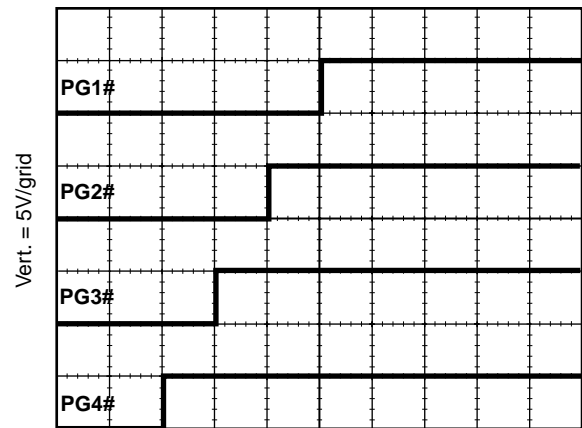
Figure 5 illustrates a faster power down sequence. The delay between Power Good outputs is 60µs. This was accomplished by changing the timing capacitor values to 6.8nF, 13.6nF, and 20.4nF from 100nF, 200nF, and 300nF.



Horiz. = 2ms/grid

3021 Fig02

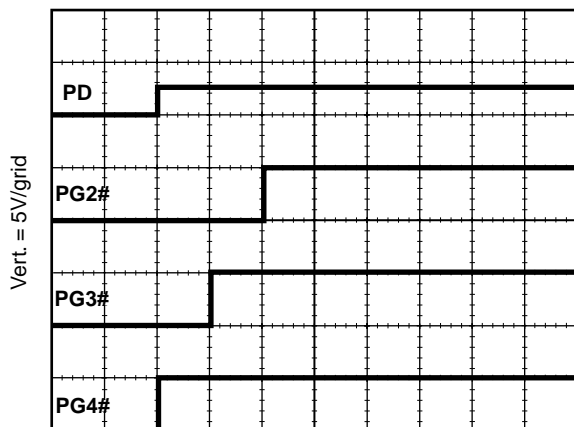
Figure 2. Power Up Sequence



Horiz. = 1ms/grid

3021 Fig04

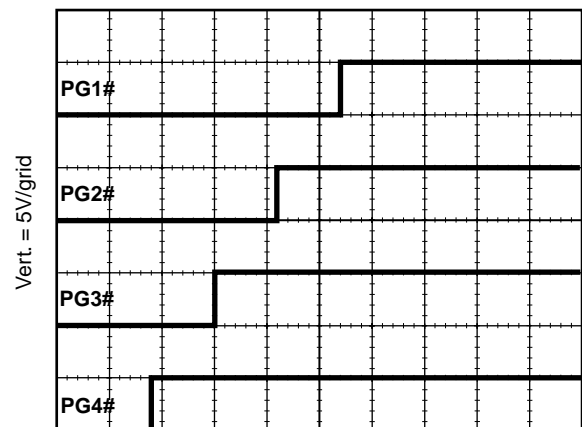
Figure 4. Power Down Sequence



Horiz. = 1ms/grid

3021 Fig03

Figure 3. Power Down Sequence with Pin Detect



Horiz. = 50µs/grid

3021 Fig05

Figure 5. Fast Power Down Sequence



APPLICATION CIRCUIT 2

Figure 6 illustrates another version of the power down sequence circuit. In this case a Schmitt trigger replaces transistor Q6. The logic sense is maintained by using two triggers in series. An input pull-up resistor ensures

logic high input when the board is unplugged. The switch point of the triggers — at 2.5V versus 0.6V in the previous case — and the hysteresis of the triggers makes this solution more immune to noise.

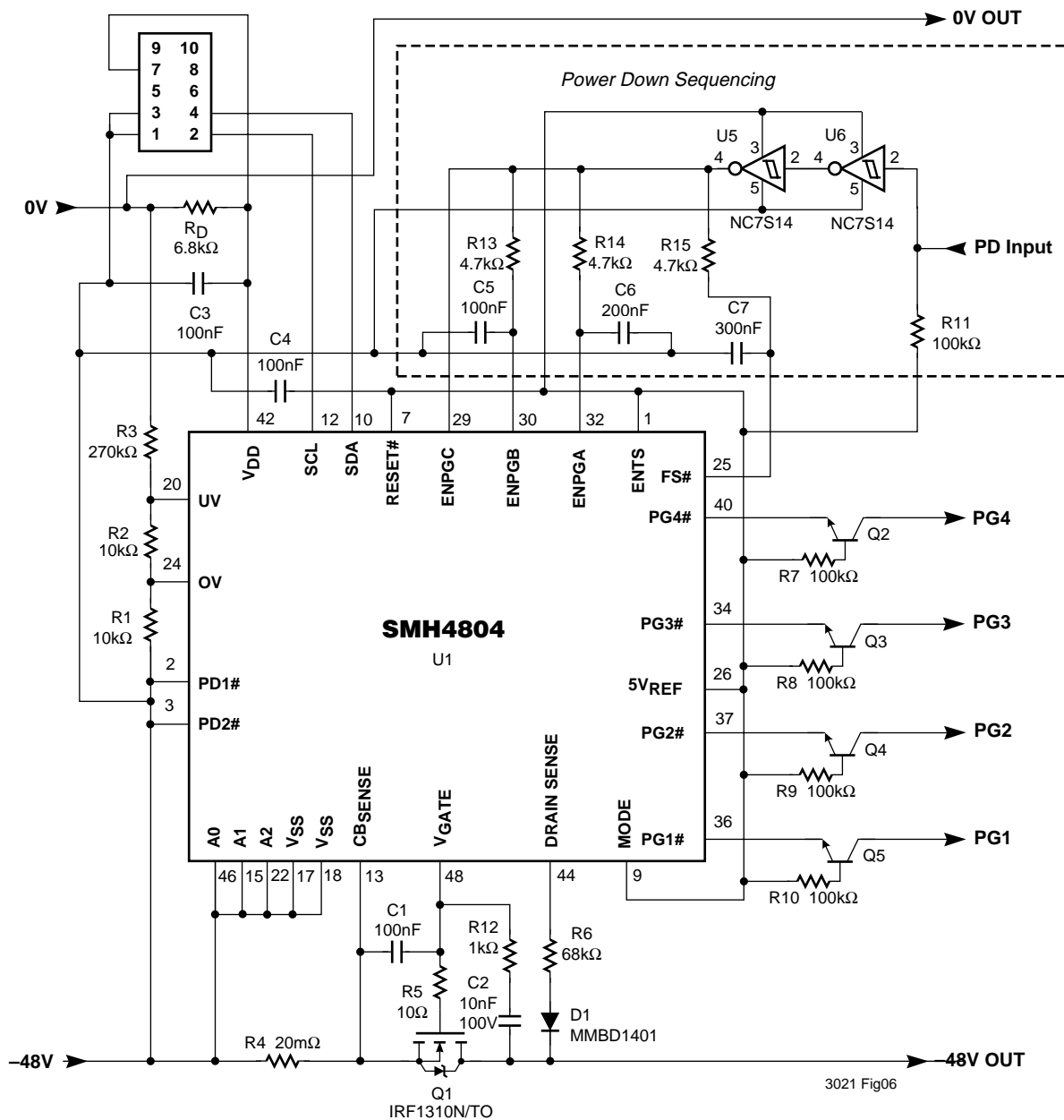


Figure 6. Application Circuit 2 Schematic



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