

CompactPCI[®] Hot Swap Design Solutions

The SMH4042 is a **CompactPCI** friendly hot swap controller. Its functions allow the SMH4042 to be used in a wide variety of add-in-board hot swap applications, such as computer telephony and industrial control.

The SMH4042 can act as an autonomous controller used solely to switch and monitor voltages on the add-in-card. However, based on its flexibility it can also be used in more sophisticated high availability systems that require handshaking with a host processor.

This paper will show implementations of the **CompactPCI** Hot Swap specification based upon major functional blocks. Some of the blocks will be needed regardless of the level of the hot swap spec trying to be attained, while other blocks may be used at the discretion of the designer.

Background

CompactPCI terms and definitions

Platform - the platform provides the physical structure for the boards. This includes the backplane, cooling and power supplies and, because the backplane is passive, a system host.

System Host - The central resource that provides services like clocks and arbitration for the **CompactPCI** bus.

Board - Any circuit board in the system [not including the system host]. Boards can be one of three categories.

Non Hot Swap do not have all the features for hot swap.

Basic Hot Swap boards have the minimum features required.

Full Hot Swap boards have the minimum features plus ability for software connection control.

Various combinations of System Host, Platform and Boards make up different system models. Those models with which we are concerned are Basic Hot Swap, Full Hot Swap and High Availability.

Figure 1 illustrates a full implementation block diagram of a generic **CompactPCI** board and platform connector. The SMH4042 is an integral block in the board's implementation where it is the primary controlling interface to the P1 connector. In a basic hot swap implementation the backend power circuits and bus interface circuits need to be addressed. As a full hot swap board (for use in a high availability system) the ejector/injector logic block needs to be provided as do the handshake signals between the host board and the SMH4042. Details on implementing each section will be discussed and a complete implementation will be given as a conclusion.

For simplicity of illustration the P1 pin functions in the block diagram are shown in their relative vertical position, but not their horizontal position. The pins on P1 are in three (3) staged lengths; the longest being those supplying voltages, the medium length pins providing signal paths, and the shortest being the BD_SEL# signal (one method of indicating board insertion).

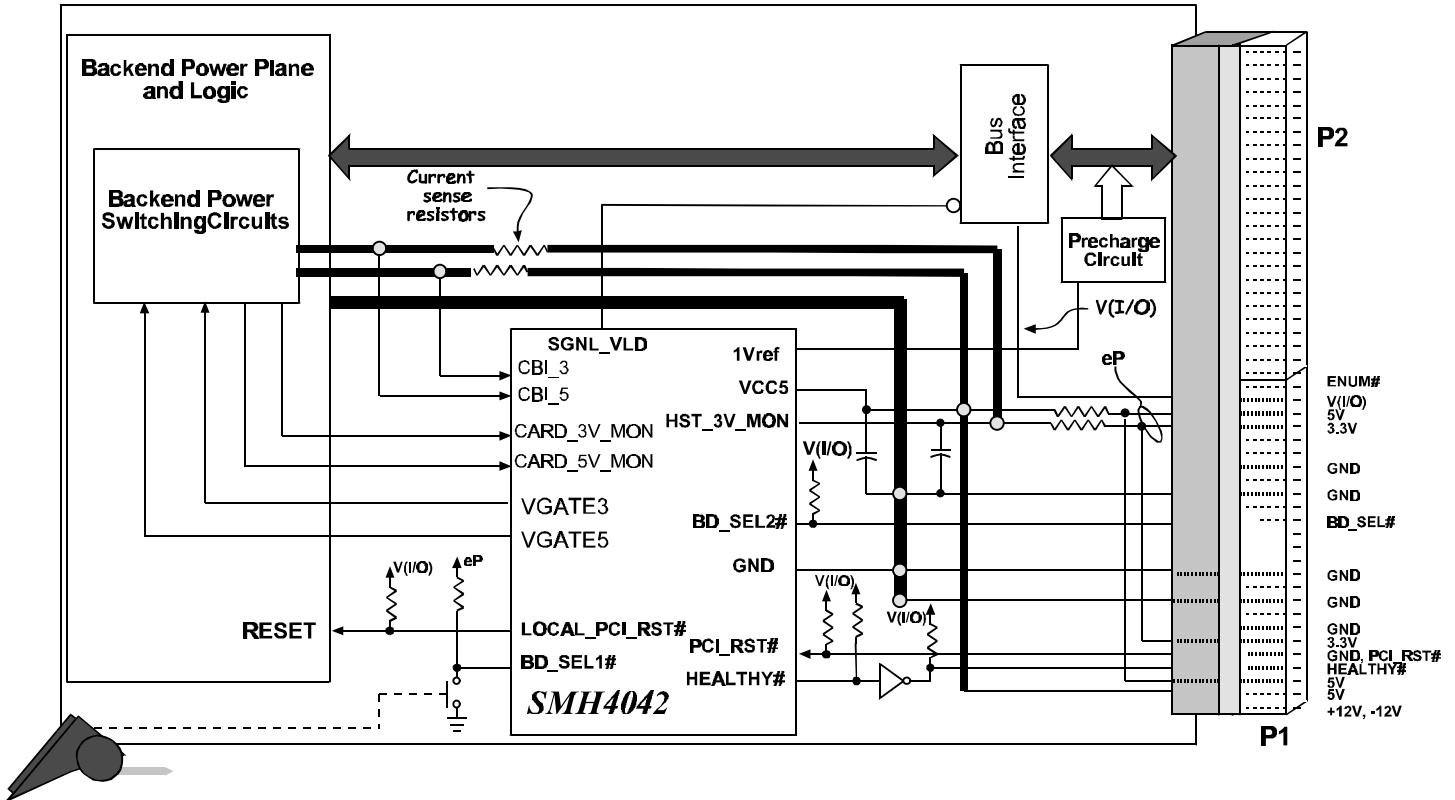


Figure 1. Generic CompactPCI Hot Swap add-in card block diagram.

Need for Hot Swap

Hot Swap is the act of removal and insertion of cards into a platform while that system is operational. This process should not cause any undue perturbations of the system's power supplies or the system's I/O signals. Protection of the card's circuitry also needs to be taken into account in this process.

Sequence of Board Insertion

Although there are a number of interim steps involved in the process, those of concern to the designer are listed below. The sequencing is predicated on the assumption that staggered pins on the receiving connector (P1) will be employed. The staggered pins provide a physical means for timing the operation and also a method to insure the card has been positively seated.

As the card is inserted into the platform:

1. Voltage potentials on the front panel and card's ground plane are discharged to chassis ground
2. The board contacts the long pins that supply +5V, +3.3V, Gnd and V(I/O)
 - a. These contacts provide early power to the control circuit (SMH4042) and bus interface circuits and the de-coupling capacitors are charged
 - b. The control circuit immediately begins driving **LOCAL_PCI_RESET#** and maintains a reset condition until the connection process has been completed
 - c. Early power is stable and the bus signals are pre-charged
 - d. The Hot Swap Blue LED is illuminated [**Full Hot Swap** only]
3. Medium length pins begin to make contact
 - a. Bus pins begin to track bus levels
 - b. Medium length power pins short the current limit resistor and provide voltage at the power MOSFETS for backend power (Backend still turned off)
4. Finally the BD_SEL# pin makes contact

Early Power

Early power (**eP**) is the voltage provided on the long pins. This includes 5V, 3.3V, GND and V(I/O). These voltages are used to power the SMH4042, the bus interface circuits and to charge the **eP** capacitors. Supply glitches that could inadvertently generate system resets may be caused by excessive in-rush currents trying to charge the **eP** capacitance. To address this issue the capacitance for the early 5V, 3.3V and V(I/O) is limited to 8.8 μ F and the board should have current limiting resistors in line with the long pins for 5V, 3.3V and V(I/O). This is illustrated in figure 2.

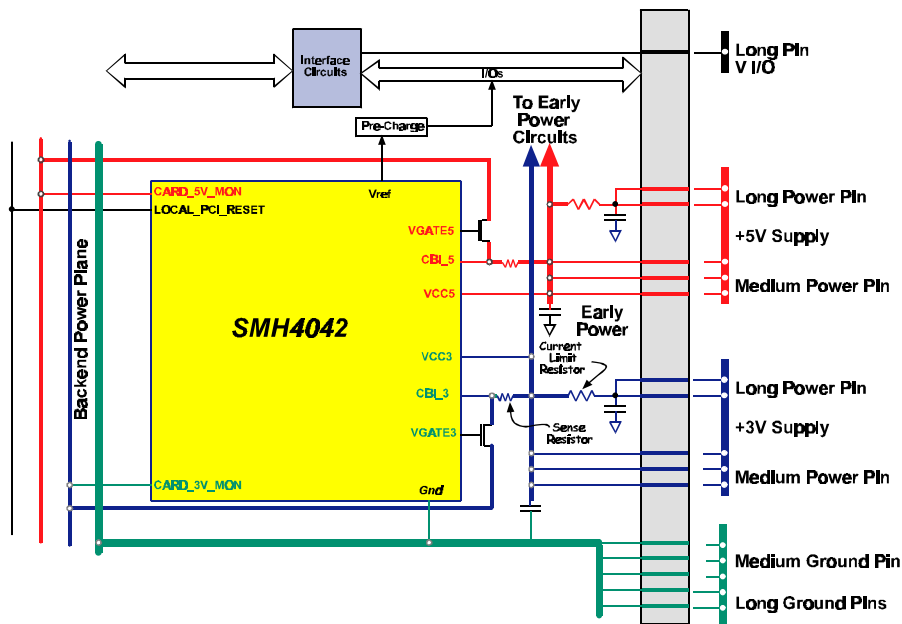


Figure 2. Power control and power plane isolation

Early power voltages are applied to the SMH4042 and it immediately begins driving the **LOCAL_PCI_RESET#** output and it will force the VGATE outputs to a known off-condition. The 1Vref output immediately becomes active providing a reference for the pre-charge circuit. At the same time V(I/O) is applied to certain pull-ups and also to any interface I/O circuitry. All of these activities must occur within 4ms of the long pins first engaging the card.

BUS CONDITIONING

The board's I/Os need to be preconditioned prior to contacting the medium length pins. All PCI signals must be in a high impedance state and pre-charged through pull-up resistors to a 1V level with the following exceptions:

PCI_RST#, **ENUM#**, **INTA#**, **INTB#**, **INTC#**, **INTD#**, and **REQ#** which should be "pulled-up" to V(I/O). It is also recommended to tie **HEALTHY#** to V(I/O) through a pull-up resistor.

Placing the I/Os in a high impedance state is a relatively easy task. The selected interface device, such as a CMOS switch, needs to be powered-on with V(I/O) and the ENABLE input or ON input needs to be connected to a SMH4042 output, such as **SGNL_VLD#**. **SGNL_VLD#** is an open drain active low output indicating the card-side power is valid and **LOCAL_PCI_RESET#** is false.

Figure 3 shows a simple method of developing the 1V volt pre-charge. The amplifier is available in an inexpensive SOT23 package making this a great board area saver. Depending upon the application requirements there are a number of silicon solutions that employ low on-resistance CMOS switches. Figure 3 shows one implementation using a QuickSwitch[®] from Quality Semiconductor. This particular device exhibits very Flat R_{ON} characteristics from 0 to 5V. The only drawback is the extra space required for the external pull-up resistors.

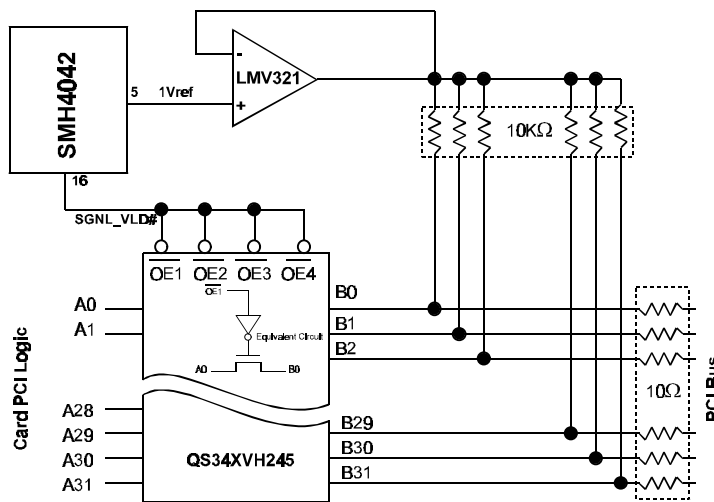


Figure 3. Pre-Charge Reference Voltage Circuit and CMOS switch implementation

Figure 4 shows another implementation, but the pull-up resistor structure is incorporated in the switch. The circuit also automatically switches the bias voltage out of the circuit as the CMOS switches are enabled. A potential advantage is the ability to place the interface closer to the edge of the card. The board designer should evaluate their requirements and design goals and determine their best solution. The bus switches are available from both Texas Instruments and Pericom Semiconductor.

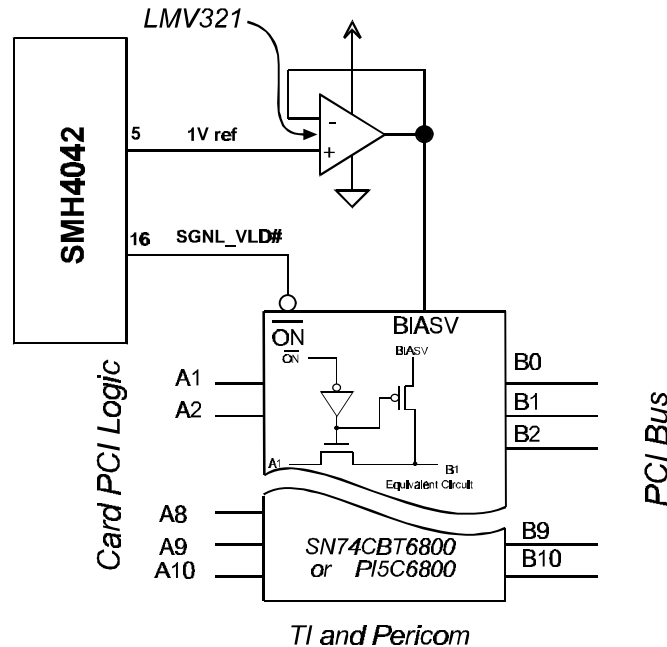


Figure 4. CMOS switch with integrated bias voltage pull-up structure.

The Rest of the Power

The medium length pins provide the balance of the power to the board; and once they are engaged they will short out the current limiting resistors. I/Os will make contact and some of the handshake signals to/from the SMH4042 will be made. The backend logic power supply is still isolated.

As the board is fully seated the last pin, BD_SEL#, makes contact and pulls one or both of the BD_SEL# inputs to ground. Simultaneously, the injector is locked in place, and optionally, closes a micro-switch which grounds the second BD_SEL# input. At this point the SMH4042 should have most of the input information needed to power the backend logic.

Powering the Backend

With the card fully seated the SMH4042 will commence sequencing power to the backend only if: the VCC and HST_3V_MON inputs are at or above their thresholds; both BD_SEL# inputs are grounded, and PWR_ON is true. The backend will continue to be held in reset and VGATE5 and VGATE3, slew rate limited high side driver outputs, will be turned on. The VGATE output voltage is generated by an on-board charge pump.

As the power MOSFETs are turned on the SMH4042 will monitor the backend voltage and the current of the two supplies. If an overcurrent condition is detected the SMH4042 will immediately turn off the VGATE outputs. The SMH4042 will monitor the voltage on the load side of the FETs and continue asserting the LOCAL_PCI_RESET# output until the voltages are at or above their specified thresholds.

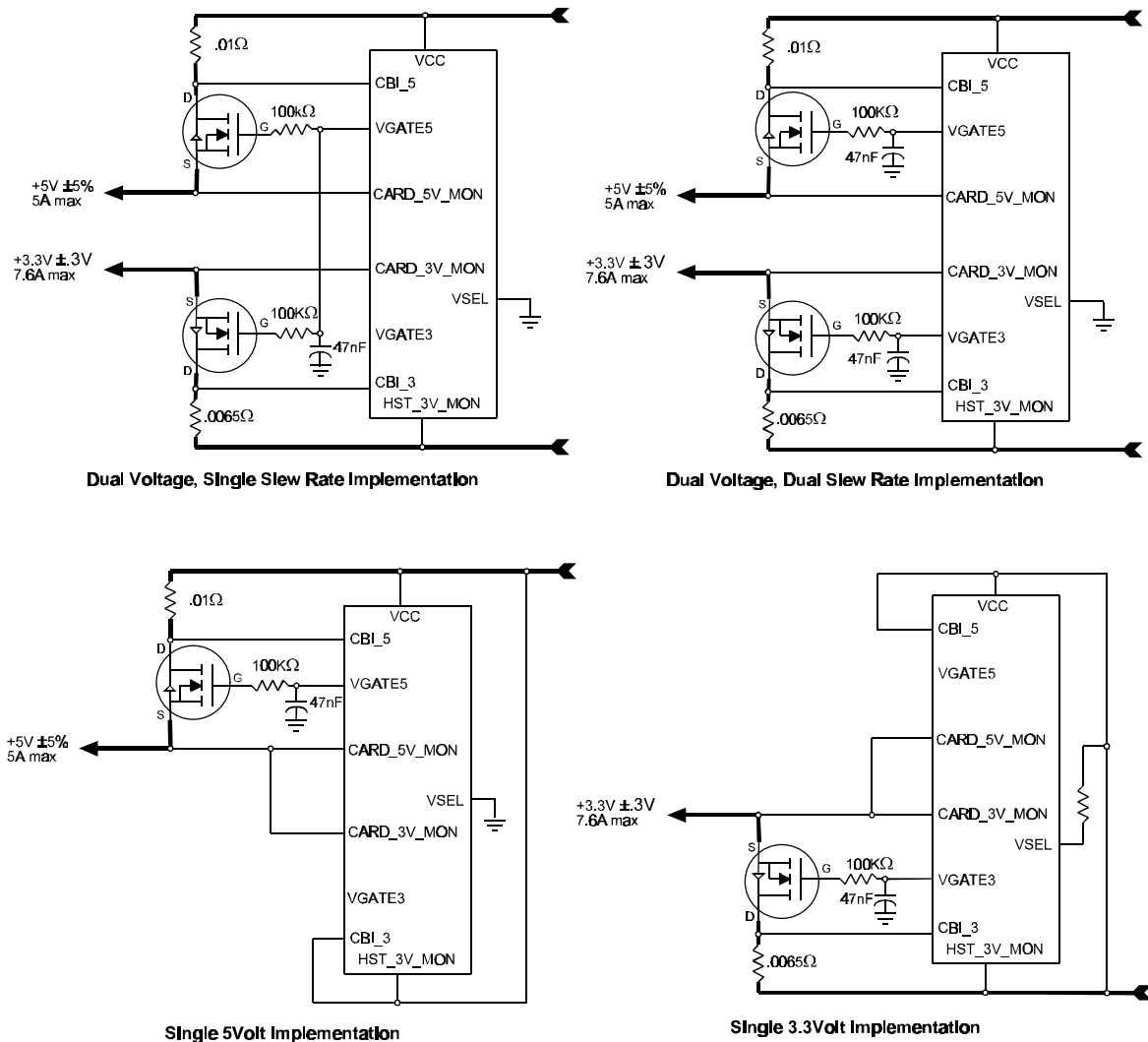


Figure 5. Power MOSFET circuit options.

There are four basic configurations for turning on the power to the backend. These are illustrated in Figure 5. Regardless of the method chosen for a dual voltage application, the designer must take into consideration the skew between +5V and +3.3V turning on. Generally you will want the +5V turning on first; therefore, the SMH4042 has provided a self-imposed skew of a one-diode drop difference between VGATE5 and VGATE3. The resultant outputs are shown in Figure 6.

The VGATE output ramp rate is nominally set at 250V/s; it can be accelerated by injecting current into the ISLEW input or alternatively slowed down by adding capacitance to the outputs. Refer to the SMH4042 data sheet for the timing details.

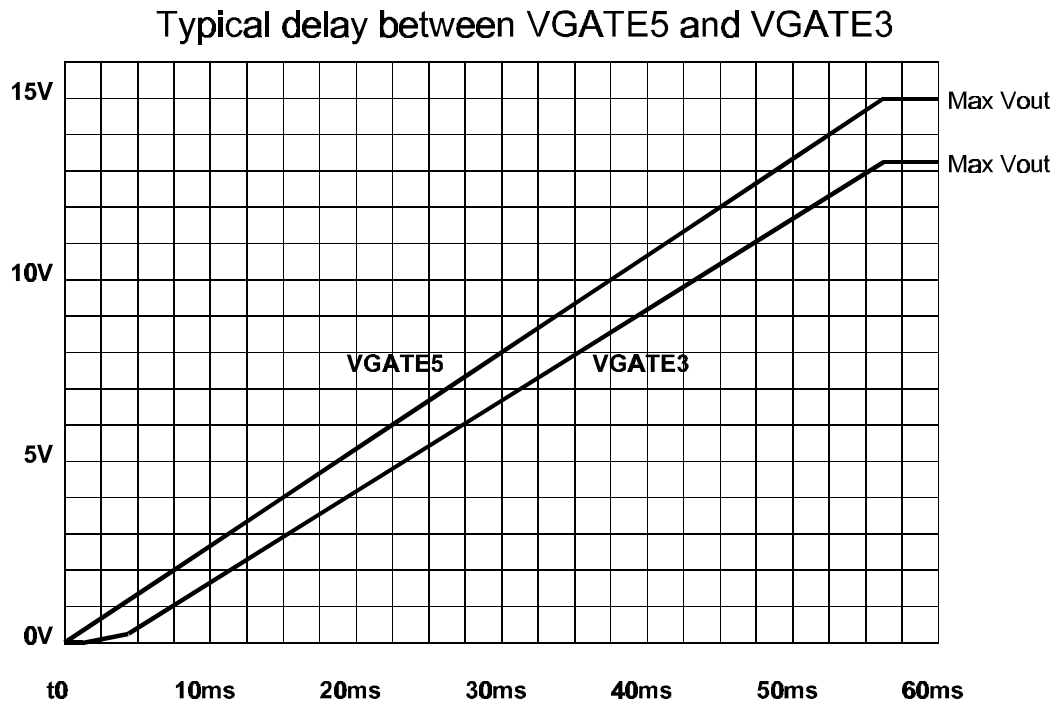


Figure 6. Skew between VGATE5 and VGATE3.

Once the voltages on the backend are at or above their thresholds the SMH4042 will drive the HEALTHY# output to indicate to the host system the power on the board is valid.

Software Connection Control

So far the discussions have only covered hardware connection control, the basic function of monitoring the insertion process and cleanly powering up the board and finally indicating to the host that the board is *HEALTHY*. These are the minimum requirements for implementing the *Basic Hot Swap* board.

Full Hot Swap boards have the minimum features plus the ability for software connection control. The additional resources needed are:

- An *ENUM#* signal, which is an open collector bussed signal.

- A switch, actuated with the lower injector handle.

- An LED to indicate status of the software connection process.

The *ENUM#* signal indicates a board has been freshly inserted or is about to be extracted. "Full Hot Swap Boards assert *ENUM#* until serviced by the Hot-Plug System Driver." *ENUM#* is activated by a micro-switch located in the lower injector handle.

A blue LED, located on the front of the board, is illuminated when it is permissible to extract the board. During the insertion process the LED is illuminated immediately by the hardware. On the host system the *BD_SEL#* signal has a weak pull-down. As the board is inserted the pull-up, on the board, overrides the pull-down generating a change in state to the host. The host can now respond and activate the power-on circuit driving the *BD_SEL#* signal low. (see figure 10)

The LED will stay on until the host system pulls the *BD_SEL#* signal low and until the board is fully powered-on. At this point the operator may fully close the injector closing the switch that generates the *ENUM#* signal. The *ENUM#* signal will stay active until the host system clears the board's status register.

The LED remains off until activated by the host software indicating the board may be extracted. It is assumed the operator will begin the extraction process by unlocking the injector (the switch opens) and then waits for the LED to be illuminated before removing the board.

The blue LED is driven by the *RESET* output of the SMH4042. This is the same as the *LOCAL_PCI_RESET#* for the backend logic. Figure 10 shows a current boost circuit for the reset. This ensures enough current sink capability for the LED and all of the backend logic.

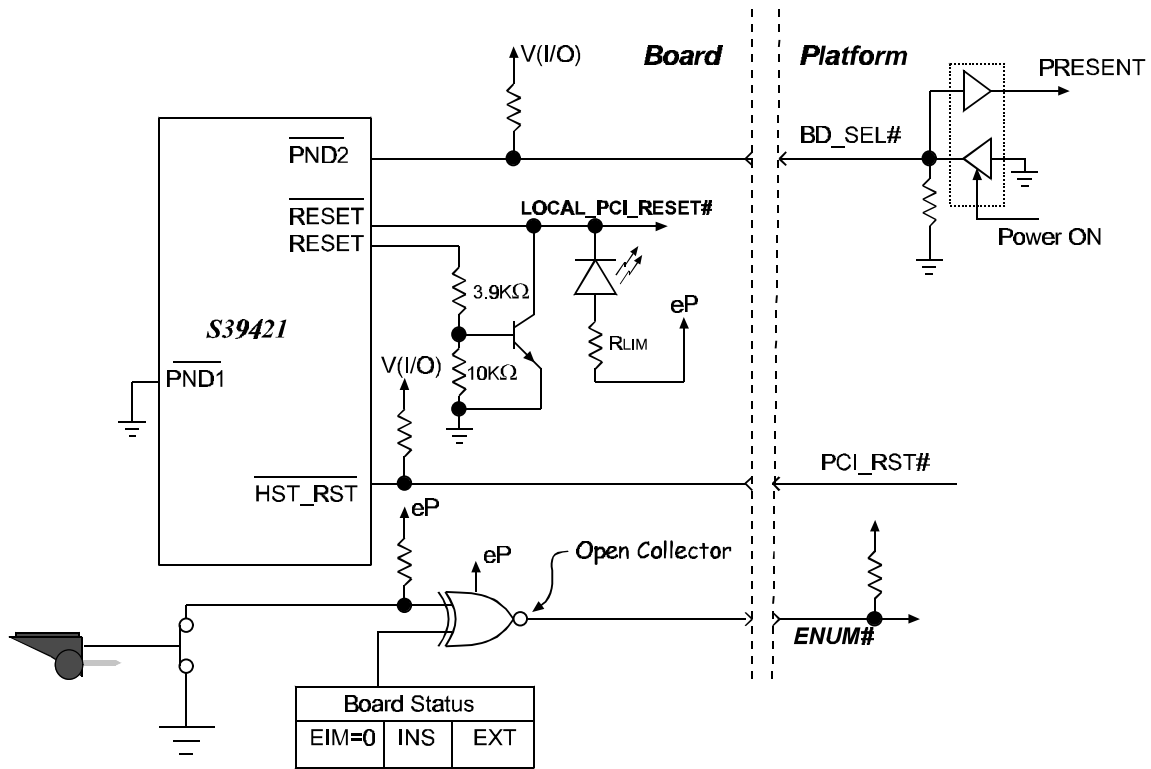


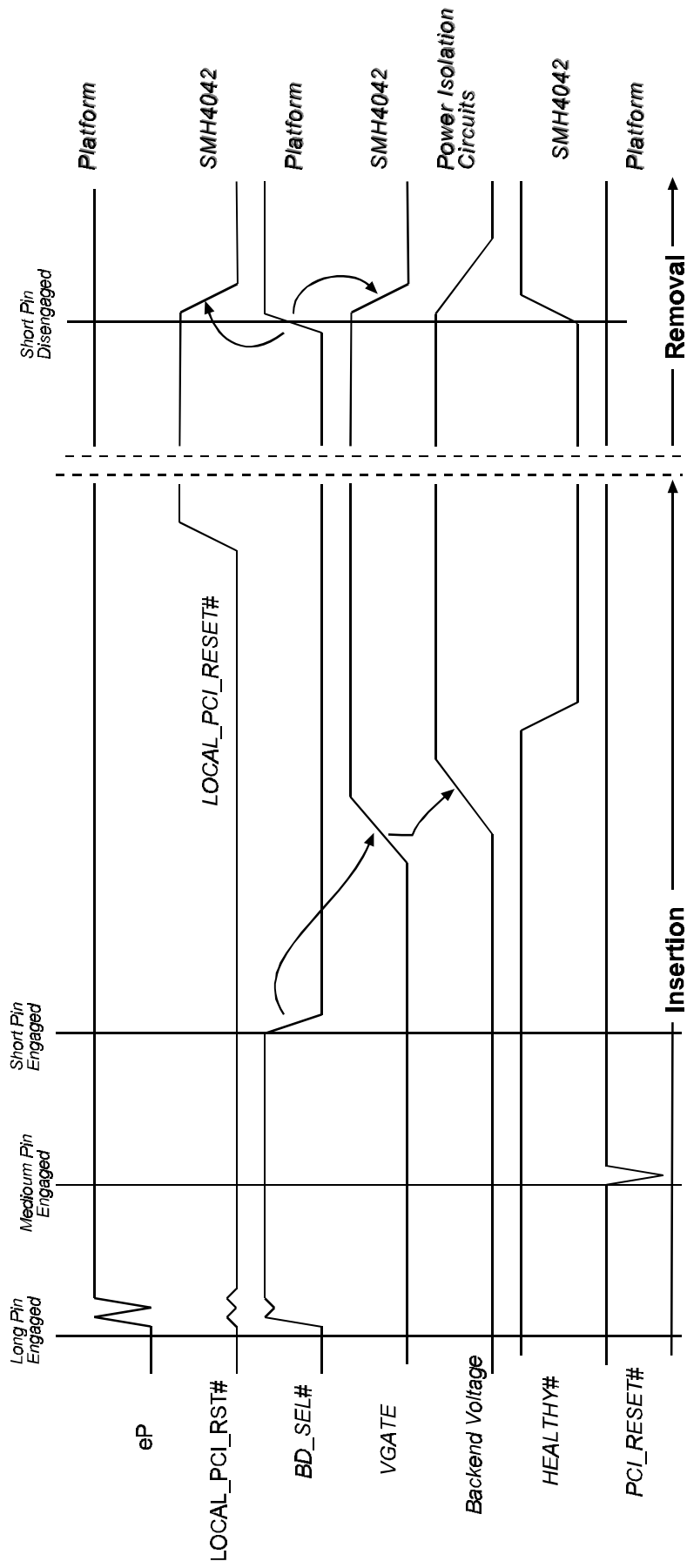
Figure 7. Example of the software connection handshake signals.

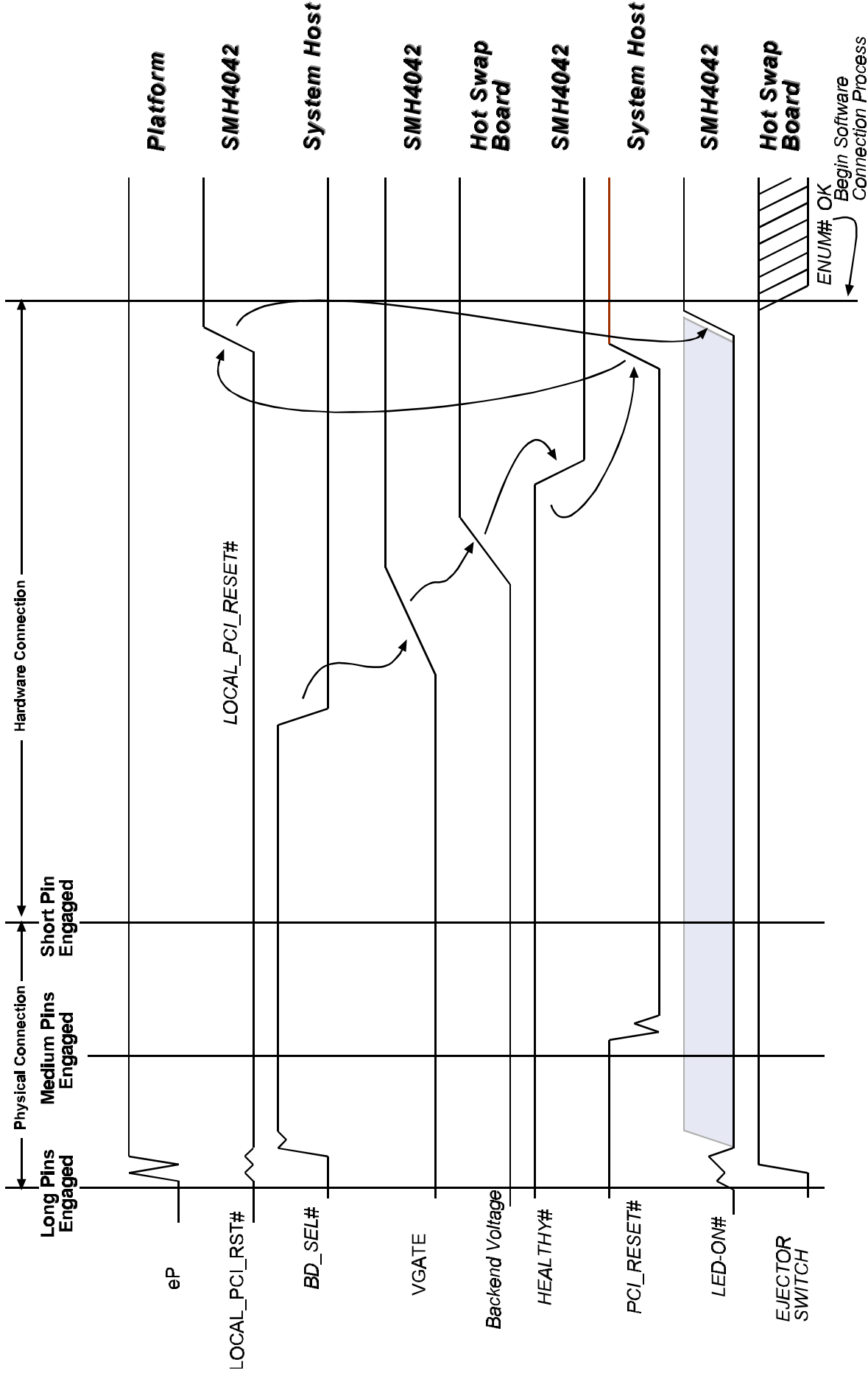
The figure on the following page illustrates a full hot swap implementation using a Tundra QSPANII bridge chip. Note how the tundra device incorporates the ENUM# logic. It also has a configuration download interface that can directly access the two-wire serial interface memory array of the SMH4042.

Conclusion

The SMH4042 has been shown to easily act as the power control circuit for a **CompactPCI** Hot Swap board. It provides enough flexibility to the designer that they may use the SMH4042 on either a **Basic Hot Swap** board or **Full Hot Swap** board and then use a minimum amount of support circuitry.







Power-On Sequence for a Full Hot Swap Board Using the S39421