

Hot Swap Implementations with the Summit S39421

The S39421 is an economical general-purpose hot swap controller. Its functions allow the S39421 to be used in a wide variety of add-in-board hot swap applications, such as computer telephony and industrial control.

The S39421 can act as an autonomous controller used solely to switch and monitor voltages on the add-in-card. However, based on its flexibility it can also be used in more sophisticated high availability systems that require handshaking with a host processor.

This paper will show implementations of the **CompactPCI** Hot Swap specification based upon major functional blocks. Some of the blocks will be needed regardless of the level of the hot swap spec trying to be attained, while other blocks may be used at the discretion of the designer.

Background

CompactPCI terms and definitions

Platform - the platform provides the physical structure for the boards. This includes the backplane, cooling and power supplies and, because the backplane is passive, a system host.

System Host - The central resource that provides services like clocks and arbitration for the **CompactPCI** bus.

Board - Any circuit board in the system [not including the system host]. Boards can be one of three categories.

Non Hot Swap do not have all the features for hot swap.

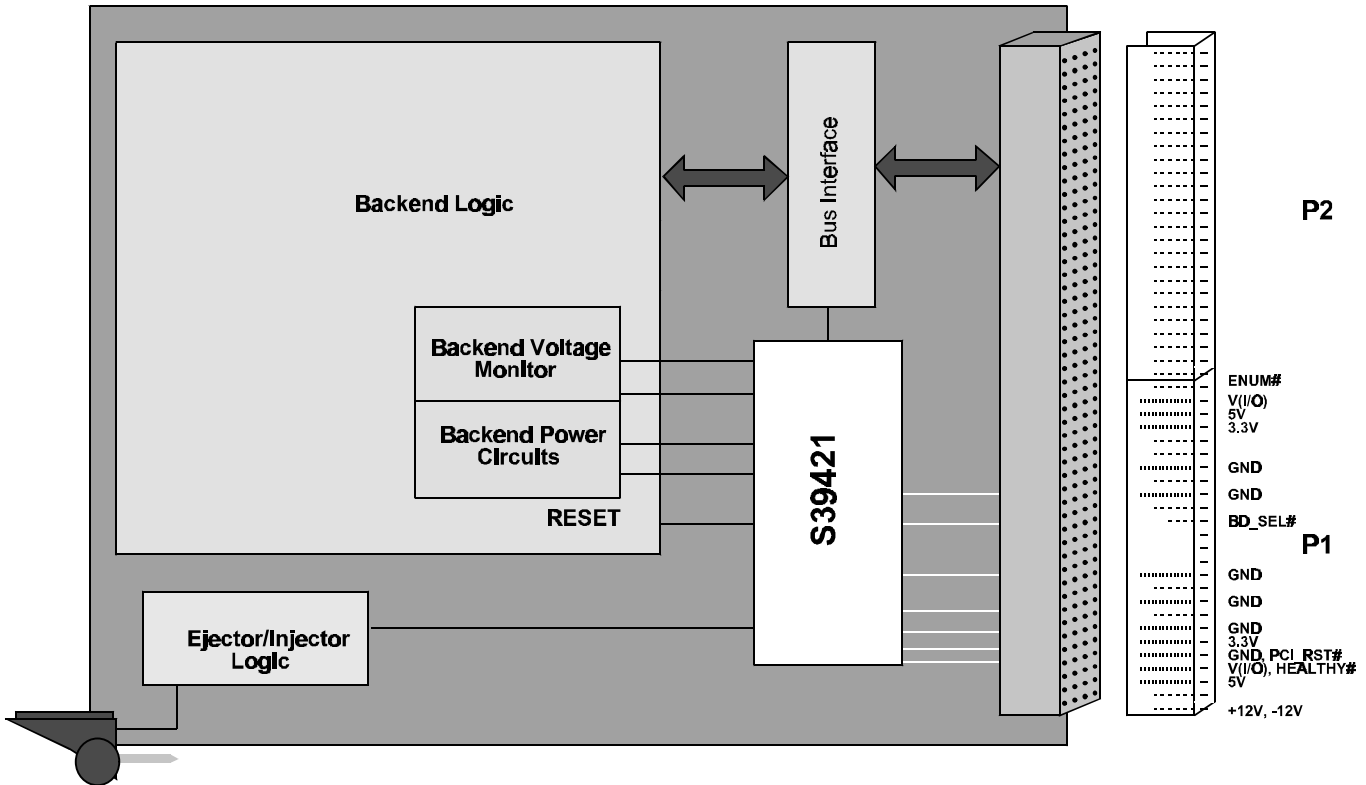
Basic Hot Swap boards have the minimum features required.

Full Hot Swap boards have the minimum features plus ability for software connection control.

Various combinations of System Host, Platform and Boards make up different system models. Those models with which we are concerned are Basic Hot Swap, Full Hot Swap and High Availability.

Figure 1 is a functional block diagram of a generic **CompactPCI** board and platform connector. The S39421 is an integral block in the board's implementation where it is the primary controlling interface to the P1 connector. In a basic hot swap implementation the backend power circuits and bus interface circuits need to be addressed. As a full hot swap board (for use in a high availability system) the ejector/injector logic block needs to be provided as do the handshake signals between the host board and the 39421.

For simplicity of illustration the P1 pin functions in the block diagram are shown in their relative vertical position, but not their horizontal position. The pins on P1 are in three (3) staged lengths; the longest being those supplying voltages, the medium length pins providing signal paths, and the shortest pins being the BD_SEL# signal (one method of indicating board insertion).



Need for Hot Swap

Hot Swap is the act of removal and insertion of cards into a platform while that system is operational. This process should not cause any undue perturbations of the system's power supplies or the system's I/O signals. Protection of the card's circuitry also needs to be taken into account in this process.

Sequence of Board Insertion

Although there are a number of interim steps involved in the process those of concern to the designer are listed below. The sequencing is predicated on the assumption that staggered pins on the receiving connector (P1) will be employed. The staggered pins provided a physical means for timing the operation and also a method to insure the card has been positively seated.

As the card is inserted into the platform:

1. Voltage potentials on the front panel and card's ground plane are discharged to chassis ground
2. The board contacts the long pins that supply +5V, +3.3V, Gnd and VIO

- a. These contacts provide early power to the control circuit (S39421) and bus interface circuits and the de-coupling capacitors are charged
 - b. The control circuit immediately begins driving **LOCAL_PCI_RESET#** and maintains a reset condition until the connection process has been completed
 - c. Early power is stable and the bus signals are pre-charged
 - d. The Hot Swap Blue LED is illuminated [**Full Hot Swap** only]
3. Medium length pins begin to make contact
 - a. Bus pins begin to track bus levels
 - b. Medium length power pins short the current limit resistor and provide voltage at the power MOSFETS for backend power (Backend still turned off)
 4. Finally the BD_SEL# pin makes contact

Early Power

Early power (eP) is the voltage provided on the long pins. This includes 5V, 3.3V, GND and V(I/O). These voltages are used to power the S39421, the bus interface circuits and to charge the eP capacitors. Supply glitches that could inadvertently generate system resets may be caused by excessive in-rush currents trying to charge the eP capacitance. To address this issue the capacitance for the early 5V, 3.3V and V(I/O) is limited to 8.8 μ F and the board should have current limiting resistors in line with the long pins for 5V, 3.3V and V(I/O).

The Hot Swap spec requires the bus interface to be in a high impedance state when the signal pins contact the connector. In addition, the I/Os must be pre-charged to a 1V ($\pm 20\%$) potential. In this way the board being inserted will be seen as an electrically benign intruder on the operating system's bus.

In Figure 2, the card is just making contact with the long pins. V(I/O) is directed to the bus interface logic and a number of pull up resistors. V(I/O) can be either 3.3V or 5V, depending upon the system definition. It is imperative the interface circuits are powered on and placed in a high impedance state.

Early power is distributed to the S39421 to initially activate its reset outputs (both an active high and active low output are available), force the VGATE outputs to a known off-condition and provide the valid outputs to the interface circuits, insuring they power-up in the high impedance state. The pre-charge circuit is activated and the I/Os are forced to a 1V potential. All of these activities must occur within 4ms of the long pins first engaging the card.

BUS CONDITIONING

The board's I/Os need to be preconditioned prior to contacting the medium length pins. All PCI signals must be in a high impedance state and pre-charged through pull-up resistors to a 1V level with the following exceptions:

PCI_RST#, **ENUM#**, **INTA#**, **INTB#**, **INTC#**, **INTD#**, and **REQ#** which should be "pulled-up" to V(I/O). It is also recommended to tie **HEALTHY#** to V(I/O) through a pull-up resistor.

Placing the I/Os in a high impedance state is a relatively easy task. The selected interface device, such as a CMOS switch, needs to be powered-on with V(I/O) and the ENABLE input or ON input needs to be connected to a S39421 output, such as SGNL_VLD\ . SGNL_VLD\ is an open drain active low output indicating the card-side power is valid and LOCAL_PCI_RESET# is false.

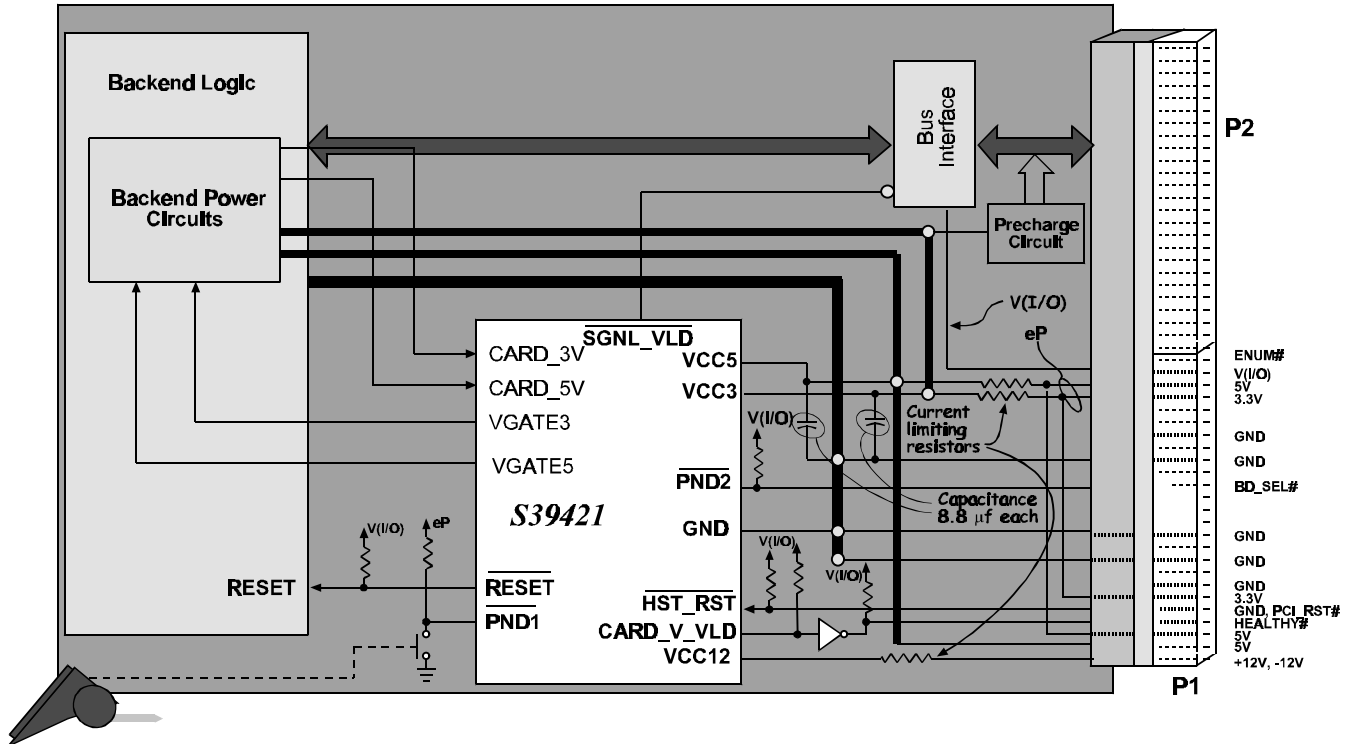


Figure 2. Board Contacting Long Pins

Figure 3 shows an inexpensive method of developing the 1V volt pre-charge. The voltage reference and amplifier are available in SOT23 packages and combined with the resistors in the circuit the amount of board space consumed is about equivalent to an 8-lead SOIC.

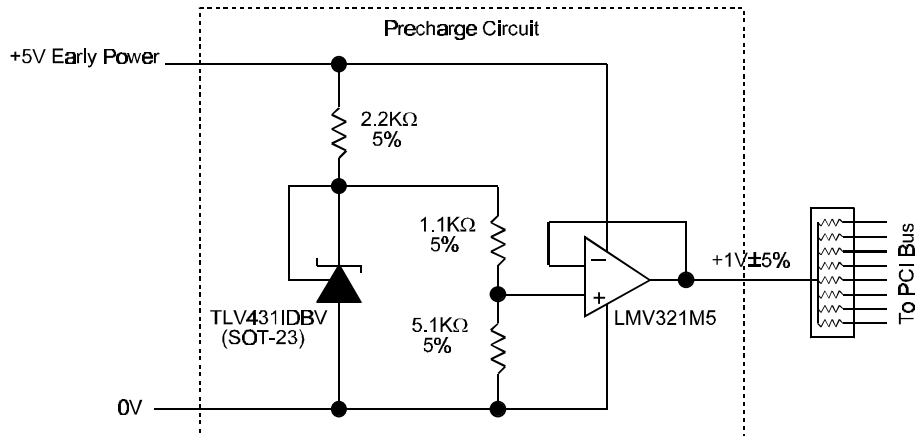


Figure 3. Pre-Charge Reference Voltage Circuit

Depending upon the application requirements there are a number of silicon solutions that employ low on-resistance CMOS switches. Figure 4 shows one implementation using a QuickSwitch[®] from Quality Semiconductor. This particular device exhibits very Flat R_{ON} characteristics from 0 to 5V. The only drawback is the extra space required for the external pull-up resistors.

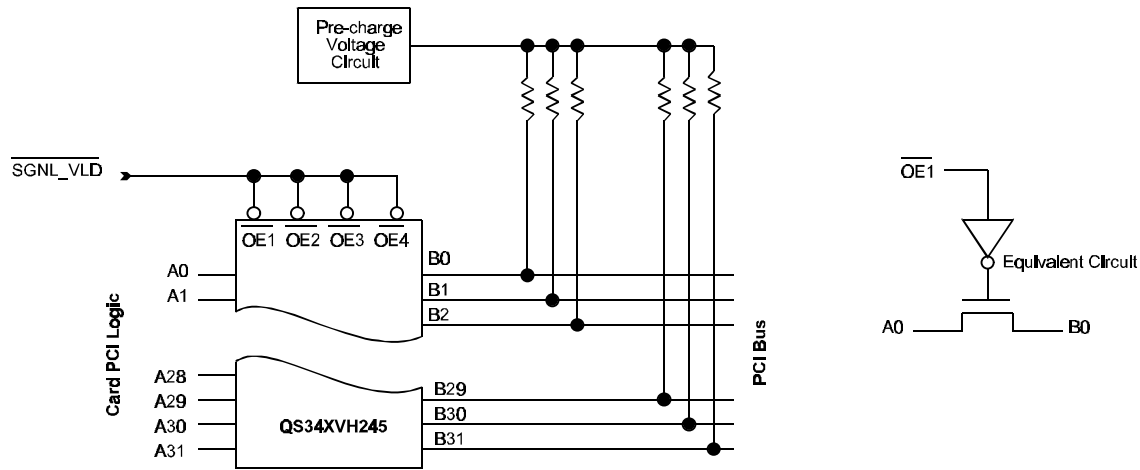


Figure 4. CMOS Switch Implementation

Figure 5 shows another implementation, but the pull-up resistor structure is incorporated in the switch. The circuit also automatically switches the bias voltage out of the circuit as the CMOS switches are enabled. A potential advantage is the ability to place the interface closer to the edge of the card. The board designer should evaluate their requirements and design goals and determine their best solution. The bus switches are available from both Texas Instruments and Pericom Semiconductor.

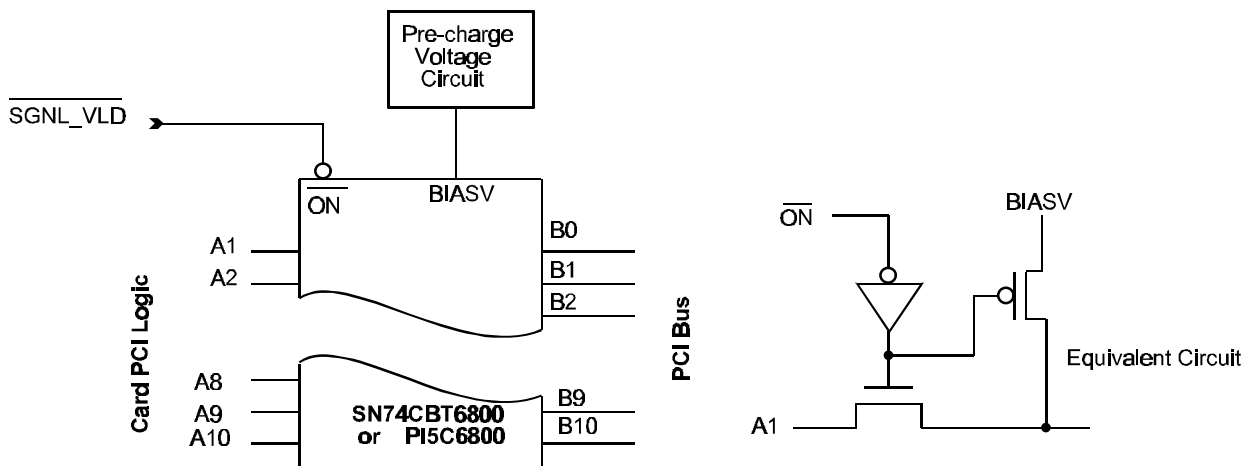


Figure 5. CMOS switch with integrated bias voltage pull-up structure.

After the long pins are fully engaged the medium length pins make contact. the balance of the power supply pins are engaged and they will short out the current limiting resistors. I/Os will make contact and some of the handshake signals to/from the S39421 will be made. The backend logic power supply is still isolated.

As the board is fully seated the last pin, BD_SEL#, makes contact and pulls one of the PND inputs to ground. Simultaneously, the injector is locked in place, and optionally, closes a micro-switch which grounds the second PND input. At this point the S39421 should have most of the input information needed to power the backend logic.

The S39421 will now proceed with the sequencing of the back end power and maintain status inputs to the host system. Figure 7 is a simplified diagram of the "OK-to-power-up-backend" (OK_PUB) logic. The S39421 can operate as a 5V only controller, 3V only controller or as a dual voltage controller. This is determined by the state of the VSEL input. For this example, assume it is a dual voltage controller; therefore, both VCC5 and VCC3 must be valid. Let's further assume for this example HST_PWR is true, and both PND1 and PND2 are grounded. These five conditions will generate OK_PUB, which in turn enables the VGATE outputs and the DRVREN\ output.

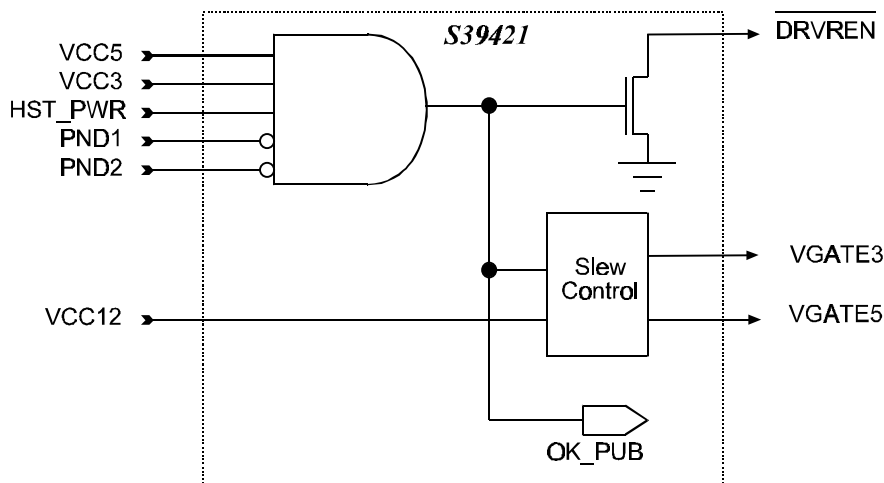


Figure 7. Logic representation of conditions needed to turn on the backend voltages

VGATE3 and VGATE5 are slew rate limited high side driver outputs that are used to turn on external power MOSFETs that isolate the 5V and 3.3V from the backend logic. The Hot Swap spec states, "During turn on and off, the maximum rate of change of current on the +5V and +3.3V supplies shall be limited to 1.5A/ms." The S39421 provides the designer a great deal of flexibility in order to meet the individual board's characteristics. The VGATE output ramp rate is nominally set at 250V/s; it can be accelerated by injecting current into the ISLEW input or alternatively slowed down by adding capacitance to the outputs. Refer to the S39421 data sheet

for the timing details. Figure 8 illustrates a typical implementation. Note the feedback of the backend voltages to the S39421. This fulfills another **CompactPCI** Hot Swap requirement, "The power isolation circuitry is responsible for insuring that the back end voltages are within tolerance." The board must also provide a signal (**HEALTHY#**) back to the host system indicating the back end voltage is within spec.

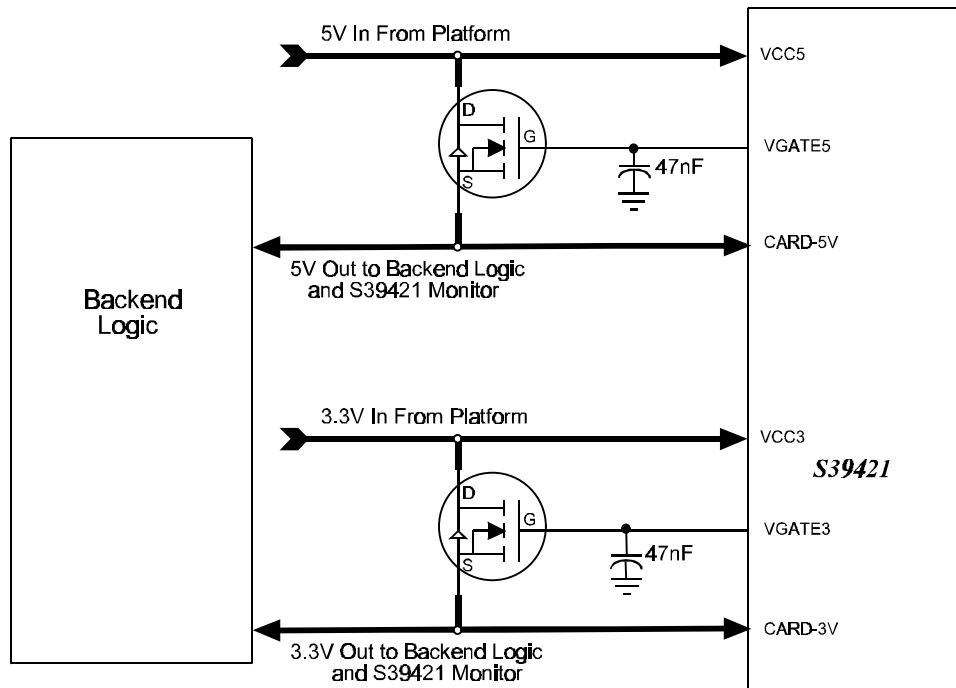


Figure 8. Typical power MOSFET power isolation circuit.

The next stage involves four related signals that are generated from a similar set of inputs. The first is **CARD_V_VLD** an active-low open-drain output, which is false when pulled low and true when released. It will be true only when the monitored backend voltages are in spec. The output can be inverted to provide the PCI **HEALTHY#** signal. The other three outputs (**RESET**, **RESET** and **SGNL_VLD**) are different forms of reset that generally track each other. **SGNL_VLD** will normally lag the reset outputs during the release phase but will lead turning-on if **OK_PUB** should go false prior to **CARD_V_VLD** going false. Figure 9 is a simplified illustration of the implementation of the logic controlling the resets.

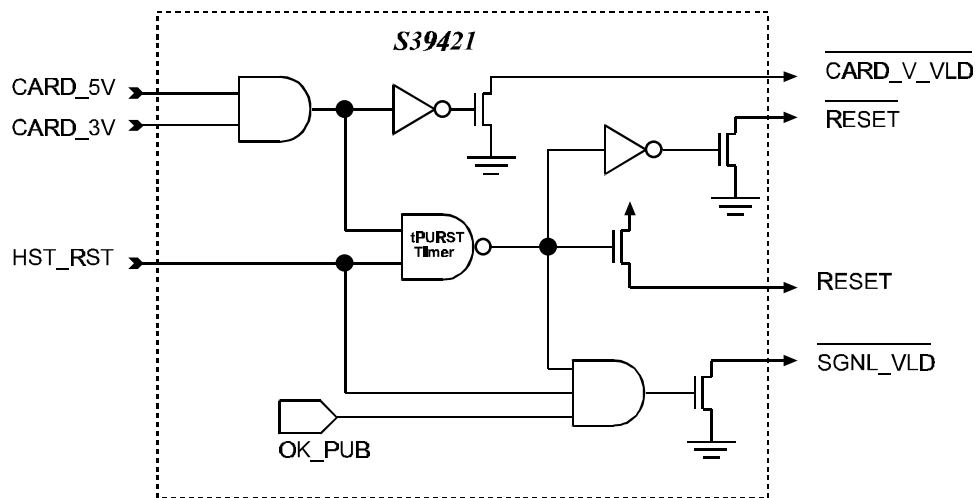


Figure 9. Relationship of reset outputs

So far the discussions have only covered hardware connection control, the basic function of monitoring the insertion process and cleanly powering up the board and finally indicating to the host that the board is **HEALTHY**. These are the minimum requirements for implementing the **Basic Hot Swap** board.

Full Hot Swap boards have the minimum features plus the ability for software connection control. The additional resources needed are:

An **ENUM#** signal, which is an open collector bussed signal.

A switch, actuated with the lower injector handle.

An LED to indicate status of the software connection process.

The **ENUM#** signal indicates a board has been freshly inserted or is about to be extracted. "Full Hot Swap Boards assert **ENUM#** until serviced by the Hot-Plug System Driver." **ENUM#** is activated by a micro-switch located in the lower injector handle.

A blue LED, located on the front of the board, is illuminated when it is permissible to extract the board. During the insertion process the LED is illuminated immediately by the hardware. On the host system the **BD_SEL#** signal has a weak pull-down. As the board is inserted the pull-up, on the board, overrides the pull-down generating a change in state to the host. The host can now respond and activate the power-on circuit driving the **BD_SEL#** signal low. (see figure 10)

The LED will stay on until the host system pulls the **BD_SEL#** signal low and until the board is fully powered-on. At this point the operator may fully close the injector closing the switch that generates the **ENUM#** signal. The **ENUM#** signal will stay active until the host system clears the board's status register.

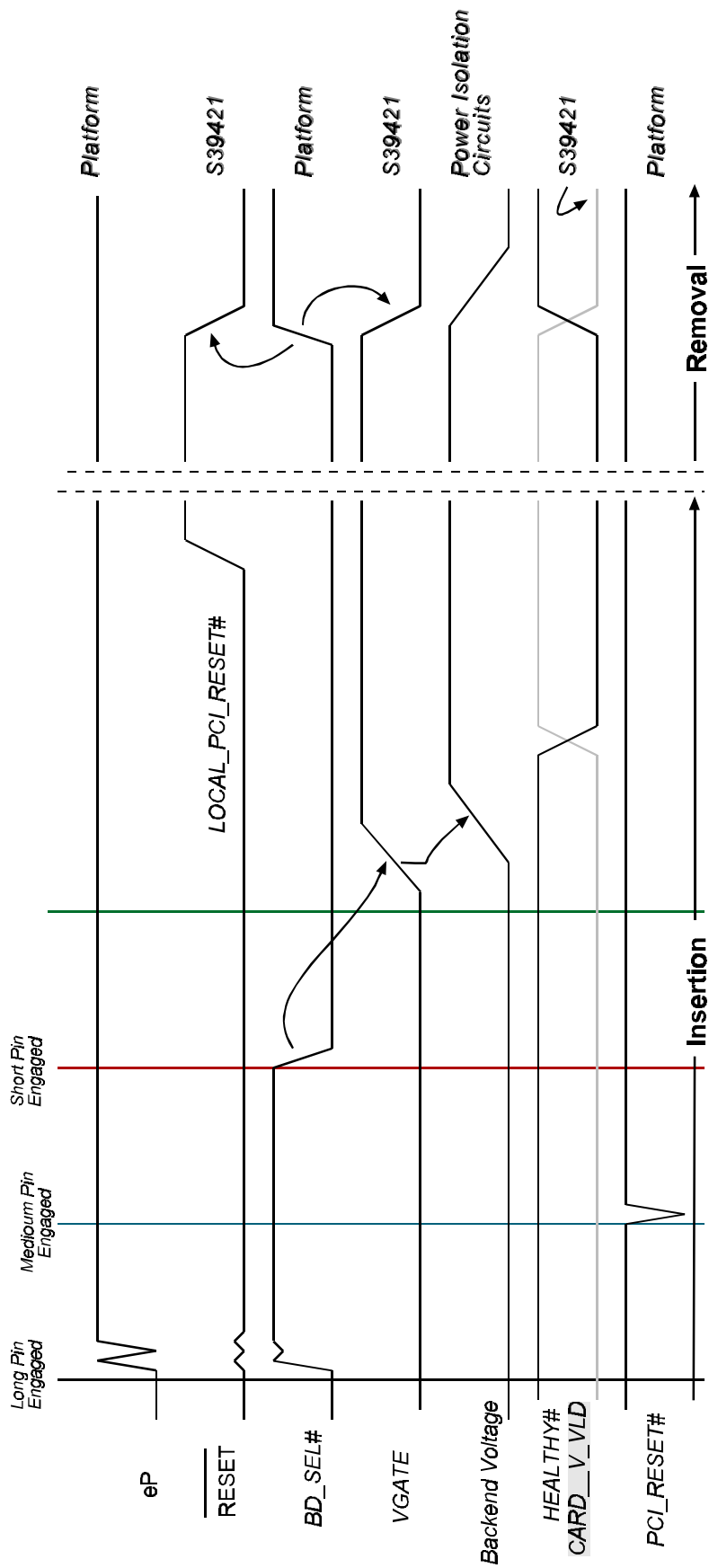


Figure 11. Basic Hot Swap Board Insertion / Removal Sequence

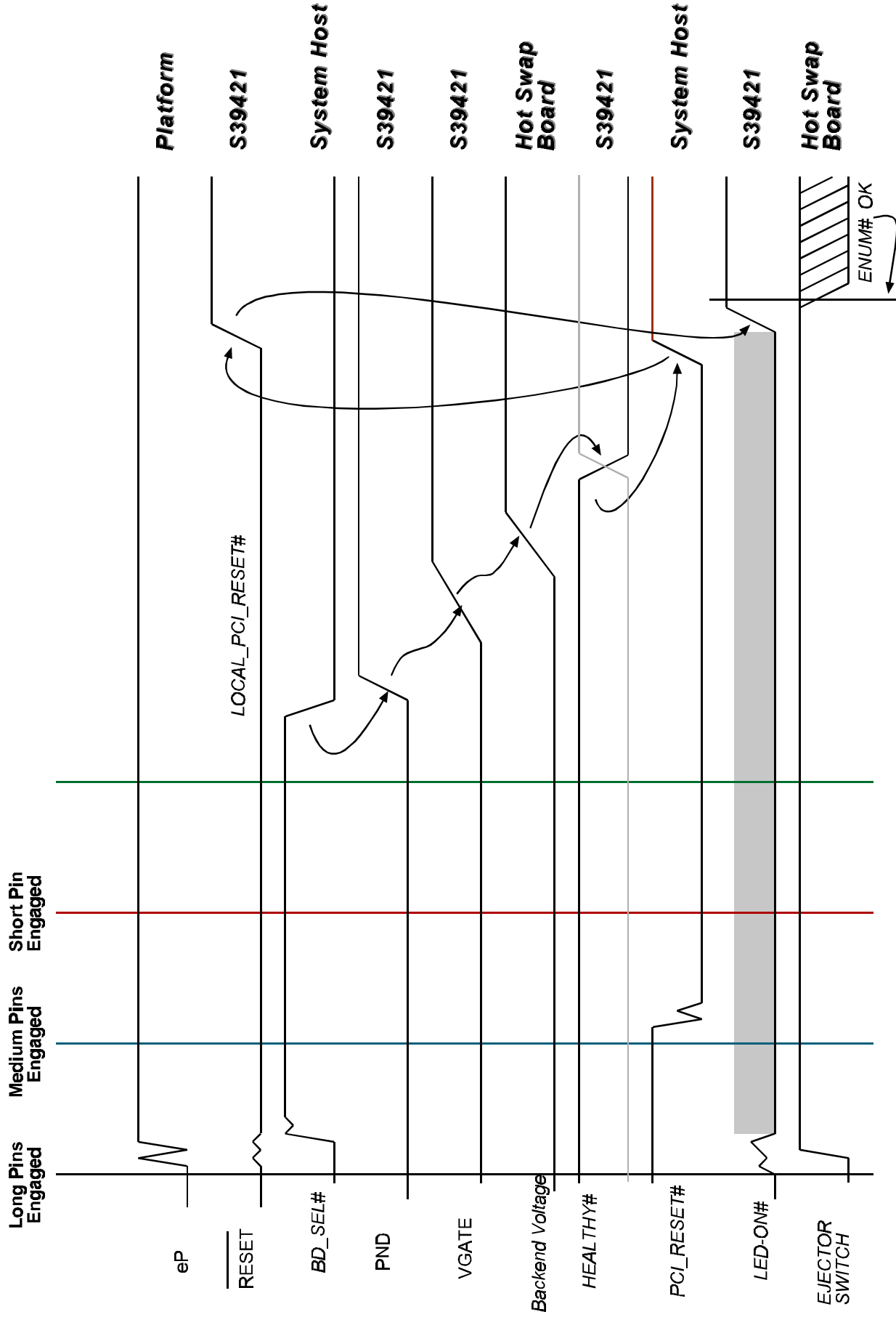


Figure 12. Power-On Sequence for a Full Hot Swap Board Using the S39421

Controller Plus

With the exception of the *ENUM#* signal the S39421 provides all the logic necessary to implement a **Full Hot Swap** board. In addition to all of the power sensing, sequencing and reset control capabilities, the S39421 also has 1K-bit of nonvolatile memory. This is a serial interface memory that is a superset of the industry standard Microwire[™] protocol. That is, any system designed to use the generic 93C46 can interface directly to this memory. However, when possible the designer can take advantage of the memory's proprietary **data download**[™] mode. After power -on either the host MCU or the board's ASIC or MCU can take the DD and CS inputs high and then begin clocking out a serial data stream. The first address to be downloaded will always be 00. Details of the memory operation are covered in the device data sheet.

Conclusion

The S39421 has been shown to easily act as the power control circuit for a **CompactPCI** Hot Swap board. It provides enough flexibility to the designer that they may use the S39421 on either a **Basic Hot Swap** board or **Full Hot Swap** board and then use a minimum amount of support circuitry.

Suggested Power MOSFET Switches for Hot-Swap Controller ICs

N-Channel

Part Number	Manufacturer	V(BR) _{DSS}	R _{DS(on)} @ V _{GS} =10V	I _D cont. @ 25°C	Package
IRF7603	Int. Rectifier	30V	35 milliohms max	4.5A	Micro-8
IRF7413	Int. Rectifier	30V	11 milliohms max	9.2A	SO-8
IRFR110	Int. Rectifier	100V	540 milliohms max	4.3A	DPAK
IRFR120	Int. Rectifier	100V	270 milliohms max	7.7A	DPAK
IRFR120N	Int. Rectifier	100V	210 milliohms max	9.1A	DPAK
MTSF3N03HD	Motorola	30V	40 milliohms max	3A	Micro-8
MMSF7N03HD	Motorola	30V	28 milliohms max	8A	SO-8
MTD20N03HDL2	Motorola	30V	35 milliohms max	20A	DPAK
MTD6N10E	Motorola	100V	400 milliohms max	6A	DPAK
MTD9N10E	Motorola	100V	250 milliohms max	9A	DPAK
Si6434DQ	Vishay Siliconix	30V	28 milliohms max	5.6A	TSSOP-8
Si6410DQ	Vishay Siliconix	30V	14 milliohms max	7.8A	TSSOP-8
Si4412DY	Vishay Siliconix	30V	28 milliohms max	7A	SO-8
Si4416DY	Vishay Siliconix	30V	18 milliohms max	9A	SO-8
Si4482DY	Vishay Siliconix	100V	60 milliohms max	4.6A	SO-8

P-Channel

Part Number	Manufacturer	V(BR) _{DSS}	R _{DS(on)} @ V _{GS} =10V	I _D cont. @ 25°C	Package
IRF7606	Int. Rectifier	-30V	90 milliohms max	2.9A	Micro-8
IRF7416	Int. Rectifier	-30V	20 milliohms max	7.1A	SO-8
MTSF2P03HD	Motorola	-30V	90 milliohms max	2.4A	Micro-8
MMSF3P02HD	Motorola	-20V	75 milliohms max	3A	SO-8
MTD20P03HDL2	Motorola	-30V	99 milliohms max	19A	DPAK
MTD6P10E	Motorola	-100V	660 milliohms max	6A	DPAK
Si6435DQ	Vishay Siliconix	-30V	90 milliohms max	4.5A	TSSOP-8
Si6415DQ	Vishay Siliconix	-30V	19 milliohms max	6.5A	TSSOP-8
Si4431DY	Vishay Siliconix	-30V	40 milliohms max	5.8A	SO-8
Si4435DY	Vishay Siliconix	-30V	20 milliohms max	8A	SO-8

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