

Preventing Data Corruption During Power Failures

Introduction

The loss or corruption of data stored in a nonvolatile memory is the reason that the reset controllers with integrated E²PROM were developed by Summit Microelectronics. These devices insure that an inadvertent write cycle cannot be initiated during the periods of power transitions. This capability has virtually eliminated the possibility of a write cycle occurring during the period of power instability, the devices do not answer the question of what happens if the power failure occurs during the internal write cycle of the device.

Background

Once the more common problem of inadvertent write cycle initiations is eliminated from the application, there is still one more circumstance which could result in improper data stored in the E²PROM. If a power failure should occur during a write cycle that was initiated prior to the power failure, the question arises, what is the final state of the nonvolatile data? Unfortunately, the answer will vary depending upon the internal architecture of the E²PROM, which varies from manufacturer to manufacturer, as well as the decay rate of the supply voltage. Since it is virtually impossible to predict every power supply failure mode and how it will affect the internal operation of the device, the problem has not been left addressed by the suppliers of E²PROM devices.

Solution

Summit has designed a family of microcontroller supervisory circuits that can be used to prevent all issues of data corruption in the serial E²PROM. The devices feature both a VCC sensor to detect when VCC is within tolerance or not as well as a second voltage sensor which can monitor another voltage in the system. In the case of the S4242 device, this second voltage sensor is called V_{SENSE} which is set to sense voltages below 1.25 Volts. Whenever the sense input is below this voltage, an active low open drain output called V_{LOW} is asserted.

The voltage sensor is used to monitor the unregulated DC in the system and the V_{LOW} output is connected to an interrupt on the microcontroller. A resistor divider is used on the V_{SENSE} input to set the desired level of unregulated DC which will correspond to the 1.25 Volt input level. The block diagram of this system implementation is shown in figure 1. The serial interface to the 4K bit E²PROM is an I²C interface utilizing the standard SCL and SDA interface connections to the microcontroller I/O ports.

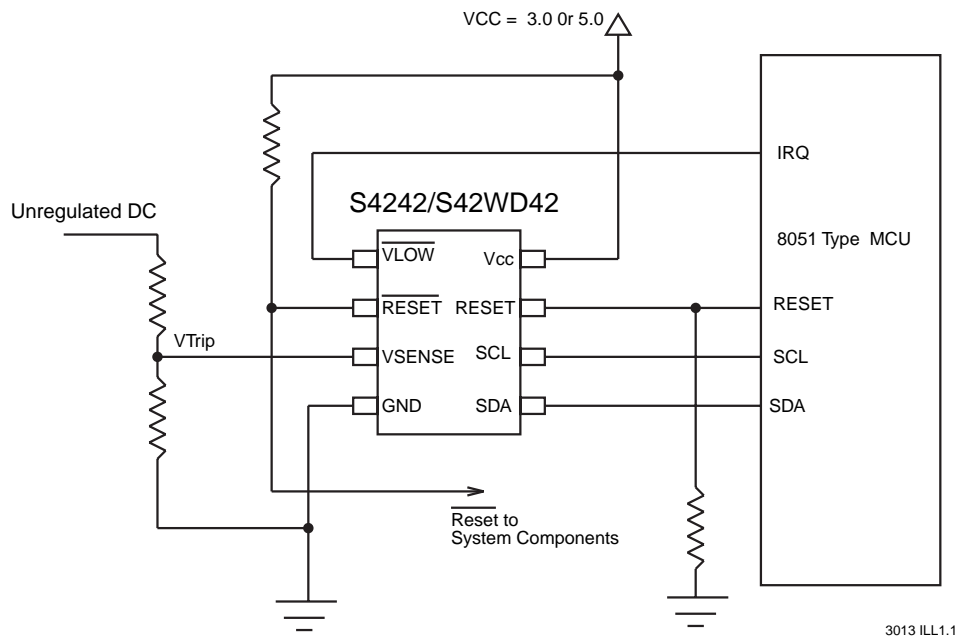


Figure 1: Typical 8051/S4242 Implementation

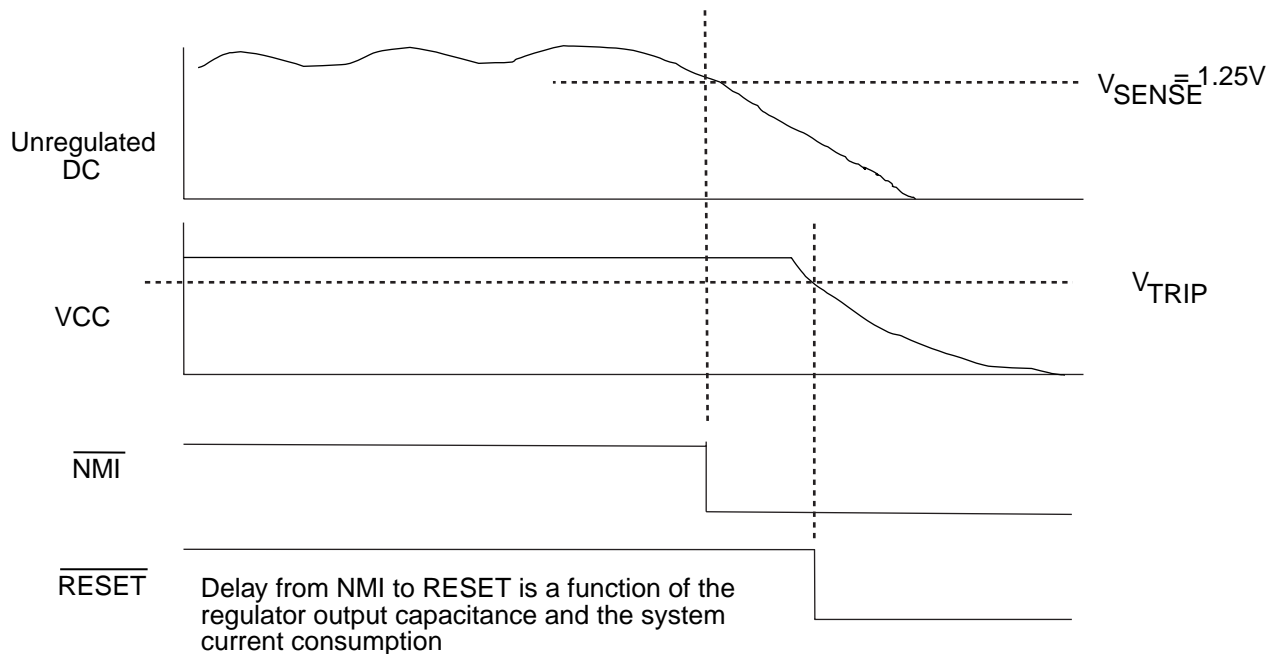


The S4242's VCC sensor monitors the condition of the VCC supply and will generate a RESET to the microcontroller whenever VCC is below a selected voltage, 4.35 volts for example, which will prevent the microcontroller from getting "confused" during a power down situation and generating write operations to the E²PROM. The voltage sensor on the VCC input is also used to disable write operations to the E²PROM whenever VCC is below the selected voltage.

In order to guard against the loss of power during an E²PROM write cycle, the MCU must determine if the unregulated DC is still in spec, which can be sensed by the status of the VLOW signal. The interrupt service routine for this sets a flag to tell the MCU that power is failing in the system. The subroutine which performs a write to the E²PROM will always check the status of this flag prior to the initiation of a write cycle.

Care must be taken to design the output stage of the regulator to insure that the fall time of the system VCC from the normal operation range to the trip point of the S4242 VCC sensor is longer than 10 ms after the power failure level of the unregulated DC is reached. This will insure that any write cycles which are initiated while the unregulated DC is within tolerance will be completed before the system enters the reset state. The maximum write cycle time for the Summit E²PROMs is 10 ms, although the typical value is closer to 5 ms. Therefore, the power down routine must add in the write operation interface period and any other routines which will be executed between the querying of the power status flag and the stop bit of the write instruction to the serial E²PROM. Figure 2 shows the timing diagram for this implementation.

Another benefit of this implementation is that the VLOW interrupt can actually be used to warn the micro of impending power failure. At this time, the micro can perform important housekeeping functions including the updating of system parameters in the S4242's E²PROM data storage so that when power returns to the system, the system will know the status when the power failure occurred.



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Figure 2: Sequence of Voltages Dropping and the S4242 Signal Response to the System