SUMMIT MICROELECTRONICS

Application Note 71

Design and Manufacturing with Summit Microelectronic's WLCSP Products

Introduction

Per the IPC/JEDEC J-STD-012 definition, a CSP is a single-die, direct surface mountable package with an area of no more than 1.2 times the original die area. Wafer Level Chip Scale Packages (WLCSP) refers to the technology of packaging an integrated circuit at wafer level instead of the traditional process of assembling the package of each individual unit after wafer dicing. WLCSP is a true chip-scale packaging (CSP) technology since the resulting package is essentially the same size as the die. Summit's WLCSP parts are ROHS6 compliant and are certified as MSL-1.

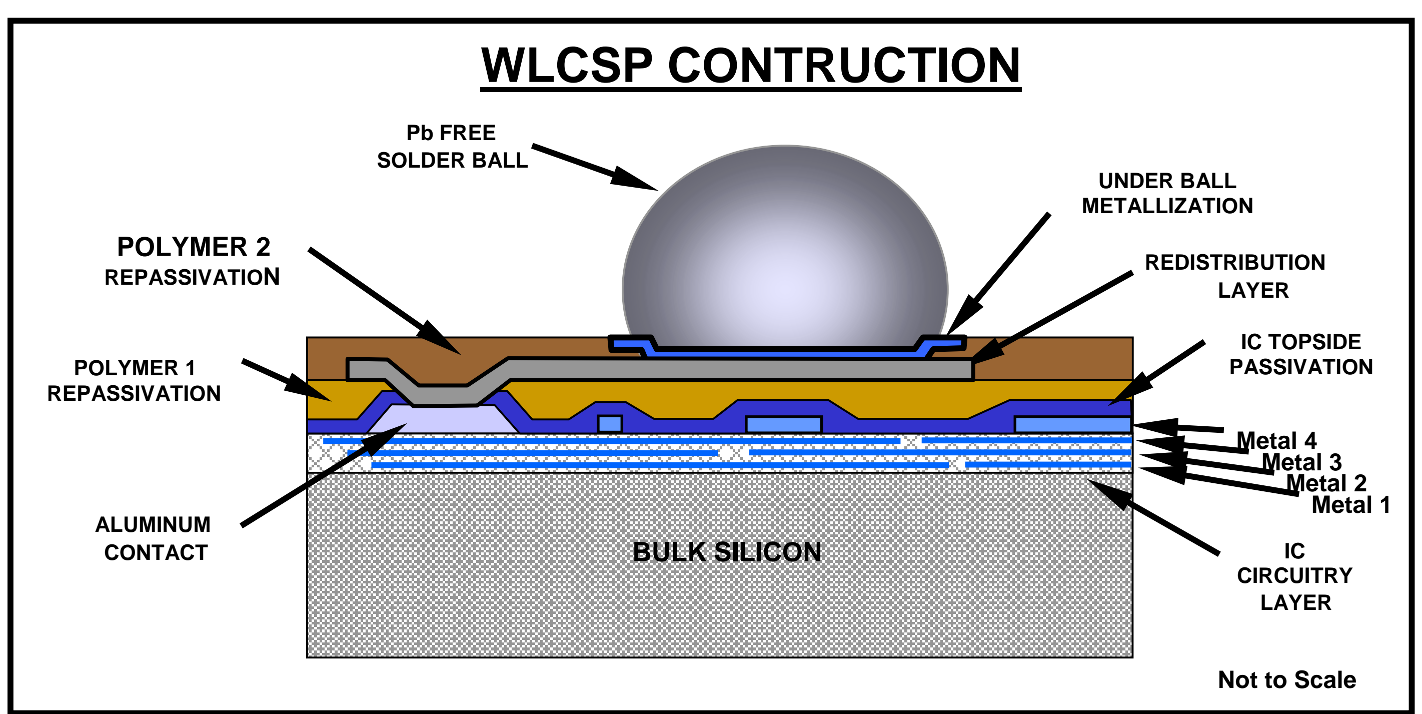
Purpose

This application note is intended to provide a recommended starting point for product design and manufacturing process optimization using Summit WLCSP components. The suggestions published here have been proven to work under the given conditions, but variances in manufacturing equipment, processes and circuit board design for a specific application may lead to a condition where other process parameters yield superior performance.

Summit utilizes the Redistribution Layer and Bump technology, which is the most widely-used WLP technology. It extends the conventional wafer fab process with additional steps that deposit a multi-layer thin-film metal rerouting and interconnection system to each individual device on the wafer. This is achieved using the same standard photolithography and thin film deposition techniques employed in wafer fabrication.

The addition of a redistribution interconnection layer (RDL) within a polymer repassivation redistributes the bonding or contact pads of each chip to an area array of under-ball metal (UBM) pads that are deployed over the chip's surface. The solder balls used in connecting the device to the application circuit board are subsequently placed over these UBM pads and attached with a reflow process.

Aside from providing the WLP's means of external connection, this redistribution and technique also improves chip reliability by allowing the use of larger and more robust balls for interconnection, provides for better thermal management, and improves the electrical performance of the device's I/O system by reducing inductance and ohmic resistance.



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Susceptibility to Mechanical Over Stress

Because of the properties of silicon and the other materials used in IC circuitry, WLCSPs are brittle and subject to Mechanical Over Stress (MOS) damage when not handled and assembled properly. Unlike conventionally packaged parts, WLCSPs may be rendered nonfunctional or unreliable by even moderate mechanical over stress damage. The three primary detrimental mechanical stresses are compressive, flexural, and impact. Care must be taken in design, handling, and manufacturing to ensure that WLCSPs are adequately protected against impacts and mechanical stresses.

Force Moments	Potential Sources	Prevention / Mitigation
Compressive	• Mishandling in Tape • Excessive Placement Force • Mishandling after SMT	• Observe proper handling protocols • Optimization of SMT Process • Underfill • Backside Laminate Coating
Flexural	• Board Flexing following SMT • Excessive CTE Mismatch • Drop and Vibration Forces	• Observe proper handling protocols • Optimize Fixturing • Underfill • Backside Laminate Coating
Impact	• Mishandling in Tape • Pick & Place Process errors • Mishandling after SMT	• Observe proper handling protocols • Underfill • Backside Laminate Coating

Primary Failure Modes

Silicon Cracks – The body of the WLCSP is comprised of silicon, a crystalline lattice, glass-like material. Cracks or crack initiation sites, once established will propagate when subjected to sustained or repeated stresses. If the force is great enough or the exposure to force long enough in duration catastrophic failure and fracture will occur. Most often this will damage the circuit area resulting of a partial or complete loss of chip functionality (See Figure 1 and Figure 2).

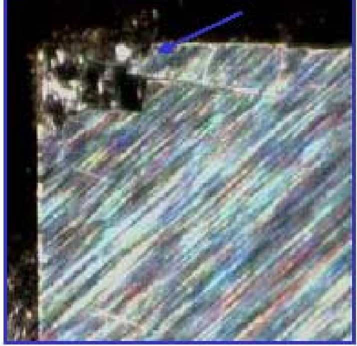


Figure 1: Gross Crack

Figure 2: Gross Crack

Primary Failure Modes (cont.)

Circuitry Damage – The circuitry on an IC resides in a layer on the underside of the chip. This layer is only a few tens of microns thick. It is comprised of deposited areas of dopants, glass like oxide insulations, aluminum interconnects and nitride passivation layer intended as a moisture and contamination barrier. Although some level of physical protection is provided by the repassivation layers and the solder balls, this area is vulnerable to contact and impact pressure that can alter the critical dimensions of the chip, break the internal aluminum interconnects or create short circuits. Similar damage may be inflicted within the circuit layer by exposure to tensile, compressive or flexural mechanical overstresses. Unlike impact or contact damage and cracks, these failure mechanisms may not be visible without costly chip de-processing and SEM or high magnification examination (See Figure 3 and Figure 4).

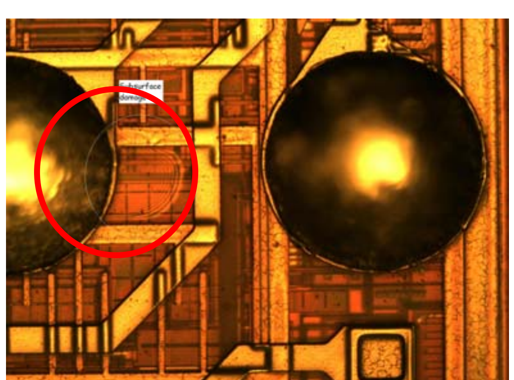


Figure 3: Micro-cracks

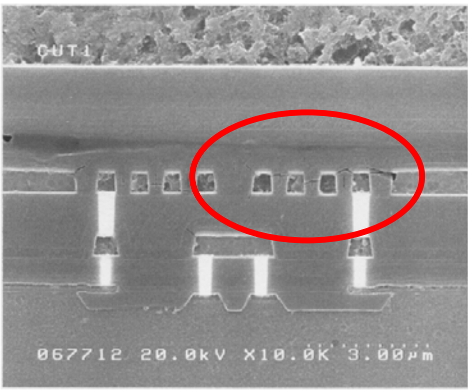


Figure 4: Micro-cracks

Metallization System Failure – The most common and understood failure mechanism in CSPs is a failure within the solder ball-to-chip circuitry interconnect system. These are manifested in three primary ways:

Intermetallic Formation: An intermetallic is an alloy of two metals in which a progressive change in composition is accompanied by a progression of phases, differing in crystal structure. Intermetallic formation at both the ball to UBM and ball to PCB interfaces is a natural consequence of the materials and processes used, and is essential for good mechanical and electrical contact. Once initiated, intermetallics will continue to propagate until one or both of the available metals are consumed. The activation energies of intermetallic growth for the soldering systems used are well known and have shown to be reliable over the normal life and use conditions of Summit's ICs. However, when subjected to excessive heat intermetallics may become brittle and resistive resulting in both continuity and structural failure.

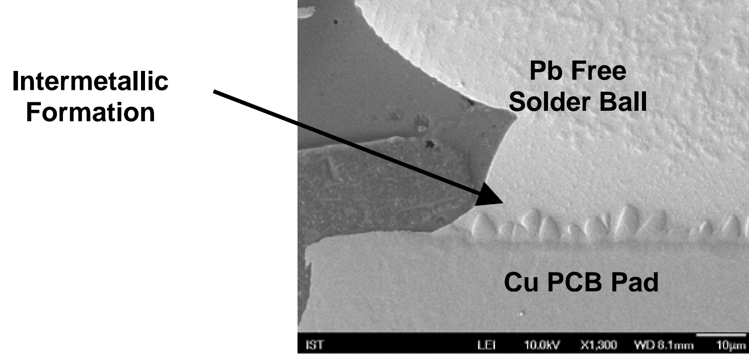


Figure 5: Intermetallic Formation

Excessive G forces: Often characterized as “Drop Test Failures”, the IC and its interconnect system can be damaged when exposed to shock or G forces in excess of the material strength of any of its load bearing elements. These failures are typically event based. Mechanical force moments are concentrated at the interface of the ball to the IC and the ball to the PCB and can result in a fracture or separation of the ball to UBM or UBM to IC interface resulting intermittent or continuity failures.

Fatigue Failures: Fatigue is a mechanical phenomenon in which a material is weakened through cyclic loading. The fatigue properties of the materials used in the interconnect systems are well understood and have been selected to provide sufficient product life and reliability when used as intended. Fatigue forces are introduced through the differential expansion and contraction of the various materials resulting from CTE (Coefficient of Thermal Expansion) mismatches and vibrational forces.

Design Considerations

Mechanical damage to WLCSPs can be catastrophic and is difficult to detect. The most effective approach is to prevent systemic or design related overstresses and to control or eliminate process and handling overstress events. Proper system design must consider the anticipated environment that the product will be exposed to during manufacturing and distribution and in which the device will operate in over its expected life. Maximum exposures to temperature excursions, temperature extremes, flexural stresses between the device and the PCB, mechanical shock and vibration and incidental contact and impact must be anticipated and prevented or mitigated.

PCB: PCB design requirements should be based on IPC-A-600 and IPC-6012A standards.

CTE mismatch must be accounted for at the most extreme temperature exposures anticipated. As a general rule higher Tg (Glass Transition Temperature) associated with high-performance FR4, FR5 or BT laminate (Tg = 170°C to 185°C) is recommended for Pb-Free solder reflow profiles with peak temperatures above 240°C. IPC-4101B “Specification for Base Materials for Rigid and Multilayer Printed Boards” contains further information on choosing the correct PCB material for the intended application.

Electroless Nickel Immersion Gold (ENIG) is the preferred plating for the PCB copper land pads surface finish (minimum 3 µin. /maximum 20 µin. Au over a minimum 100 µin. /maximum 300 µin. Ni) for all Summit solder bump alloys. Organic Surface Protective (OSP) coating over copper land pads is also acceptable.

Non-Solder-Mask Defined (NSMD) land pads are preferred over Solder-Mask Defined (SMD) pads for WLCSPs because of their better dimensional control, but either may be used successfully. Pad sizes should normally be 20% to 25% less than the solder bump maximum diameter to enable the desired package standoff height. Solder mask is recommended between all pads, with solder mask design clearance to pads of 0.002in to 0.003in.

Via-in-pad should be avoided as it is known to cause incomplete soldering and continuity problems as solder is wicked into the via, away from the desired solder joint. Large voids and blow outs in the solder joints are also a consequence of via-in-pad. Flux and other volatiles can become trapped in the via and cause it to form voids in the solder ball. To prevent this, the vias should be plated (capped) until the dimple is completely shut or the via should be filled with a conductive epoxy prior to final plating of the board to cover the hole so the surface appears as a flat pad. However, these methods are process adders in the board fabrication.

Land patterns may be either circular or square. Pads and connecting traces should be arranged symmetrically to prevent off-center wetting forces during solder reflow. To prevent solder thieving, each NSMD copper pad should be connected by only one signal trace, the trace width being no more than 1/2 the diameter of its connected NSMD copper pad. The trace should have a fillet radius at the point it meets the pad, this is also known as “tear dropping”. This prevents the stress riser that would otherwise occur at the pad to trace intersection.

Component locations should be considered to ensure that WLCSPs are not placed in locations susceptible to manufacturing and handling flexing and impact damage. Thermal mass considerations of neighboring components should be considered to ensure that WLCSPs are exposed to an appropriate reflow profile.

Solder: A variety of SAC (SnAgCu – Tin, Silver, Copper) Pb-free solder alloys are available. Although compositional and manufacturing differences are minor Summit recommends customers consider their end application when selecting their solder ball composition.

MATERIAL PROPERTY	SAC405	SAC305	SAC266	SAC105
Sn	95.5%	96.5%	96.8%	98.5%
Ag	4.0%	3.0%	2.6%	1.0%
Cu	0.5%	0.5%	0.6%	0.5%
Liquidous (Melting) point	217ºC	218ºC	220ºC	226ºC
Stress - σ_n (MPa)	107.6	102.0	93.45	76.3
Shear - σ_s (MPa)	44.16	44.44	33.67	28.53
Equivalent Plastic Strain - ξ_p (%)	6.831	7.577	8.265	11.075
Elastic Modulus (Gpa)	53	57	50	46
Ultimate Tensile Strength	53	40	35	27
Yield Stress (MPa)	26	34	28	24
Drop test Performance	-	-	Baseline	+
Temp Cycle Performance	+	-	Baseline	-

Backside Laminate Coating: Backside Laminate Coating, a 40μm thick opaque laminate protective polymer film, is available for all Summit WLCSP products. This film has been shown to increase die strength, reduce chip-outs during saw, and improve marking legibility. It is recommended for applications in which more severe handling and manufacturing stresses are anticipated.

Assembly Considerations

Handling: As described above WLCSPs are more unforgiving of mishandling and processing related Mechanical Over Stress as conventional molded chip and wire packages. Care must be exercised throughout the transportation, inventory, staging, and manufacturing operations to ensure that the parts are not damaged. Experience has shown that all persons involved and associated with material handling and manufacturing should be trained in the proper methods and techniques of handling WLCSPs to avoid incidental damage.

All semiconductor devices, whether packaged or unpackaged, may be inadvertently damaged by static discharges. These charges can build up on any insulating surface, including the operator's hair and clothing and are measured in tens of thousands of volts.

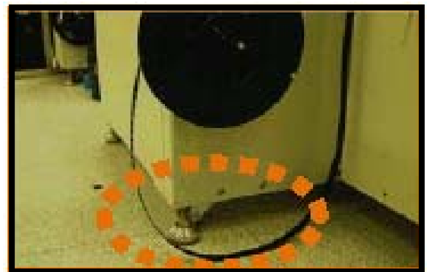
Just touching any of the connections on an grounded component can induce tunneling defects in the internal dielectric layers. The best way to avoid this is to ensure that all operators, tools and equipment are suitably grounded, before any contact is made.

ICs are also vulnerable to oxidation, contamination and mechanical damage. Boxes, Moisture Barrier Bags and Reels should only be opened and handled and approved work stations. Loose units outside of their original carrier tape packing should be considered compromised and should be scrapped.

The original packing materials have been selected to provide adequate protection to the WLCSP units through a normal distribution and manufacturing process. Repacking of Summit's products onto other reel sizes or into other immediate containers without Summit's approval is not recommended and can potentially void Summit's product warranty.

Summit's factory packing does not protect the WLCSPs from damage in extreme or excessive cases. Boxes and reels should not be dropped, impacted or exposed to crushing forces.

Care must be taken when unreeling the tape to prevent bending and impact the carrier tape with hard or moving surfaces.



Tape should not be allowed to twist or bend such that the carrier or cover tape is distorted or deform or that the cover tape separates Partial reels should always have a leader of a minimum of 50 cm of empty pockets to provide protection to the remaining ICs from crushing forces and from lateral contact to the cover tape.

SMT Considerations

Solder Paste Type: Type 3 and Type 4 pastes are commonly used to mount 0.4 mm pitch components. Type 4 paste provides the most consistent prints. Type 3 paste has larger solder spheres and therefore results in less consistent printing results. A solder paste type should be selected that is compatible with both the solder ball alloy of the WLCSP and the reflow process to be used. Summit recommends a low halide or halide-free No-clean paste for elimination of post assembly cleaning process.

Stencil Technology and Aperture Dimensions: IPC-7525 Guidelines for Stencil Design. For a 0.4 mm pitch WLCSP, Summit recommends that the end user use a 100 micron thick stencil. Laser defined apertures or electroformed stencils provide the crispest printing results. Square stencil apertures provide the most consistent paste transfer and should be about 230 to 280 microns wide.

Stencil Cleaning Frequency: Fine pitch paste printing requires increased stencil cleaning frequency. Since cleaning the stencil decreases the productivity of the paste printing process, characterization of the process is required to optimize the cleaning frequency. Cleaning frequency is usually once every 1 to 5 prints. Frequent stencil cleaning is common at fine pitches. If the stencil cleaning is too infrequent, then shorting could occur or insufficient solder paste may be deposited.

Stencil Alignment: The recommended stencil alignment accuracy for 0.4 mm pitch printing is +/-50 microns @ 3 sigma.

Pick and Place:

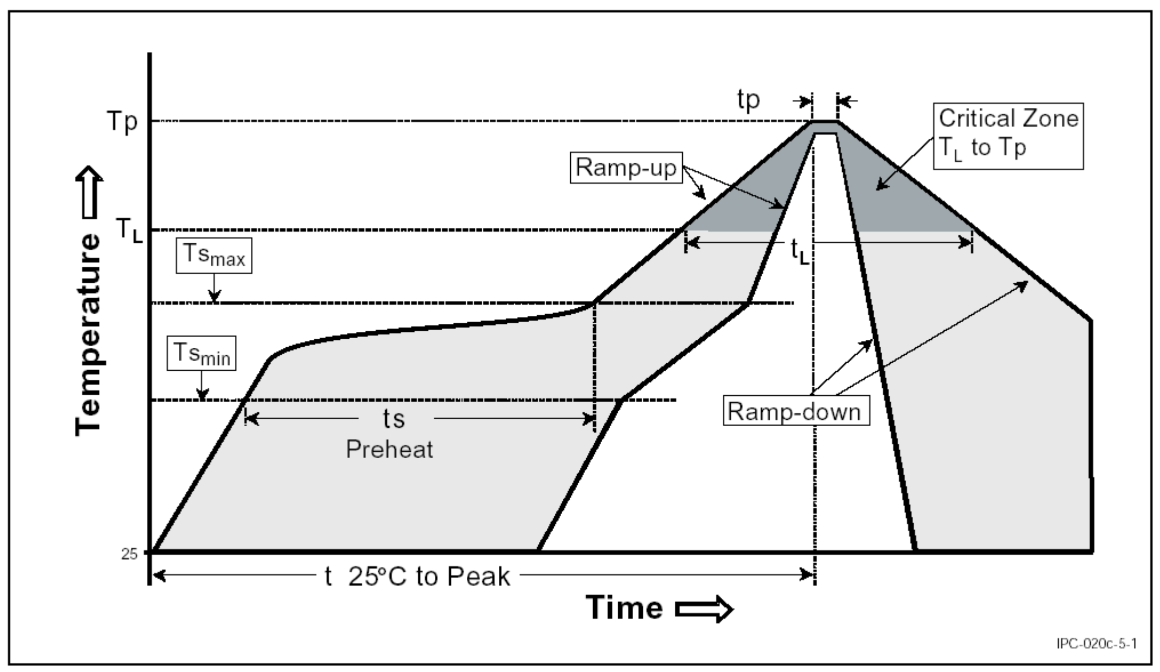
Standard surface mount placement equipment can routinely place 0.5 and 0.4 mm WLCSPs at high speeds and yields. WLCSPs like most other array packages provide robust self-alignment, and will re-center even with substantial component misregistration. A non-metallic pickup nozzle is also recommended to avoid die backside damage and to mitigate force concentration moments associated with skewed or non-coplanar pick up nozzles.

The maximum recommended placement force for WLCSPs is 35 grams/bump, inclusive of the inertial impact spike associated with high speed placement systems. Exceeding this force level can result in backside, interconnect, and circuitry damage which can impact mounted component functionality and reliability. It is recommended that bumps be immersed into the solder paste on the PCB to greater than 20% of deposited paste thickness. When using height

controlled placement the natural variation of the PCB thickness should be taken into consideration.

Reflow Profile

260ºC Lead (Pb) Free Suggested Reflow Profile per JEDEC J-STD-020



Profile Feature	IR - Infra Red Reflow
Average Ramp-Up rate from 200°C to (+0°C/-5°C)	3°C / sec. max.
Preheat 150°C to 200°C (+/-25°C)	60 to 180 sec.
Time maintained above 217°C (critical zone)	60 to 150 sec.
Peak temperature - T_p	260°C (+0°C/-5°C)
Time within 5°C of T_p	20 to 40 sec.
Average Ramp-Down rate	6°C / sec max.
Time 25°C to T_p	8 minutes max.

Underfill: Although underfilling SMT components including WLCSPs is often considered to be undesirable due to the added process complexity and cost it has been demonstrated to be beneficial in board level reliability testing including thermal cycling, drop testing and board bending performance.

As a result, underfills have been effectively used to improve solder joint reliability and enhance WLCSP board level reliability in the impact conditions associated with mobile electronics and a number of applications demanding high reliability including medical, automotive, industrial and military electronics. The decision to use and the selection of a specific underfill should be carefully considered and their effectiveness evaluated by the customer.

Packing: The WLCSP devices used in high volume SMT applications are generally supplied in 8 mm or 12 mm wide pocket tape with a peel-able heat or pressure activated cover tape, in accordance with Standard EIA/IS-763.

WLCSPs are oriented in the pocket of the carrier tape in a bumps-down orientation in order to facilitate pick-up by the component placement equipment. The carrier tape is designed so that the component theta rotation in the pocket is less than ±5° and has less than 0.3 mm of lateral movement in both the X and Y directions.

Rework of WLCSP:

Summit recommends that rework be performed using a controlled and qualified process that prevent contamination, thermal, mechanical and ESD damage to the device, the PCB and the surrounding components. Focused infrared technology is preferred for WLCSP rework over traditional hot gas BGA rework systems. Focused IR allows for pin-point accuracy, reflow, removal, and replacement of even the smallest CSP on a high-density circuit assembly without adjacent component contact heating.

If removed devices are to be returned for analysis Summit requires these devices to be cleaned and preserved within a packing method that does not introduce mechanical damage or contamination. Acceptable methods include using GelPaks (http://www.gelpak.com) or placing units inside the original carrier and cover tape.

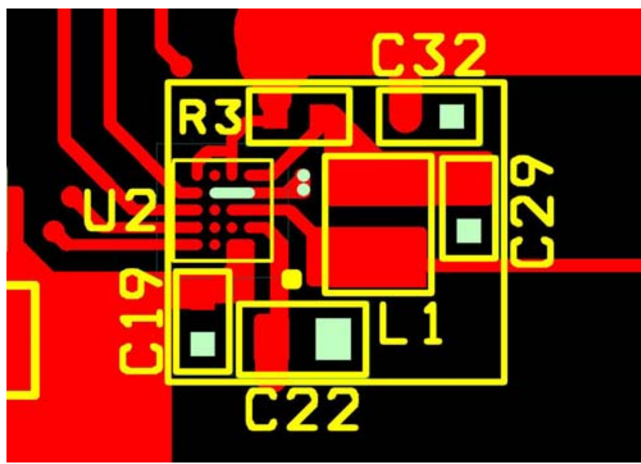


Figure 6: Example of CSP Layout

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