

Four Channel Programmable DC-DC Power Manager Windows GUI Users Guide and Configuration Register Descriptions

Introduction

The information contained in Application Note 62 details the Configuration Register settings for the SMB113A four-channel PWM DC-DC power manager. The SMB113A Windows Graphical User Interface (GUI) is also shown with the associated registers and functions highlighted. For additional explanation on device functionality related to the configuration registers, refer to the SMB113A Data Sheet.

Note: This application note also applies on the SMB113B and SMB117, four-channel programmable DC-DC power managers.

Register Formats and Functions

The SMB113A internally maps into 256 register fields that divide into four different categories: 96 bytes of general-purpose EEPROM memory, 64 bytes of non-volatile configuration registers, 80 bytes of non-volatile reserved registers, and 16 bytes of software enabled volatile registers. All memory locations are accessed via the I²C interface, which responds to a programmable slave address (SA[3:0]=C_17[3:0]) and a programmable bus address (BA[2:0]=C17[6:4]).

General Purpose EEPROM:

The register space between 0xA0 and 0xFF (inclusive) consists of 96 bytes of general-purpose EEPROM

memory (Figure 1). This space is subdivided into two blocks: general-purpose memory block 0 (0xA0–0xBF) and general-purpose memory block 1 (0xC0–0xFF). The memory may be written in byte mode or page mode (16 bytes). A sequential read within the general-purpose memory space will cycle through the entire array contiguously.

Array-Based Configuration Registers:

The non-volatile configuration register content is stored in the array. Upon initial power-up, those locations from the array are read out into volatile registers on the chip. The output of these registers determines the configuration of the device. When data is written into the configuration space, that data is written directly into the memory array. At the conclusion of the internal write cycle, another readout will occur so that information may be transferred from the array into its volatile register location.

Volatile Registers:

The register space between 0x8F and 0x9F consists of volatile registers. These registers are used to commence sequencing, enable and disable channels and read the status of individual channels.

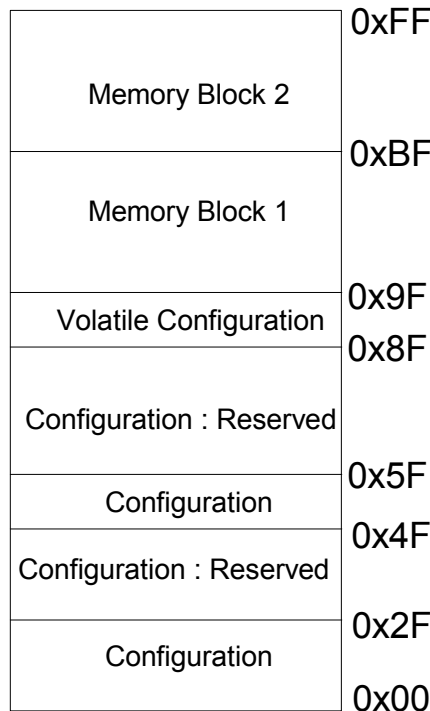


Figure 1: Memory map of the SMB113A displaying volatile/non-volatile configuration registers and general-purpose memory



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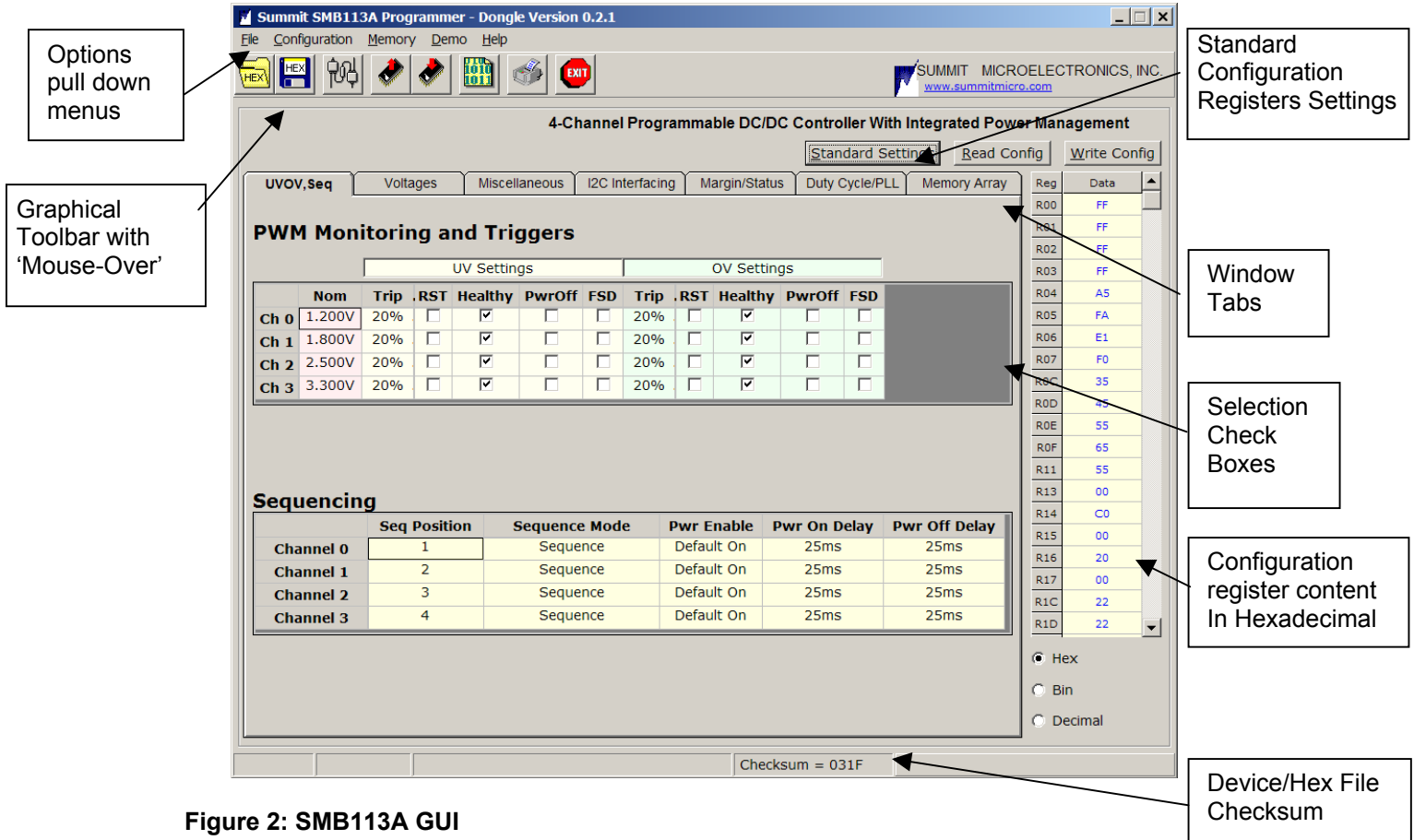


Figure 2: SMB113A GUI

SMB113A Windows Graphical User Interface

The SMB113A Windows GUI (Figure 2) is used with the SMX3200 programming 'Dongle'. It is an easy to use Graphical Interface that is compatible with Windows 9X, NT, 2000 and XP operating systems. The GUI consists of pull-down menus, check boxes, up/down buttons, etc. The GUI generates a checksum that can compare the programmed device configuration register values versus the hex contents.

Help

The Help menu can be used to view the SMB113A Datasheet or this app note while prototyping with the Windows GUI. The 'About' selection will show the GUI version number, which is also displayed in the upper left hand corner of the GUI. It is advised that the user periodically visit the Summit web site (www.summitmicro.com) to check for the most current data sheet and GUI software.

Demo

To help familiarize the user with the SMB113A a systematic tutorial will guide the user through the extensive feature set. The Demo demonstrates the power on/off sequencing, independent channel

enable, Input voltage monitoring and dynamic voltage control capabilities of the SMB113A.

Memory

The SMB113A is equipped with 96 bytes of user programmable non-volatile EEPROM memory. From the Memory options, pull down menu the memory can be accessed and modified in one of several modes. When a selection is chosen from the memory pull down menu the memory tab will automatically be selected on the GUI. The user can view the memory contents in either a graphical or a tabular form. The contents of the memory can be read by a memory dump or read. The memory can be written to as either a single byte or a page (16 bytes). The memory is separated into two separate 48 byte sections each of which may be independently locked to protect memory content.

Configuration:

The configuration pull down menu can be used to read from or write to the configuration registers on the SMB113A. In addition, the configuration menu is used to check for an acknowledge from the addressed device over the I²C bus or create a detailed description of all registers and their contents. When performing an



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I²C read or Write operation it is necessary for power to be applied before the command is issued.

File

The file menu is used to open a file, save a file, modify the system settings, or exit the program. When a file is saved the contents of the configuration registers is saved in a hexadecimal format, likewise when a file is opened the configuration registers are loaded with the

contents of the file. After opening a file it is necessary for the user to perform a write operation to store the contents into the configuration registers. Additional options in the file menu allow I²C parameters to be accessed and modified. Features that may be modified include an automatic read after write option, I²C read and write speed and direct register access mode.

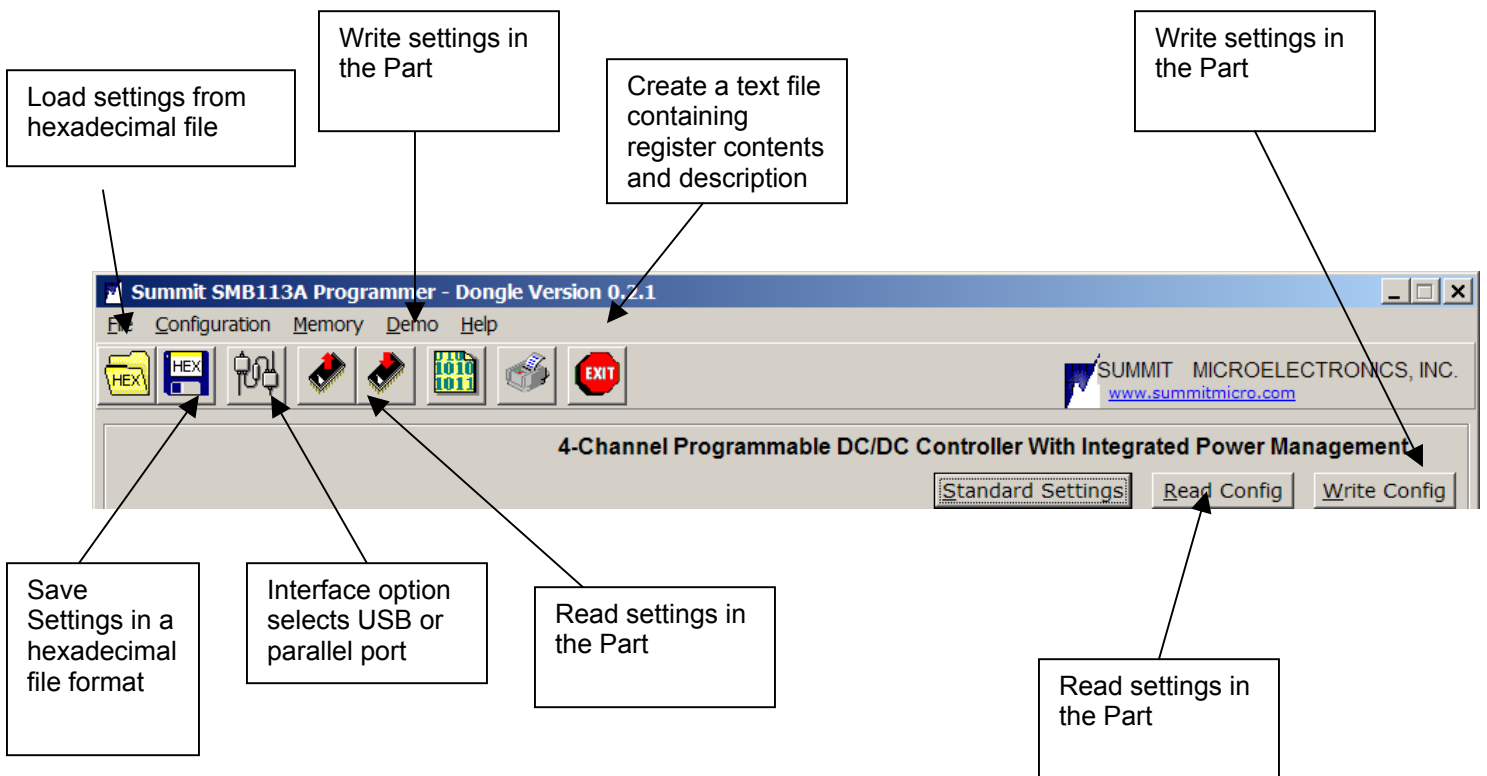


Figure 3: SMB113A Graphical toolbar and pull down menu.



UV/OV Sequencing:

DESCRIPTION REGISTER

UV Trip Level	R[20:23]
UV Glitch Filter	R[20:23]
UV Healthy	R[1C:1F]
UV Power Off	R[1C:1F]
UV Force SD	R[1C:1F]
OV Trip Level	R[20:23]
OV Glitch Filter	R[20:23]
OV Healthy	R[1C:1F]
OV Power Off	R[1C:1F]
OV Force SD	R[1C:1F]

Sequence Position	R[C:F]
Sequence Mode	R[11]
Power Enable	R[13]
Power On Delay	R[C:F]
Power Off Delay	R[C:F]

Voltages:

Nominal Ref	R[4:7]
Margin Hi Ref	R[5C:5F]
Margin Lo Ref	R[54:57]
R Divider	R[30:31]

Miscellaneous Settings:

UV1 Trip Point	R28
UV1 Force Shut Down	R14
UV1 Power Off	R14
UV1 Healthy	R2D
UV1 FS Latched	R14

UV1 Power Off Latched	R14
UV2 Trip Point	R28
UV2 Force Shut Down	R14
UV2 Power Off	R14
UV2 Healthy	R2D
UV2 FS Latched	R14
UV2 Power Off Latched	R14
Last Sequence Position Used	R14
Sequence Termination Timer	R2A
Reset Timer	R2A
Ref Slew Rate Control	R15
Reset Triggers Healthy	R2D
Wait for I ² C Power On Command	R14
Power On/Off Command	R91
Clear UV1	R91

I²C Interfacing:

Programmable Slave Address	R17
Programmable Bus Address	R17
Configuration Registers Lock	R16

Margin/Status:

I ² C Power Enable	R90
Status Register	R[98:99]
Margin Command	R[9C:9D]

EE Memory Array:

Lock EE Memory Block 0	R16
Lock EE Memory Block 1	R16



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Registers 0x00 through 0x04 control the non-overlap delay (dead time) of the n-channel and p-channel MOSFETS. The dead times described below refer to the HSRDV and LSDRV states. Registers 0x00 to 0x04 correspond to channels 0 through three respectively. In the default mode, the contents of registers 0x04 through 0x07 are hidden from the user unless the expert mode is selected. To set the desired

output voltage the user enters the desired output voltage in the *Output Voltage* box, by double clicking on the box typing in the value and pressing enter. Once the desired output voltage has been entered, the reference voltage is automatically calculated and loaded into the corresponding register. A write operation must then be performed to change the output voltage.

Registers 00, 01, 02, and 03 (HIDDEN REGISTER)								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
0	0	0	0	X	X	X	X	Minimum falling edge dead time
1	1	1	1	X	X	X	X	Maximum falling edge dead time
X	X	X	X	0	0	0	0	Minimum rising edge dead time
X	X	X	X	1	1	1	1	Maximum rising edge dead time

Table 1: Dead time control registers. This register is not displayed in the GUI.

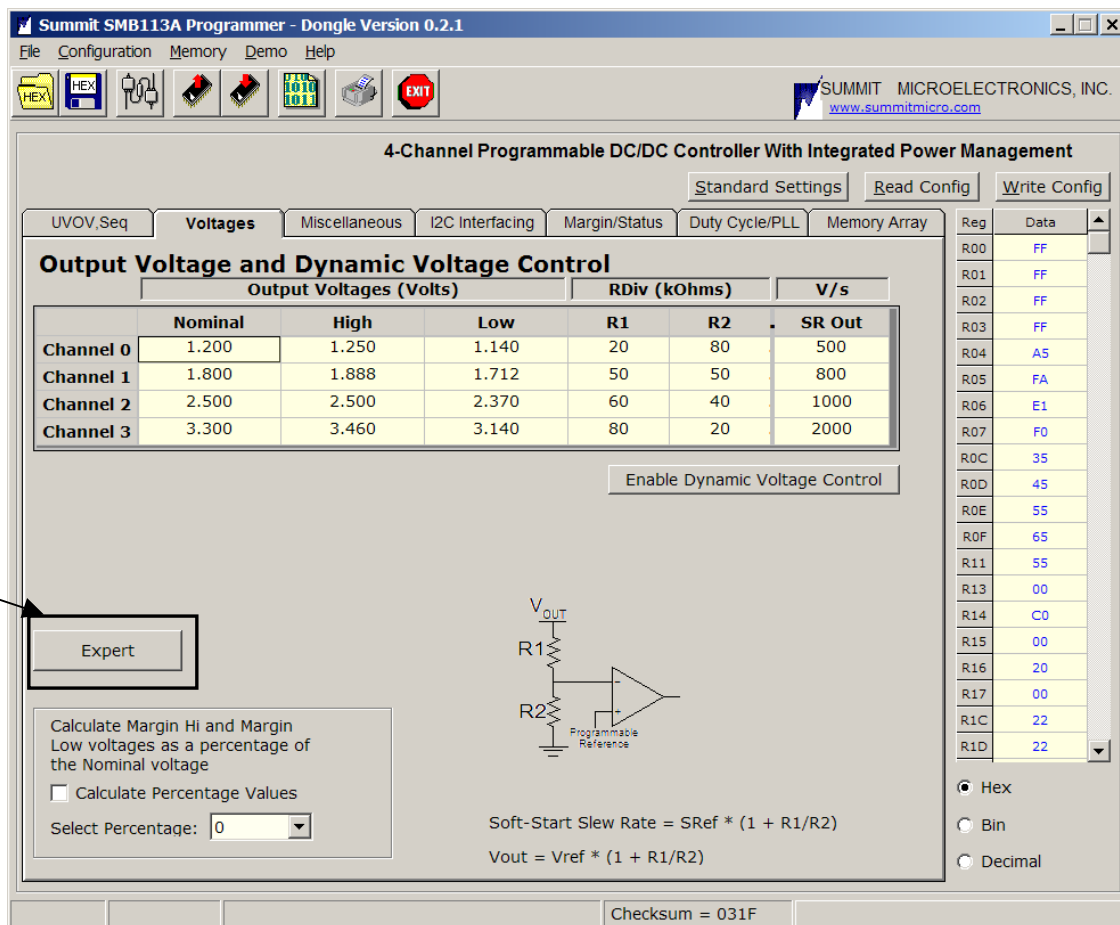


Figure 4: The default settings allow the user to enter the output voltage settings without specifying a reference voltage

When expert mode is selected, Registers 0x04 through 0x07 can be modified from the GUI. These registers set the output voltage on the COMP1_ChX

feedback pin of the SMB113A. The Voltage range is programmable from 0 -1.0V in 4 mV increments for channels 0-3. R04 corresponds to Channel 3 and R07



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corresponds to channel 0. The GUI allows the user to increment or decrement the value stored in registers 4-7 by one bit, corresponding to a 4 mV change, or to

enter a value directly. The output voltage for each channel is calculated according to the formula displayed in the GUI.

Registers 04, 05, 06, 06, and 07								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
0	0	0	0	0	0	0	0	Channel Y Nominal Set Point = 0.000 volts
0	0	0	0	0	0	0	1	Channel Y Nominal Set Point = 0.004 volts
1	1	1	1	1	0	1	0	Channel Y Nominal Set Point = 1.000 volts

Table 2: Programmable reference set point values.

Output Voltage and Dynamic Voltage Control

Channel	Output Voltages (Volts)			RDiv (kOhms)		Reference Set Points (Volts)			V/s
	Nominal	High	Low	R1	R2	Nominal	High	Low	
Channel 0	1.200	1.250	1.140	20	80	0.960	1.000	0.912	500
Channel 1	1.800	1.888	1.712	50	50	0.900	0.944	0.856	800
Channel 2	2.500	2.500	2.370	60	40	1.000	1.000	0.948	1000
Channel 3	3.300	3.460	3.140	80	20	0.660	0.692	0.628	2000

Soft-Start Slew Rate = $S_{Ref} * (1 + R1/R2)$
 $V_{out} = V_{ref} * (1 + R1/R2)$

Figure 5: Channel 0 through 3 reference set points

Registers 08, 09, 0A, and 0B								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	X	X	X	X	X	X	X	These registers are unused, do not modify.

Table 3: Unused registers

Registers 0C-0F correspond to the sequence position and power-on/off delay settings of channels 3 through 0 respectively. The channels will only sequence on when the channel is not in manual mode. Any channel can occupy any sequence position, as long as no

sequence positions are skipped and the last sequence position is entered into the appropriate register (R14). If an intermediate bus is used to supply other channels then this channel must be enabled prior to the channels it is supplying. There is no stipulation on the



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number of channels that can occupy the same sequence position. Each channel has its own power-on delay, which may be set to 1.5, 12.5, 25, or 50 ms. Each channel will be enabled a power on delay after its sequence position has been entered. Similarly, each channel will be

disabled a power off delay after its sequence position has been entered during a power off sequence. When SEQUENCING is selected, the power on delay is included in the sequence termination timeout period, and it should be taken into account accordingly.

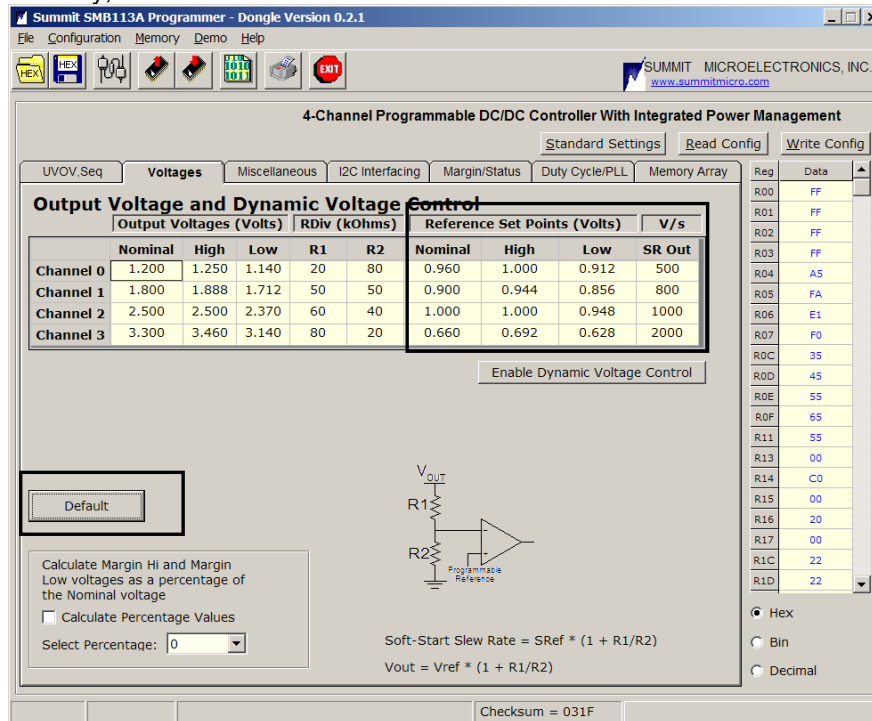


Figure 6: The expert settings allow the user to manually adjust the reference voltages used to determine the output voltages.

Registers 0C, 0D, 0E, and 0F								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
0	0	1	1	X	X	X	X	Channel Y sequence position = 4
0	1	0	0	X	X	X	X	Channel Y sequence position = 3
0	1	0	1	X	X	X	X	Channel Y sequence position = 2
0	1	1	0	X	X	X	X	Channel Y sequence position = 1
1	1	0	0	X	X	X	X	Channel Y not used (Null)
*	*	*	*	X	X	X	X	*All other combinations are disallowed
X	X	X	X	0	0	X	X	Channel Y power-on delay = 1.5 ms
X	X	X	X	0	1	X	X	Channel Y power-on delay = 12.5 ms
X	X	X	X	1	0	X	X	Channel Y power-on delay = 25 ms
X	X	X	X	1	1	X	X	Channel Y power-on delay = 50 ms
X	X	X	X	X	X	0	0	Channel Y power-off delay = 1.5 ms
X	X	X	X	X	X	0	1	Channel Y power-off delay = 12.5 ms
X	X	X	X	X	X	1	0	Channel Y power-off delay = 25 ms
X	X	X	X	X	X	1	1	Channel Y power-off delay = 50 ms

Table 3: Programmable sequence position options.

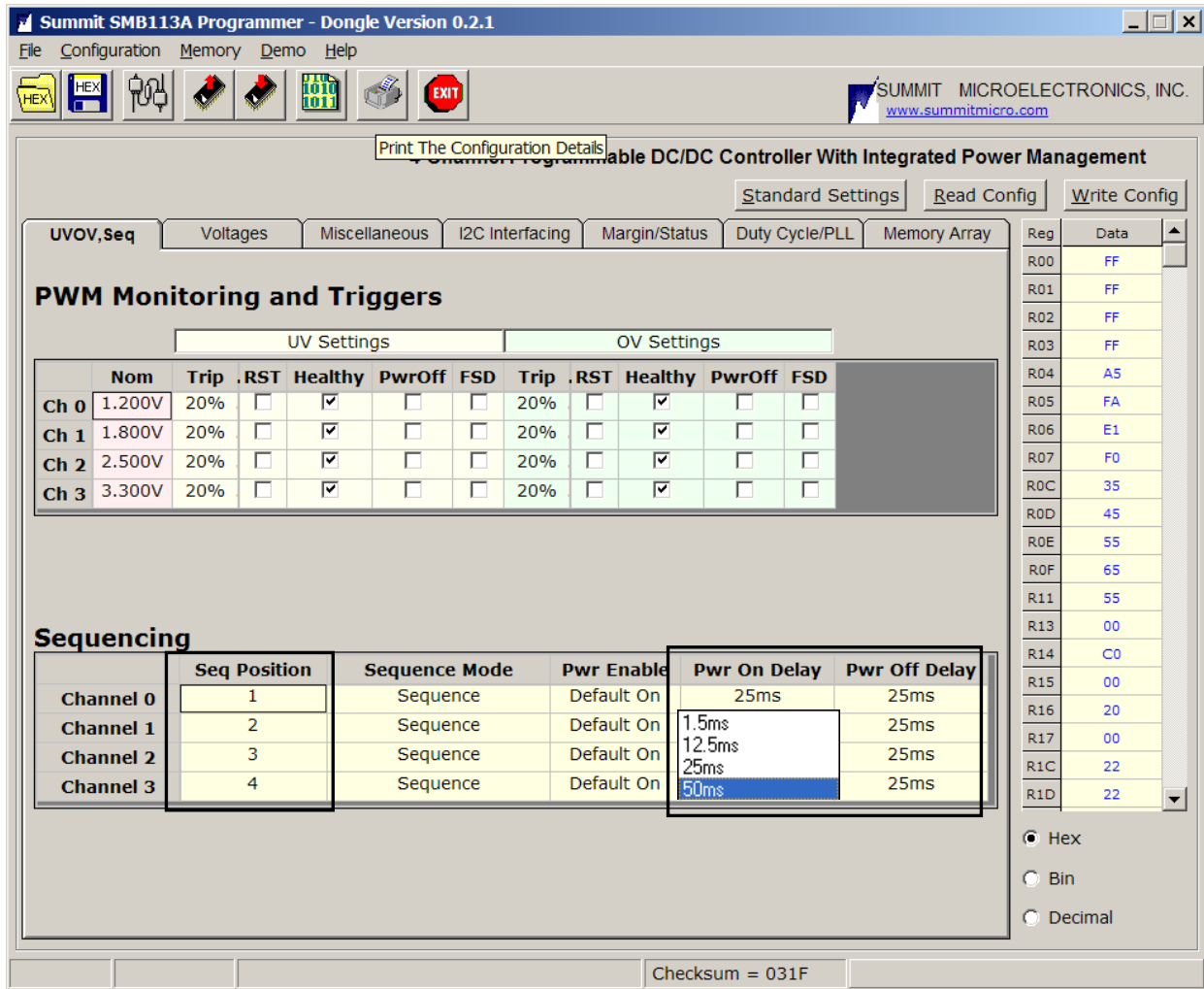


Figure 7: Registers 0x0C to 0x0F determine the sequence position and power on/off delay for all channels.

Register 10								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	X	X	X	X	X	X	X	This register is unused

Table 4: Unused registers

Register 11 controls the sequencing option for all channels. Each channel can be set to sequence on in one of three modes: Normal Sequencing, Sequencing with Enable, and sequencing with channel bypass, for a complete description of the sequencing modes please refer to Figure 8 and register 13. In addition, a

manual mode can be selected during which, sequencing is disabled and the channels are controlled by the enable signal. When a sequencing mode is selected, sequencing can be initiated either by an I²C power on command or by the PWREN pin depending on the programmed settings.



Register 11								Actions
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	X	X	0	0	Disallowed. Do not use.
X	X	X	X	X	X	0	1	Channel 3 Sequence
X	X	X	X	X	X	1	0	Disallowed. Do not use.
X	X	X	X	X	X	1	1	Channel 3 Manual Control
X	X	X	X	0	0	X	X	Disallowed. Do not use.
X	X	X	X	0	1	X	X	Channel 2 Sequence
X	X	X	X	1	0	X	X	Disallowed. Do not use.
X	X	X	X	1	1	X	X	Channel 2 Manual Control
X	X	0	0	X	X	X	X	Disallowed. Do not use.
X	X	0	1	X	X	X	X	Channel 1 Sequence
X	X	1	0	X	X	X	X	Disallowed. Do not use.
X	X	1	1	X	X	X	X	Channel 1 Manual Control
0	0	X	X	X	X	X	X	Disallowed. Do not use.
0	1	X	X	X	X	X	X	Channel 0 Sequence
1	0	X	X	X	X	X	X	Disallowed. Do not use.
1	1	X	X	X	X	X	X	Channel 0 Manual Control

Table 5: Programmable sequence mode options.

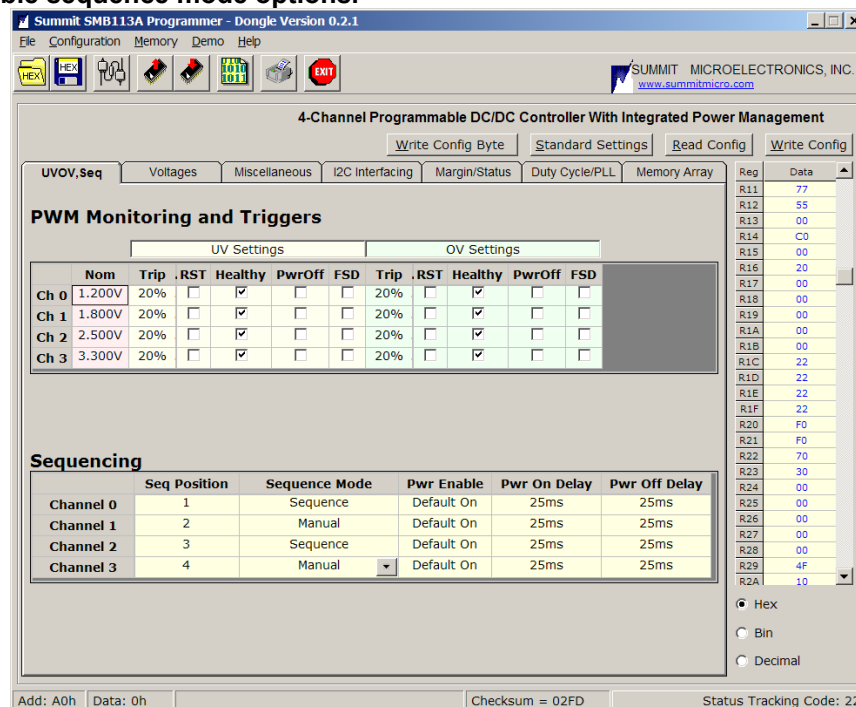


Figure 8: Register 11 controls the sequencing option for all channels.

Register 13 controls the mode in which the SMB113A receives the enable signal. There are three ways a channel can receive its enable signal: from a volatile configuration bit that can be initialized on or off (Default On or Default Off), or from the general purpose enable input. When a channel is in the normal sequencing mode, the enable input will be disengaged. The enable mode for each channel can

be set individually. When the enable signal is assigned to the volatile configuration register (R90), the register must be initialized upon receipt of system power. If initialized ON, then a power on command will begin the sequencing for that channel; when initialized to off, an active enable must be supplied before a power on command will commence sequencing.



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Register 12								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	X	X	X	X	X	X	X	This register is unused

Table 6: Unused registers

Register 13								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	X	X	X	X	X	0	0	Channel 3 Defaulted On
X	X	X	X	X	X	0	1	Channel 3 Default Off
X	X	X	X	X	X	1	0	Channel 3 PWREN
X	X	X	X	X	X	1	1	Disallowed. Do not use.
X	X	X	X	0	0	X	X	Channel 2 Defaulted On
X	X	X	X	0	1	X	X	Channel 2 Default Off
X	X	X	X	1	0	X	X	Channel 2 PWREN
X	X	X	X	1	1	X	X	Disallowed. Do not use.
X	X	0	0	X	X	X	X	Channel 1 Defaulted On
X	X	0	1	X	X	X	X	Channel 1 Default Off
X	X	1	0	X	X	X	X	Channel 1 PWREN
X	X	1	1	X	X	X	X	Disallowed. Do not use.
0	0	X	X	X	X	X	X	Channel 0 Defaulted On
0	1	X	X	X	X	X	X	Channel 0 Default Off
1	0	X	X	X	X	X	X	Channel 0 PWREN
1	1	X	X	X	X	X	X	Disallowed. Do not use.

Table 7: Programmable enable signal source for SMB113A.

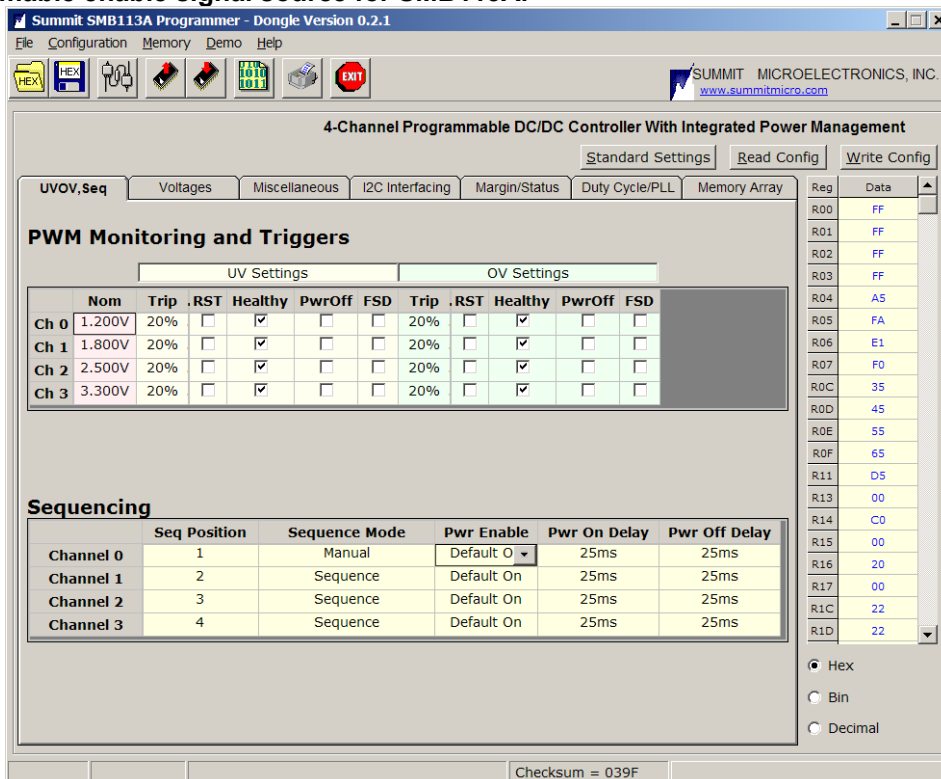


Figure 9: Register 13 controls the enable options for all channels.



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Register 14 controls the settings for input voltage monitoring and the power on sequencing control.

A power on sequencing operation can be initiated by writing to a volatile register, or by asserting the general-purpose enable input pin, PWREN.

Sequencing can be initiated by the PWREN pin in two ways, by asserting the PWREN pin high, or by programming the enable input as an active low push button enable were the PWREN pin is momentarily asserted low.

If no sequencing control mechanism is selected, sequencing will commence as soon as power is

supplied to the SMB113A, provided the channels are enabled.

If a sequencing control mechanism is selected, sequencing will commence once the sequencing mechanism is provided.

Input voltage monitoring thresholds allow the user to select whether a violation in the UV/OV thresholds result in the termination of the supplies. The available options allow the supplies to be sequenced off in the opposite order as they where sequenced on (power-off) or immediately terminate all supplies (force shutdown).

Register 14								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
0	X	X	X	X	X	X	X	Register 91 initiates sequencing. Labeled Wait for I2C Power on command
1	X	X	X	X	X	X	X	Register 91 does not initiate sequencing. Labeled Wait for I2C Power on command
X	0	X	X	X	X	X	X	PWREN pin does not initiate sequencing
X	1	X	X	X	X	X	X	PWREN pin initiates sequencing
X	X	0	X	X	X	X	X	UV2 does not trigger Power-Off
X	X	1	X	X	X	X	X	UV2 triggers Power-Off
X	X	X	0	X	X	X	X	UV1 does not trigger Power-Off
X	X	X	1	X	X	X	X	UV1 triggers Power-Off
X	X	X	X	0	X	X	X	Power-Off not latched
X	X	X	X	1	X	X	X	Power-Off latched by UV1 or UV2 Trigger
X	X	X	X	X	0	X	X	UV2 does not trigger Force Shutdown
X	X	X	X	X	1	X	X	UV2 triggers Force Shutdown
X	X	X	X	X	X	0	X	UV1 does not trigger Force Shutdown
X	X	X	X	X	X	1	X	UV1 triggers Force Shutdown
X	X	X	X	X	X	X	0	Force Shutdown not latched
X	X	X	X	X	X	X	1	Force Shutdown latched by UV1 or UV2 Trigger

Table 8: Programmable under voltage options for SMB113A.



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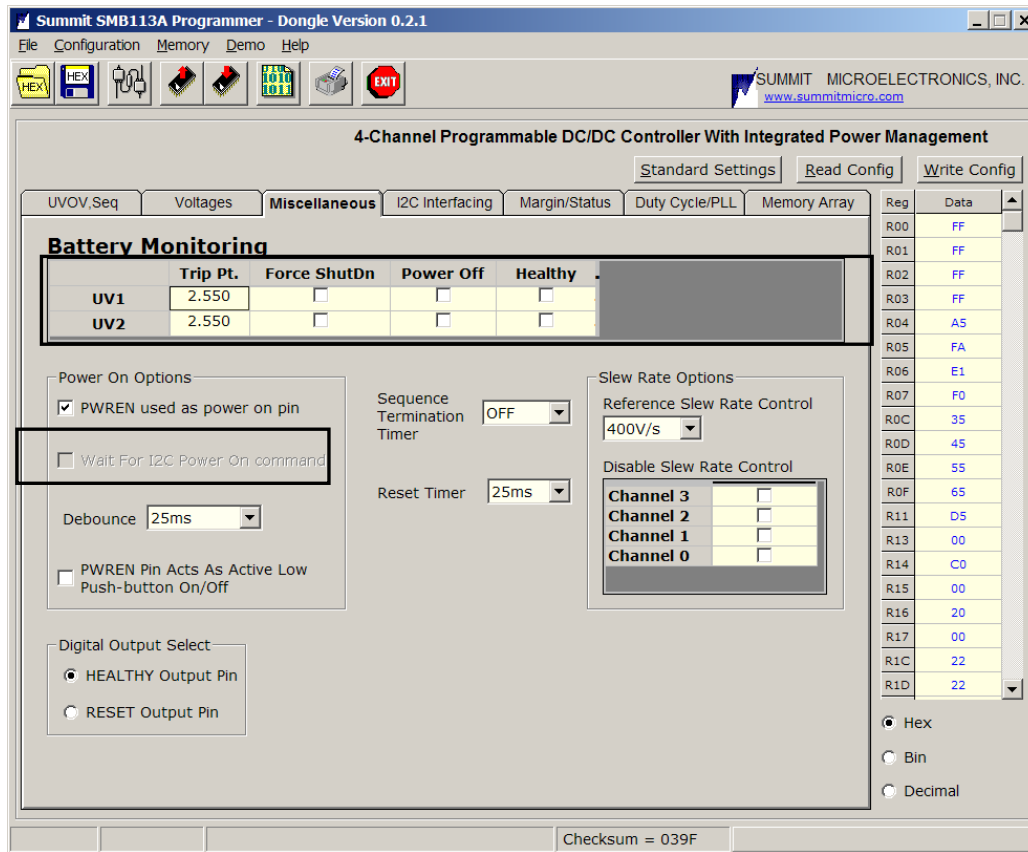


Figure 10: Register 14 determines the settings for the input voltage monitor functions.

The SMB113A is equipped with a global slew rate limiting soft start feature. A soft start allows the output voltages to be gradually ramped up at a rate that is proportional to the final output voltage and the global slew rate setting. The selectable global slew rate values vary from 400V/s to 20 V/s. The actual slew rate for each channel can then be computed from the equation

$$SR_{OUT} = SR_{REF} * (1 + R1/R2)$$

All possible slew rates are displayed in Table 6 as a function of the global slew rate reference and the resistor divider settings.

The soft start control can also be disabled when necessary; however, the soft start function should not be disabled on the boost channels.

Global Slew Rate			400V/sec	200V/sec	100V/sec	50V/sec	50V/sec	33V/sec	25V/sec	20V/sec
Resistor Divider	Voltage Range	Voltage Step Size	Output Slew Rate (V/sec)							
90K/10K	0 to 10V	12mV	4000	2000	1000	670	500	330	250	200
80K/20K	0 to 5V	11mV	2000	1000	500	335	250	165	125	100
70K/30K	0 to 3.33V	10mV	1333	667	333	223	167	110	83	67
60K/40K	0 to 2.5V	9mV	1000	500	250	168	125	83	63	50
50K/50K	0 to 2.0V	8mV	800	400	200	134	100	66	50	40
40K/60K	0 to 1.67V	7mV	667	333	167	112	83	55	42	33
30K/70K	0 to 1.43V	6mV	571	286	143	96	71	47	36	29

Table 9: Voltage slew rates as a function of the internal resistor divider and the global slew rate setting.



Register 15								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
0	0	0	X	X	X	X	X	Global Slew Rate = 400 V/s
0	0	1	X	X	X	X	X	Global Slew Rate = 200 V/s
0	1	0	X	X	X	X	X	Global Slew Rate = 100 V/s
0	1	1	X	X	X	X	X	Global Slew Rate = 67 V/s
1	0	0	X	X	X	X	X	Global Slew Rate = 50 V/s
1	0	1	X	X	X	X	X	Global Slew Rate = 33 V/s
1	1	0	X	X	X	X	X	Global Slew Rate = 25 V/s
1	1	1	X	X	X	X	X	Global Slew Rate = 20 V/s

Table 10: Programmable global slew rate options for the SMB113A.

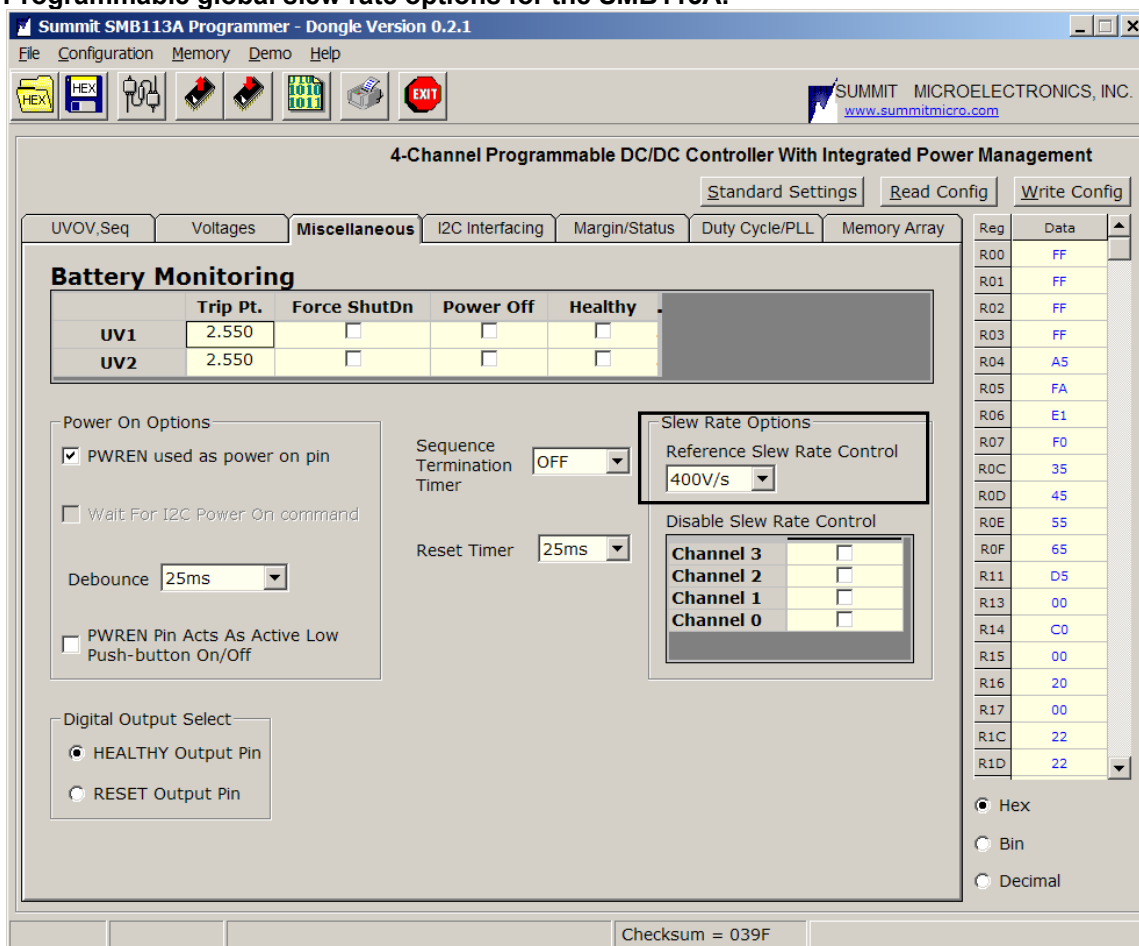


Figure 11: Register 15 sets the global slew rate.

Register 16 controls the locking of the configuration registers can be locked to avoid any unintentional writes to these registers. This option, however, is not

allowed when using the GUI, as it is irreversible. The memory that is separated into two continuous independently lockable sections can also be locked.



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Registers 16								Register locks	
D7	D6	D5	D4	D3	D2	D1	D0	Actions	
X	X	X	X	X	0	X	X	Configuration registers unlocked	
X	X	X	X	X	1	X	X	Configuration registers locked	
X	X	X	X	X	X	0	X	Memory Block 1 unlocked	
X	X	X	X	X	X	1	X	Memory Block 1 locked	
X	X	X	X	X	X	X	0	Memory Block 2 unlocked	
X	X	X	X	X	X	X	1	Memory Block 2 locked	

Table 11: Programmable register locking options for volatile and non-volatile memory.

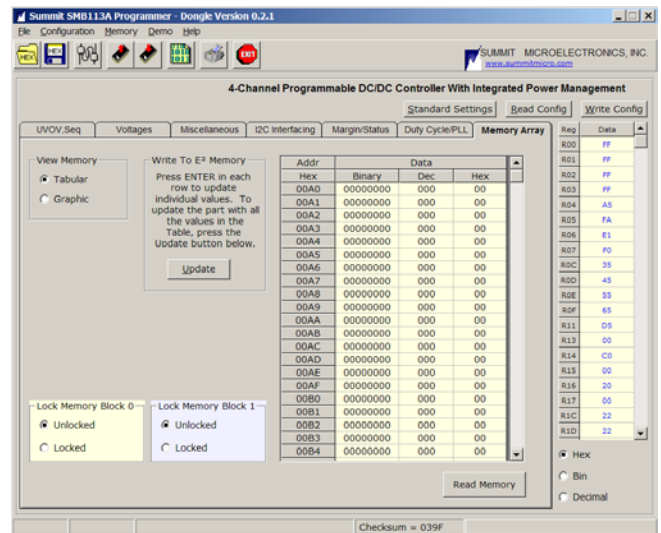
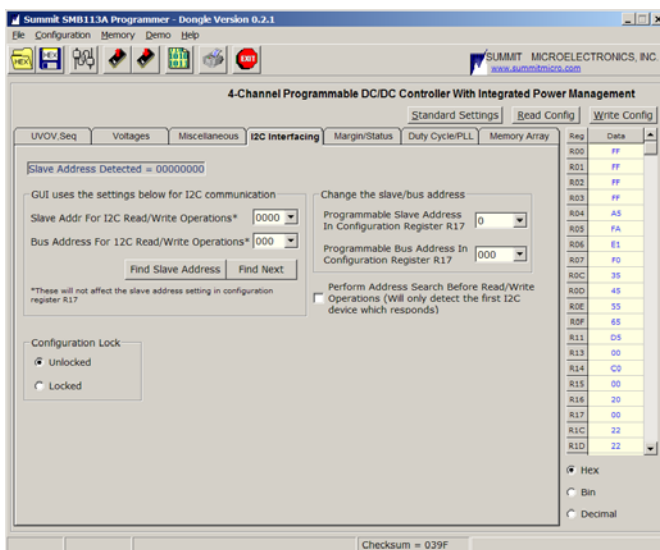


Figure 12: Register 16 controls the configuration and memory locking mechanism.



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Register 17 contains the I²C Slave address from which all registers are accessed. The slave address can be set to any of the 256 possible addresses. The SMB113A is always the slave, never the master. After the address has been changed using the GUI it will be

necessary to use the new address for the next read or write command. An address search can also be performed in which the address of the first device to sent an acknowledge is returned.

Registers 17 Slave Address								Actions
D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	Seven level Dynamic voltage control disabled
1	X	X	X	X	X	X	X	Seven level Dynamic voltage control enabled
X	0	0	0	0	0	0	0	Slave address = 0000000
X	0	0	0	0	0	0	1	Slave address = 0000001
X	1	1	1	1	1	1	1	Slave address = 1111111

Table 12: Programmable slave address options.

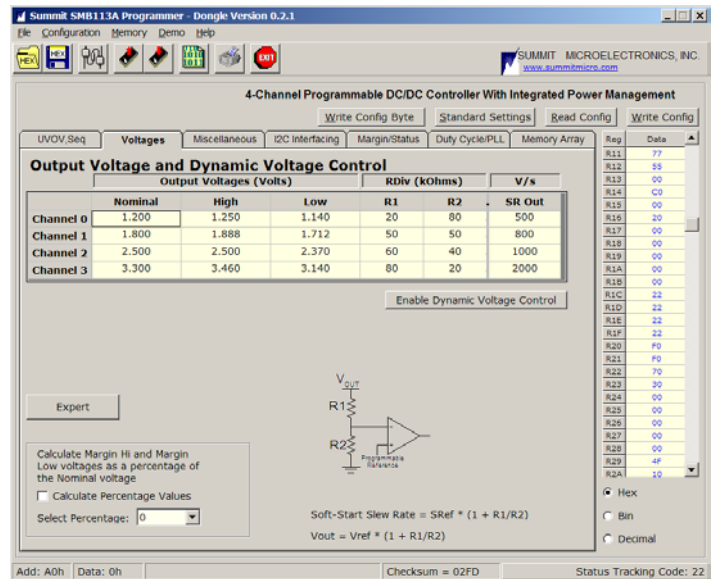
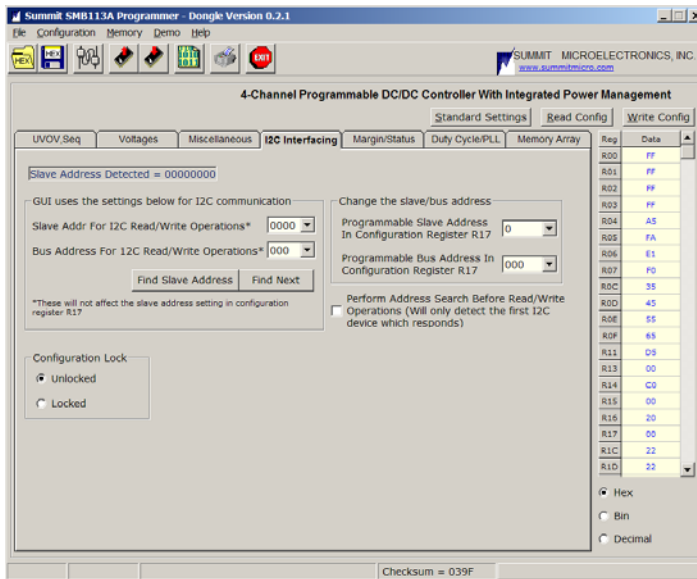


Figure 13: Register 17 sets the slave address, and the seven level dynamic voltage control for the SMB113A.

Register 18, 19, 1A, and 1B								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	X	X	X	X	X	X	X	This register is unused

Table 13: Unused registers

Registers 1C through 1F correspond to the over voltage and under voltage settings of channels 3 through 0 respectively. Similar to the battery monitoring registers, registers 1C-1F control whether

an over voltage or under voltage cause a power off or force shutdown. In addition, to triggering a power off, a the HEALTHY status pin can also be asserted when an over voltage or under voltage occur.



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Registers 1C, 1D, 1E, and 1F Over Voltage and Under Voltage triggers								Actions
D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	Channel Y OV does not trigger a Force Shutdown
1	X	X	X	X	X	X	X	Channel Y OV triggers a Force Shutdown
X	0	X	X	X	X	X	X	Channel Y OV does not trigger a Power-On/Off
X	1	X	X	X	X	X	X	Channel Y OV triggers a Power-On/Off
X	X	0	X	X	X	X	X	Channel Y OV does not trigger a Healthy
X	X	1	X	X	X	X	X	Channel Y OV triggers a Power- Healthy
X	X	X	0	X	X	X	X	Channel Y OV does not trigger a Power- nRESET
X	X	X	1	X	X	X	X	Channel Y OV triggers a Power- nRESET
X	X	X	X	0	X	X	X	Channel Y UV does not trigger a Force Shutdown
X	X	X	X	1	X	X	X	Channel Y UV triggers a Force Shutdown
X	X	X	X	X	0	X	X	Channel Y UV does not trigger a Power-On/Off
X	X	X	X	X	1	X	X	Channel Y UV triggers a Power-On/Off
X	X	X	X	X	X	0	X	Channel Y UV does not trigger a Healthy
X	X	X	X	X	X	1	X	Channel Y UV triggers a Power- Healthy
X	X	X	X	X	X	X	R	This bit is READ-only. Attempt to change will cause part malfunction

Table 14: Programmable under voltage and over voltage options.

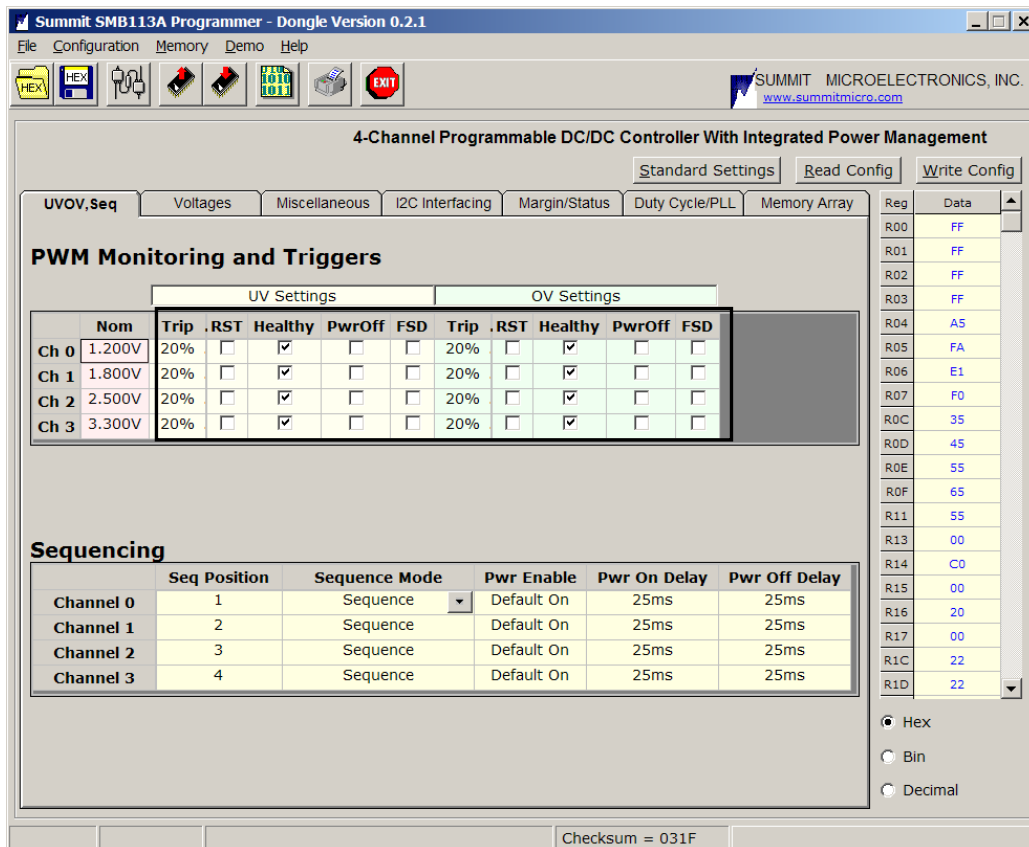


Figure 14: Registers 1C through 1F control the over voltage and under voltage fault responses for channels 0 through 3

Registers 20, 21, 22, and 23 bits 7 and 6 control the output voltage range for each channel. The 0 to 90 options allow the channel output to approach 0V while limiting the upper output limit. The 10 to 100% limit

allows the output to equal the input voltage but limits the minimum voltage the controller can sustain.



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Register 20 Channel 0 duty cycle options								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
0	1	X	X	X	X	X	X	100% Max duty cycle, minimum duty cycle enabled
1	1	X	X	X	X	X	X	90% Max duty cycle, minimum duty cycle disabled

Table 15: Channel 0 duty cycle options.

Register 21 Channels 2 and 1 duty cycle options								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
1	1	X	X	X	X	X	X	Must set bit 7 to a 1

Table 16: Channel 1 and 2 duty cycle options.

Register 22								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
0	X	X	X	X	X	X	X	Channel 2 100% Max duty cycle, minimum duty cycle enabled
1	X	X	X	X	X	X	X	Channel 2 90% Max duty cycle, minimum duty cycle disabled
X	0	X	X	X	X	X	X	Channel 1 100% Max duty cycle, minimum duty cycle enabled
X	1	X	X	X	X	X	X	Channel 1 90% Max duty cycle, minimum duty cycle disabled

Table 17: Channel 1 and 2 duty cycle options.

Register 23 Channel 3 duty cycle options								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
0	X	X	X	X	X	X	X	Channel 3 100% Max duty cycle, minimum duty cycle enabled
1	X	X	X	X	X	X	X	Channel 3 90% Max duty cycle, minimum duty cycle disabled

Table 18: Channel 3 duty cycle options.

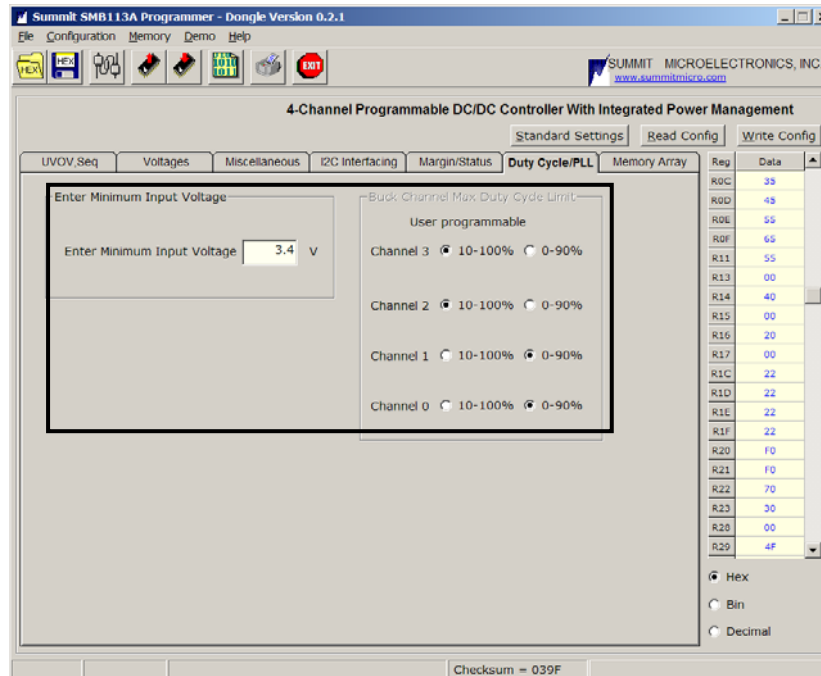


Figure 15: Duty cycle options Tab. The correct settings are chosen by the GUI based on the user provided input voltage setting.

Registers 20 through 23 bits 5 to 0 control the OV and UV glitch filters and OV and UV trip points for channels 0 through 3 respectively. The UV and OV trip

points can be programmed separately for each of the four PWM outputs, the available settings include 5, 10, 15, and 20 percent above (OV) the nominal output voltage, and 5, 10, 15 and 20 percent below (UV) the



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nominal output voltages settings. In order for a UV or OV condition to occur the output voltage must exceed the trip point for a minimum period corresponding to

the value in the glitch filter register. The glitch filter times are selectable at 0 or 8 μ s.

Registers 20, 21, 22, 23								Over Voltage and Under Voltage glitch filter and trip levels
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	X	0	X	X	X	X	X	Channel Y OV glitch filter off
X	X	1	X	X	X	X	X	Channel Y OV glitch filter 8 us
X	X	X	0	X	X	X	X	Channel Y UV glitch filter off
X	X	X	1	X	X	X	X	Channel Y UV glitch filter 8 us
X	X	X	X	0	0	X	X	Channel Y OV trip level 20%
X	X	X	X	0	1	X	X	Channel Y OV trip level 15%
X	X	X	X	1	0	X	X	Channel Y OV trip level 10%
X	X	X	X	1	1	X	X	Channel Y OV trip level 5%
X	X	X	X	X	X	0	0	Channel Y UV trip level 20%
X	X	X	X	X	X	0	1	Channel Y UV trip level 15%
X	X	X	X	X	X	1	0	Channel Y UV trip level 10%
X	X	X	X	X	X	1	1	Channel Y UV trip level 5%

Table 19: Under voltage and over voltage trip point options.



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Summit SMB113A Programmer - Dongle Version 0.2.1

File Configuration Memory Demo Help

HEX HEX USB USB I2C EXIT

SUMMIT MICROELECTRONICS, INC. www.summitmicro.com

4-Channel Programmable DC/DC Controller With Integrated Power Management

Standard Settings Read Config Write Config

UVOV,Seq Voltages Miscellaneous I2C Interfacing Margin/Status Duty Cycle/PLL Memory Array

PWM Monitoring and Triggers

UV Settings							OV Settings				
	Nom	Trip	RST	Healthy	PwrOff	FSD	Trip	RST	Healthy	PwrOff	FSD
Ch 0	1.200V	20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch 1	1.800V	5%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch 2	2.500V	10%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch 3	3.300V	15%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
		20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>		<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Sequencing

	Seq Position	Sequence Mode	Pwr Enable	Pwr On Delay	Pwr Off Delay
Channel 0	1	Sequence	Default On	25ms	25ms
Channel 1	2	Sequence	Default On	25ms	25ms
Channel 2	3	Sequence	Default On	25ms	25ms
Channel 3	4	Sequence	Default On	25ms	25ms

Checksum = 031F

Reg Data

R00	FF
R01	FF
R02	FF
R03	FF
R04	A5
R05	FA
R06	E1
R07	F0
R0C	35
R0D	45
R0E	55
R0F	65
R11	55
R13	00
R14	C0
R15	00
R16	20
R17	00
R1C	22
R1D	22

Hex
Bin
Decimal

Register 24, 25, 26, and 27

D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	X	X	X	X	X	X	X	This register is unused

Table 20: Unused registers

Register 28 controls the UV1 and UV2 trip point levels. The programmable threshold values range from 2.55V to 3.6V in 150 mV increments. The UV1 trip point

should always exceed the UV2 trip point. This requirement stems from the fact that UV1 is a latched pin that will not be reset unless the UV2 trip point is passed and then exceeded.



Register 28 UV1 and UV2 programmable threshold levels								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	0	X	X	X	X	X	X	Use for SMB113A
X	1	X	X	X	X	X	X	Use for SMB117
X	X	0	0	0	X	X	X	UV2 trip level = 2.55 V
X	X	0	0	1	X	X	X	UV2 trip level = 2.7 V
X	X	1	1	1	X	X	X	UV2 trip level = 3.6 V
X	X	X	X	X	0	0	0	UV1 trip level = 2.55 V
X	X	X	X	X	1	0	1	UV1 trip level = 2.7 V
X	X	X	X	X	1	1	1	UV1 trip level = 3.6 V

Table 21: Programmable battery monitoring options.

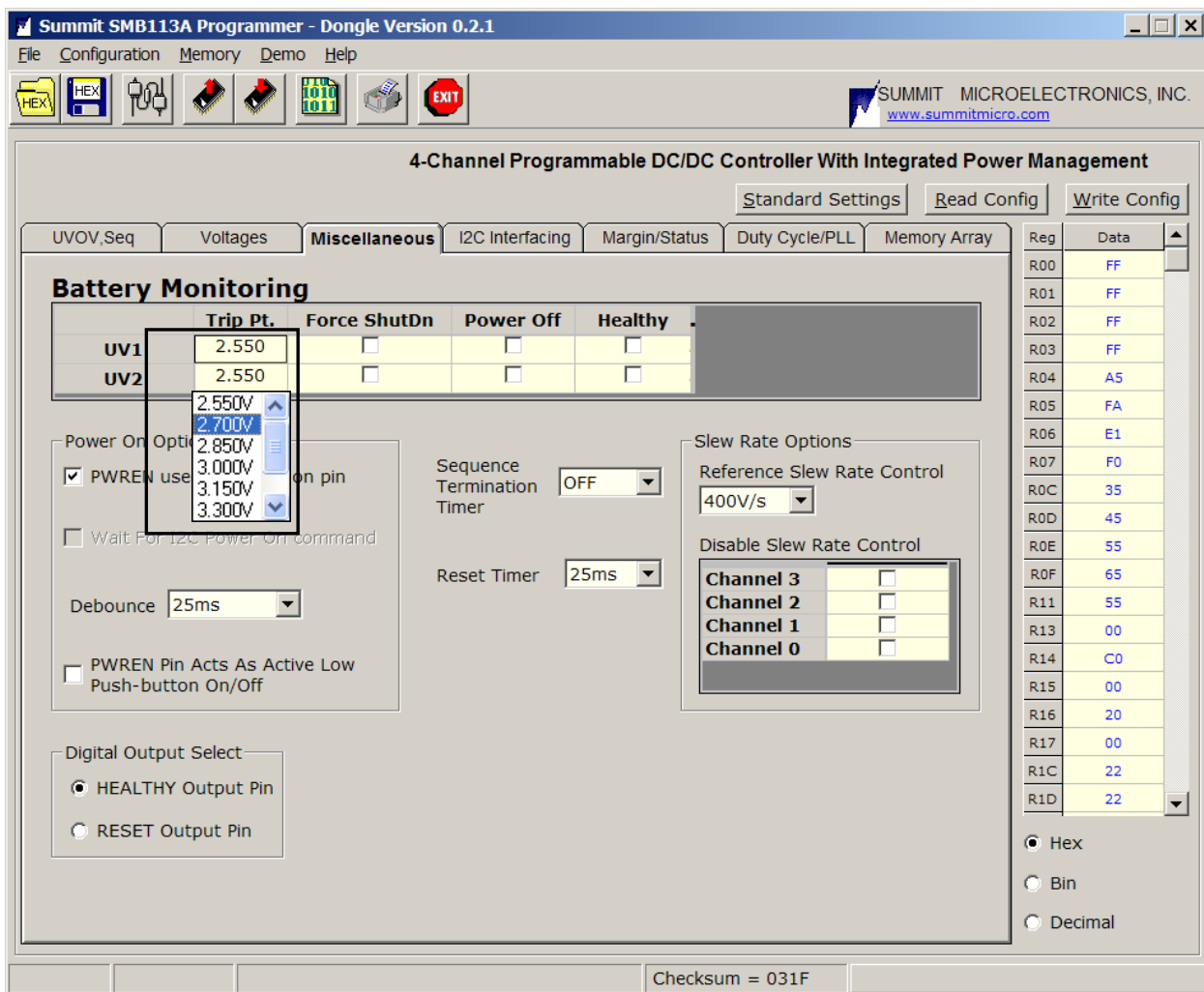


Figure 17: Register 28 controls the two input voltage monitoring trip point levels.

Register 29								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	0	X	X	X	X	X	X	Single phase, all channels switch in phase
X	1	X	X	X	X	X	X	Half of channels switch 180 degrees out of phase

Table 22: Channel interleaving options.



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Register 2A contains the settings for the sequence termination timer. When one of the three sequencing modes is selected, the sequence termination timer can be used. This function prevents a stalled power on or power off sequencing operation from occurring. In the event that the sequence termination timer expires before a channel passes its UV setting, all supplies will

be immediately terminated with a force shutdown operation. The allowable sequence termination timer timeout periods are 25, 50, 100, and 200 ms. It is not advised that the sequence termination timer should be used with the sequencing with enable; unless the enable signal is valid at the time the power-on sequencing operation begins.

Register 2A								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
0	X	X	X	X	X	X	X	PWREN pin acts as an active Low push-button to initiate sequencing
1	X	X	X	X	X	X	X	PWREN pin act as an active High input to initiate sequencing
X	X	0	0	X	X	X	X	PWREN pin debounce time = 0 ms
X	X	0	1	X	X	X	X	PWREN pin debounce time = 25 ms
X	X	1	0	X	X	X	X	PWREN pin debounce time = 50 ms
X	X	1	1	X	X	X	X	PWREN pin debounce time = 100 ms
X	X	X	X	0	0	X	X	Sequence termination timeout period = 0 ms
X	X	X	X	0	1	X	X	Sequence termination timeout period = 50 ms
X	X	X	X	1	0	X	X	Sequence termination timeout period = 100 ms
X	X	X	X	1	1	X	X	Sequence termination timeout period = 200 ms
X	X	X	X	X	X	0	0	Reset timeout period = 25 ms
X	X	X	X	X	X	0	1	Reset timeout period = 50 ms
X	X	X	X	X	X	1	0	Reset timeout period = 100ms
X	X	X	X	X	X	1	1	Reset timeout period = 200 ms

Table 23: Programmable sequence termination options.

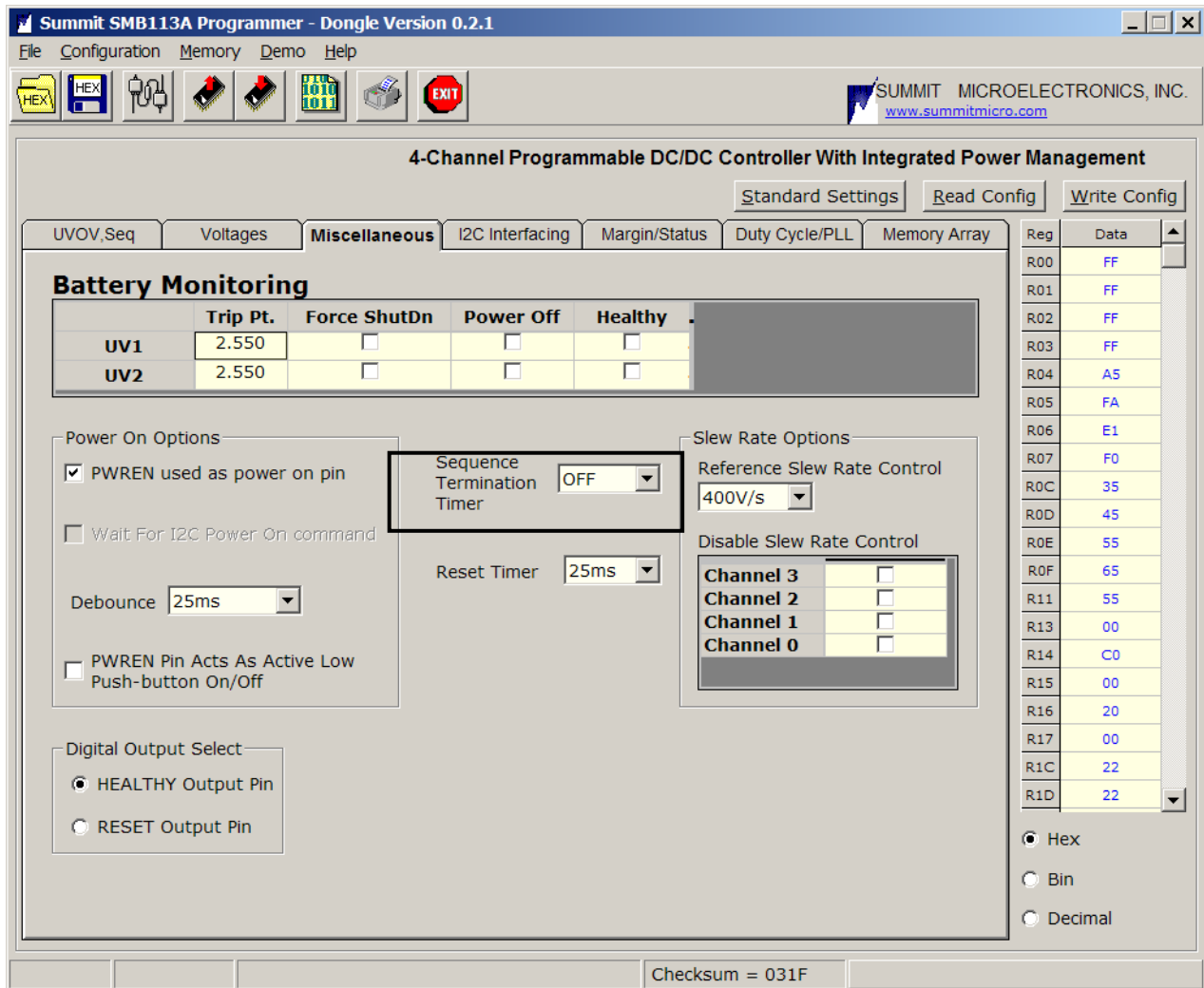


Figure 18: Register 2A controls Sequence Termination Timer setting.

Register 2B contains the settings capable of disabling the soft start feature. When soft start is disabled, the outputs will slew up at a fixed rate dependent on the maximum slew rate capabilities of the output drivers.

When enabled, the outputs will slew up at a rate dependent on the programmed output voltage and the global slew rate reference.

Register 2B								Disable soft start
D7	D6	D5	D4	D3	D2	D1	D0	Actions
0	X	X	X	X	X	X	X	Channel 0 soft start disabled
1	X	X	X	X	X	X	X	Channel 0 soft start enabled
X	0	X	X	X	X	X	X	Channel 1 soft start disabled
X	1	X	X	X	X	X	X	Channel 1 soft start enabled
X	X	0	X	X	X	X	X	Channel 2 soft start disabled
X	X	1	X	X	X	X	X	Channel 2 soft start enabled
X	X	X	0	X	X	X	X	Channel 3 soft start disabled
X	X	X	1	X	X	X	X	Channel 3 soft start enabled
X	X	X	X	1	1	1	1	These bits are READ-only. Attempt to change will cause part malfunction

Table 24: Programmable soft start settings.

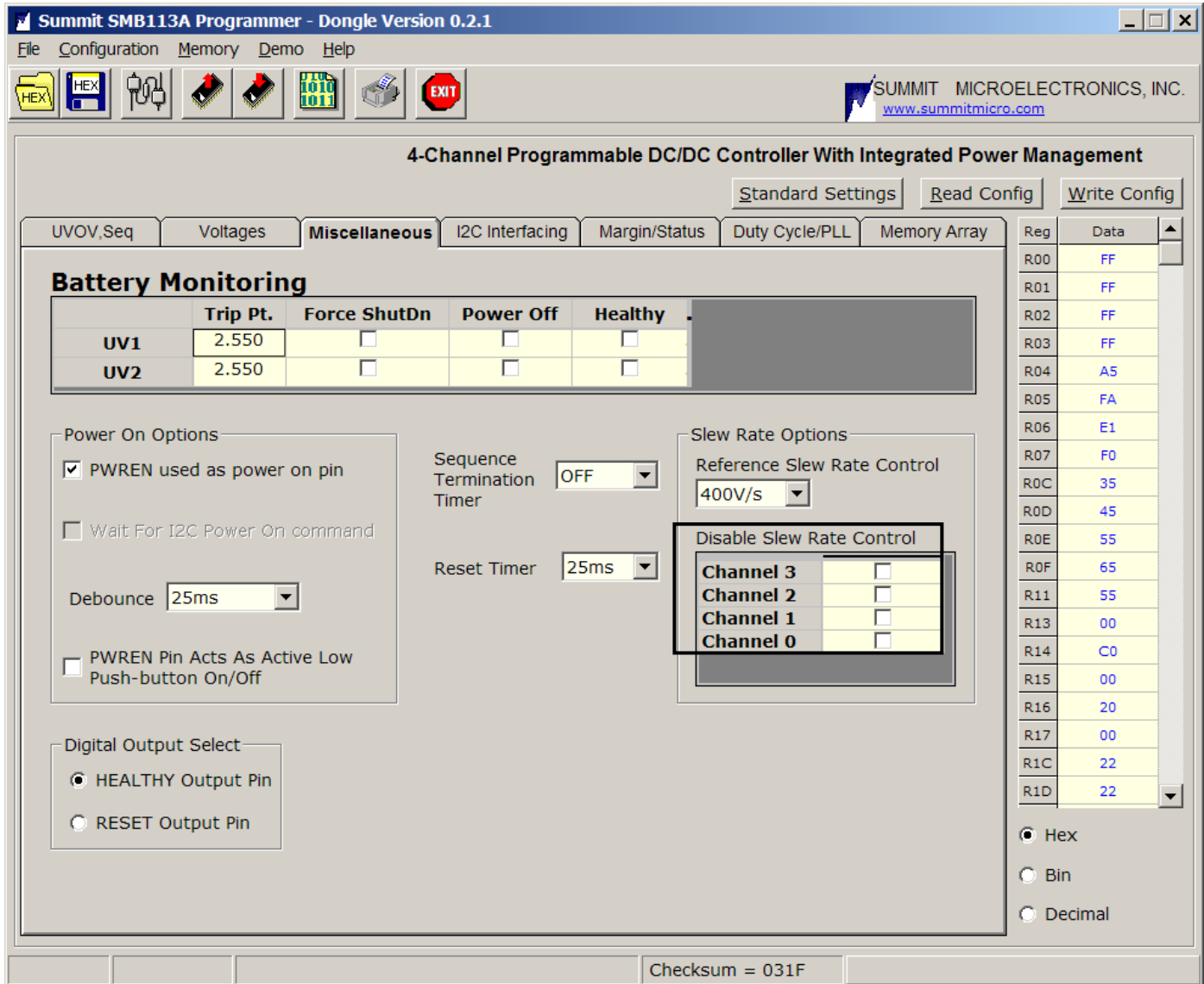


Figure 19: Register 2B enables and disabled the soft Start function on the SMB113A.

Register 2C contains data pertinent to the sequencing functionality of the SMB113A. When any of the three sequencing modes are selected, it is necessary to store the last sequence position used. The sequence positions must begin at sequence position 1 and incrementally increase. It is necessary to store the

last sequence position plus one in this register so that the proper operating mode is transitioned to. By default, the SMB113A GUI automatically updates the last sequence position used according to the necessary guidelines.

Register 2C									Last sequence position used + 1 (HIDDEN REGISTER)	
D7	D6	D5	D4	D3	D2	D1	D0	Actions		
X	X	X	X	0	1	0	1	Last Sequence position used + 1 = 1		
X	X	X	X	0	1	0	0	Last Sequence position used + 1 = 2		
X	X	X	X	0	0	1	1	Last Sequence position used + 1 = 3		
X	X	X	X	0	0	1	0	Last Sequence position used + 1 = 4		
X	X	X	X	*	*	*	*	*All other combinations are disallowed and will cause part malfunction		

Table 25: Programmable last sequence position used options.



4-Channel Programmable DC/DC Controller With Integrated Power Management

Standard Settings | Read Config | Write Config

UVOV,Seq | Voltages | Miscellaneous | I2C Interfacing | Margin/Status | Duty Cycle/PLL | Memory Array

PWM Monitoring and Triggers

UV Settings							OV Settings				
	Nom	Trip	.RST	Healthy	PwrOff	FSD	Trip	.RST	Healthy	PwrOff	FSD
Ch 0	1.200V	20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch 1	1.800V	20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch 2	2.500V	20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Ch 3	3.300V	20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	20%	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Sequencing

	Seq Position	Sequence Mode	Pwr Enable	Pwr On Delay	Pwr Off Delay
Channel 0	1	Sequence	Default On	25ms	25ms
Channel 1	2	Sequence	Default On	25ms	25ms
Channel 2	3	Sequence	Default On	25ms	25ms
Channel 3	4	Sequence	Default On	25ms	25ms

Checksum = 031F

Figure 20: Register 2C sets the last sequence position used during sequencing.

Register 2D allows the healthy output to be asserted when the voltage on the VBATT pin falls below the UV1 or UV2 settings.

Register 2D HEALTHY triggers								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	X	0	X	X	X	X	X	Multiplexed Healthy/nRESET pin acts as Healthy output
X	X	1	X	X	X	X	X	Multiplexed Healthy/nRESET pin acts as Reset output
X	X	X	1	X	X	X	X	Reset Triggers Healthy
X	X	X	X	1	X	X	X	Battery Fault Triggers Healthy
X	X	X	X	X	1	X	X	Power Fail Triggers Healthy
X	X	X	X	X	X	1	X	Battery Fault Triggers Reset
X	X	X	X	X	X	X	1	Power Fail Triggers Reset

Table 26: Programmable options for under voltage on the VBATT supply to trip the healthy pin.

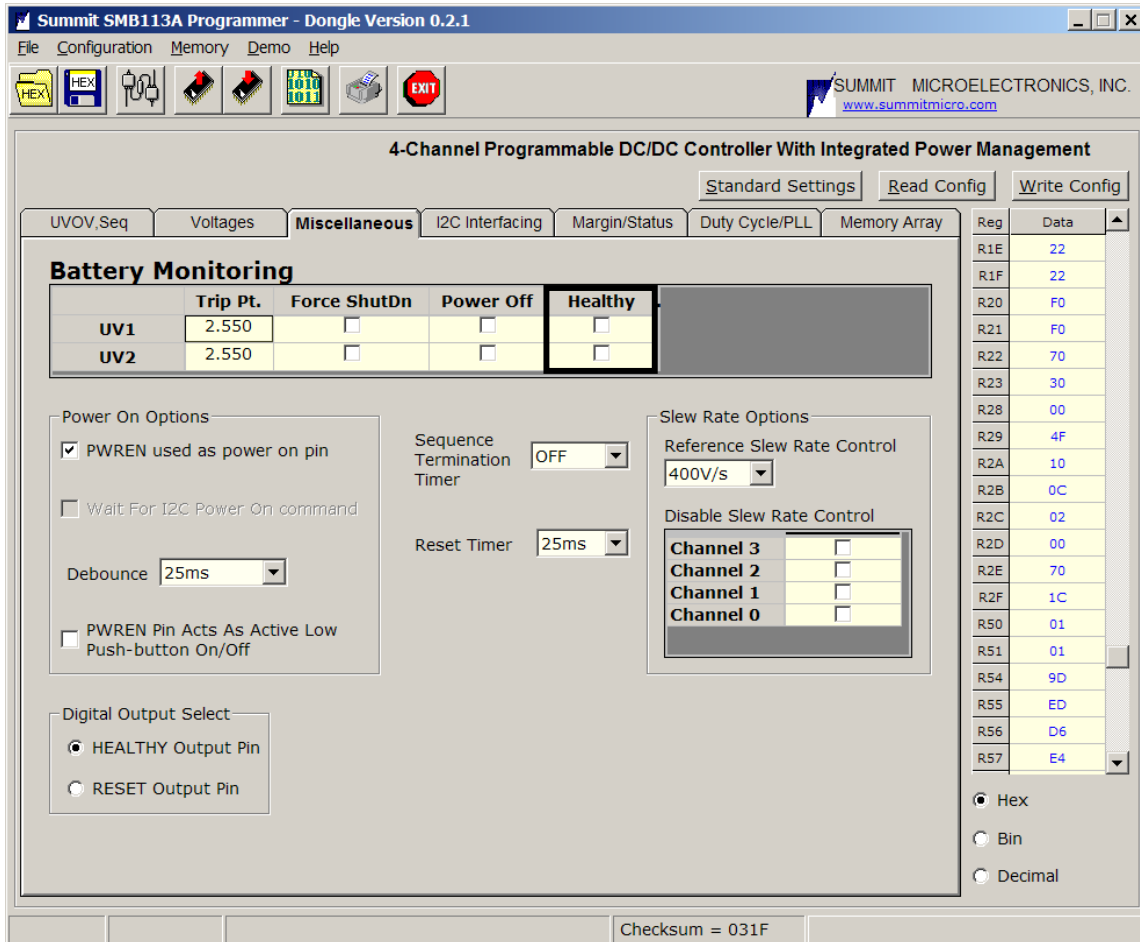


Figure 21: Register 2D controls the HEALTHY pin triggers.

Register 2E and 2F controls the setting of the internal resistor dividers on all channels. The sum of the upper and lower resistors is 100 kΩ. The GUI

automatically selects the value of resistor divider based on the desired output voltage.

Register 2E Internal resistor divider settings on Step Down outputs								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	1	X	X	X	X	X	X	Must set bit 6 to a 1
X	X	0	0	0	X	X	X	Channel 3 R2 = 20k, R1 = 80k
X	X	0	0	1	X	X	X	Channel 3 R2 = 30k, R1 = 70k
X	X	1	1	1	X	X	X	Channel 3 R2 = 90k, R1 = 10k
X	X	X	X	X	0	0	0	Channel 0 R2 = 20k, R1 = 80k
X	X	X	X	X	1	0	1	Channel 0 R2 = 30k, R1 = 70k
X	X	X	X	X	1	1	1	Channel 0 R2 = 90k, R1 = 10k

Table 27: Programmable resistor divider selection options.



Register 2F								Internal resistor divider settings
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	X	0	0	0	X	X	X	Channel 1 R2 = 20k, R1 = 80k
X	X	0	0	1	X	X	X	Channel 1 R2 = 30k, R1 = 70k
X	X	1	1	1	X	X	X	Channel 1 R2 = 90k, R1 = 10k
X	X	X	X	X	0	0	0	Channel 2 R2 = 20k, R1 = 80k
X	X	X	X	X	1	0	1	Channel 2 R2 = 30k, R1 = 70k
X	X	X	X	X	1	1	1	Channel 2 R2 = 90k, R1 = 10k

Table 28: Programmable resistor divider selection options.

4-Channel Programmable DC/DC Controller With Integrated Power Management

Standard Settings | Read Config | Write Config

UVOV,Seq | **Voltagess** | Miscellaneous | I2C Interfacing | Margin/Status | Duty Cycle/PLL | Memory Array

Output Voltage and Dynamic Voltage Control

	Output Voltages (Volts)			RDiv (kOhms)		Reference Set Points (Volts)			V/s
	Nominal	High	Low	R1	R2	Nominal	High	Low	SR Out
Channel 0	1.200	1.250	1.140	40	80	0.960	1.000	0.912	500
Channel 1	1.800	1.888	1.712	50	50	0.900	0.944	0.856	800
Channel 2	2.500	2.500	2.370	70	40	1.000	1.000	0.948	1000
Channel 3	3.300	3.460	3.140	90	20	0.660	0.692	0.628	2000

Enable Dynamic Voltage Control

Default

Calculate Margin Hi and Margin Low voltages as a percentage of the Nominal voltage

Calculate Percentage Values

Select Percentage: 0

Soft-Start Slew Rate = $S_{Ref} * (1 + R1/R2)$

$V_{out} = V_{ref} * (1 + R1/R2)$

Reg | Data

- R1E | 22
- R1F | 22
- R20 | F0
- R21 | F0
- R22 | 70
- R23 | 30
- R28 | 00
- R29 | 4F
- R2A | 10
- R2B | 0C
- R2C | 02
- R2D | 00
- R2E | 70
- R2F | 1C
- R50 | 01
- R51 | 01
- R54 | 9D
- R55 | ED
- R56 | D6
- R57 | E4

Checksum = 031F

Figure 22: Register 2E and 2F set the internal resistor dividers.

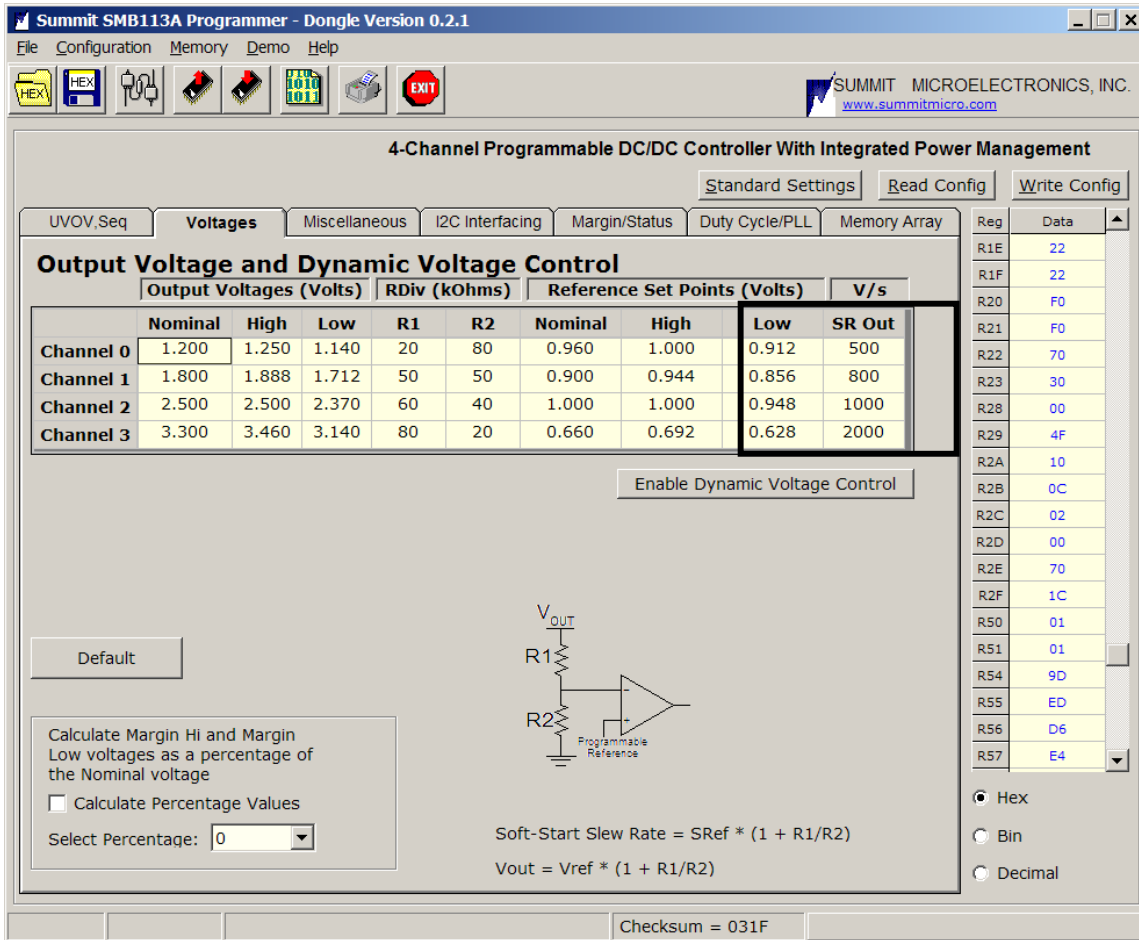


Figure 23: Registers 54 through 57 control the reference voltage for the margin low settings. Registers 5C through 5F control the reference voltages for the margin high settings.

Register 30 through 53								Actions
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	X	X	X	X	X	X	X	These registers are unused, do not modify.

Table 29: Unused registers.

Registers 54 through 57 contain the margin low settings for channels 3-0 respectively and Registers 5C through 5F contain the margin high settings for channels 3 to 0 respectively. All outputs can be adjusted by writing to a volatile margin command register. When a non-volatile write operation is carried out the voltage on the COMP1 pin is adjusted from the nominal setting to the setting corresponding to that

stored in the margin high register. The available settings on this pin range from 0-1.0V on channels
NOTE: When a write or read operation is performed, the SMB113A must not be margining. Subsequently when a write or read operation is selected, the GUI will automatically adjust the outputs to their nominal set points.

Registers 54, 55, 56, and 57 Channel 0-3 Margin low settings (Channel 3 set in Register 54, etc.)								Actions
D7	D6	D5	D4	D3	D2	D1	D0	Actions
0	0	0	0	0	0	0	0	Channel Y Nominal Set Point = 0.000 volts
0	0	0	0	0	0	0	1	Channel Y Nominal Set Point = 0.004 volts
1	1	1	1	1	X	X	1	Channel Y Nominal Set Point = 1.000 volts

Table 30: Programmable margin low set point.



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Register 58 through 5B								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	X	X	X	X	X	X	X	These registers are unused, do not modify.

Table 31: Unused registers.

Registers 5C, 5D, 5E, and 5F Channel 0-3 Margin high settings (Channel 3 set in Register 5C, etc.)								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
0	0	0	0	0	0	0	0	Channel Y Nominal Set Point = 0.000 volts
0	0	0	0	0	0	0	1	Channel Y Nominal Set Point = 0.004 volts
1	1	1	1	1	X	X	1	Channel Y Nominal Set Point = 1.000 volts

Table 32: Programmable margin high set point.

Register 60 through 8F								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	X	X	X	X	X	X	X	These registers are unused, do not modify.

Table 33: Unused registers.

Register 90 is a volatile configuration register used to enable and disable the outputs of channels 0-3. When the SMB113A is not set to normal sequencing mode all outputs can be enabled and disabled by their respective enable signals. When the enable signal is

controlled by I²C initialized to on or I²C initialized to off then register 90 will enable and disable the channel. The setting of this register depends on the current state of register 13, which determines if I²C is initialized as on, or off.

Registers 90 Volatile I ² C Power Enable								
D7	D6	D5	D4	D3	D2	D1	D0	Actions
0	X	X	X	X	X	X	X	Ch 0 Power (h13[7:6]=00) Enabled or (h13[7:6]=01) Disabled
1	X	X	X	X	X	X	X	Ch 0 Power (h13[7:6]=01) Enabled or (h13[7:6]=00) Disabled
X	0	X	X	X	X	X	X	Ch 1 Power (h13[5:4]=00) Enabled or (h13[5:4]=01) Disabled
X	1	X	X	X	X	X	X	Ch 1 Power (h13[5:4]=01) Enabled or (h13[5:4]=00) Disabled
X	X	0	X	X	X	X	X	Ch 2 Power (h13[3:2]=00) Enabled or (h13[3:2]=01) Disabled
X	X	1	X	X	X	X	X	Ch 2 Power (h13[3:2]=01) Enabled or (h13[3:2]=00) Disabled
X	X	X	0	X	X	X	X	Ch 3 Power (h13[1:0]=00) Enabled or (h13[1:0]=01) Disabled
X	X	X	1	X	X	X	X	Ch 3 Power (h13[1:0]=01) Enabled or (h13[1:0]=00) Disabled

Table 34: Programmable sequence mode options.

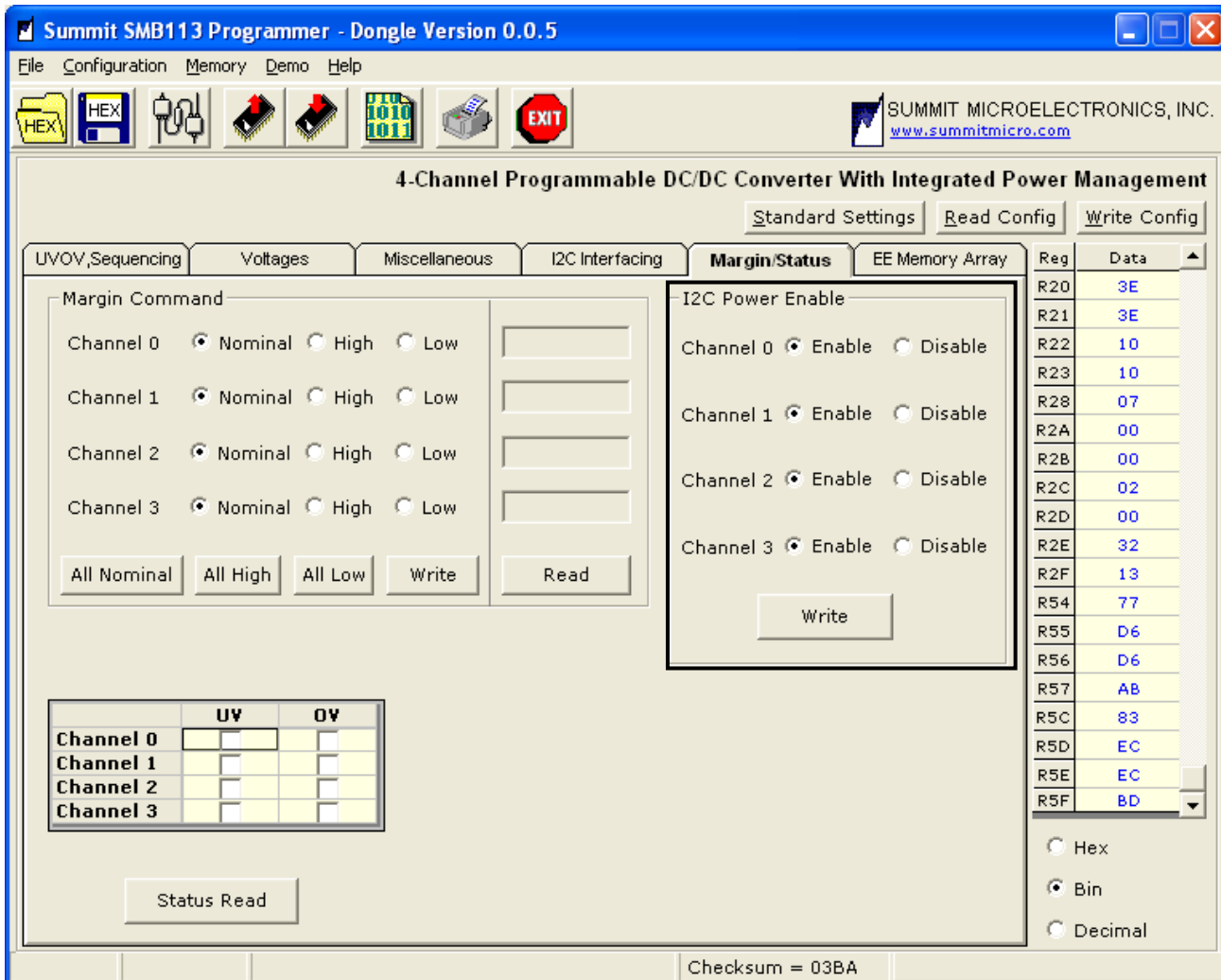


Figure 24: Register 90 is a volatile register used to enable and disable the output voltages when an I²C enable is selected. In the Normal-sequencing mode, the I²C Enable is disabled.

Figure:

Register 91 initiates the power on/off sequencing and clears the latched state of the internal UV1 register. When the SMB113A is in one of its three power on sequencing modes, it can be sequenced on or off by a write command to this registers. When the voltage on

the VBATT pin dips below the UV1 trip point the UV1 register bit will become latched. If a latched condition is not automatically cleared by dipping below the UV2 trip point, the register bit can be cleared by writing to the volatile register.

Register 91 Power on off control								Actions
D7	D6	D5	D4	D3	D2	D1	D0	
1	0	X	X	X	X	X	X	Power-ON
0	1	X	X	X	X	X	X	Power-OFF
X	X	X	X	1	X	X	X	Clear UV1

Table 35: Programmable Power on off control.

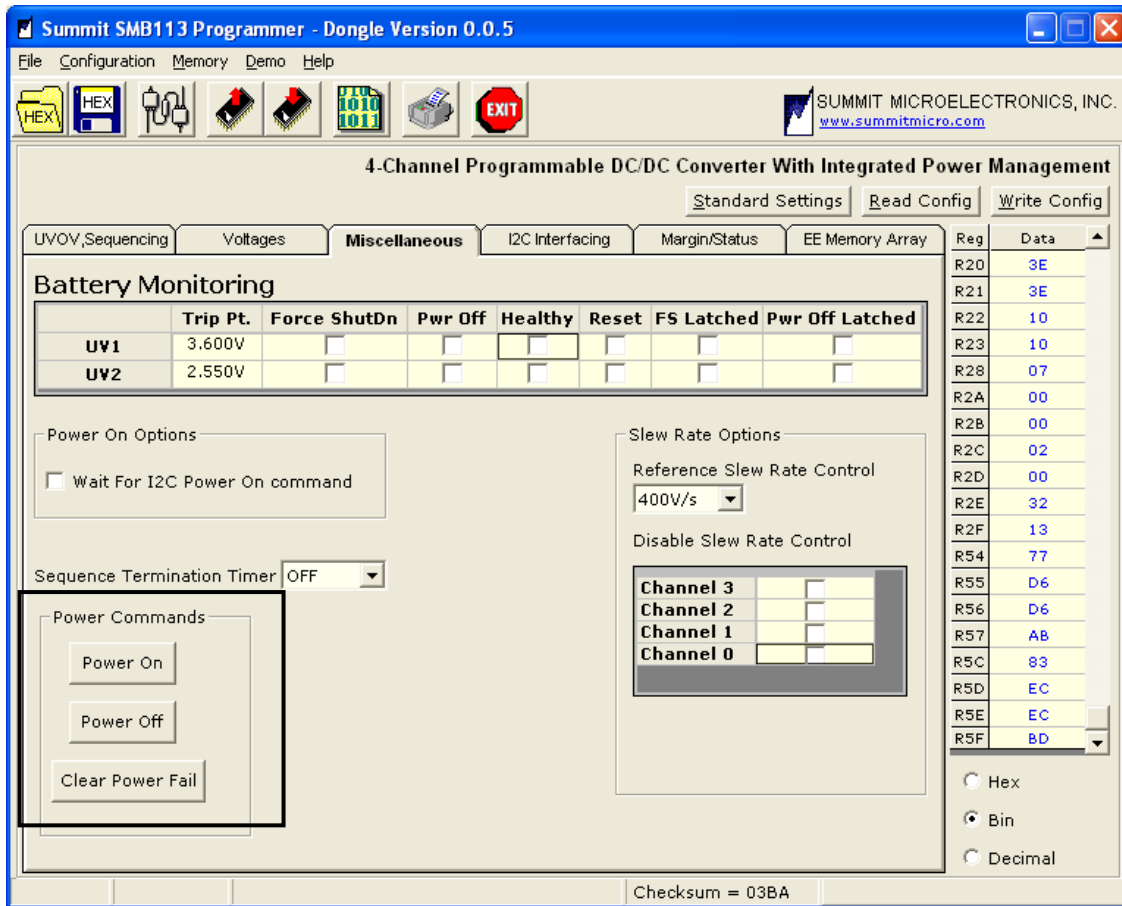


Figure 25: Register 91 is a volatile register used to commence an I²C Power on sequencing operation, it also contains a setting used to clear a latched condition in the UV1 volatile register.

Register 98 and 99 are non-volatile read only registers that contain information about the current state of the outputs. These registers can be read at any time and they will tell the user whether an OV or UV condition is present on any of the monitored output voltages.

When the supplies are off, they will show an under voltage condition because they are below the programmable UV threshold. When all supplies are on and within the programmed range, no OV or UV settings will be detected.

Register 98								volatile 2-byte read
D7	D6	D5	D4	D3	D2	D1	D0	Actions
X	X	X	X	X	X	X	X	First byte ignored

Table 36: Programmable sequence mode options.



Register 99								volatile 2-byte write
D7	D6	D5	D4	D3	D2	D1	D0	Actions
1	X	X	X	X	X	X	X	Channel 0 OV
X	1	X	X	X	X	X	X	Channel 0 UV
X	X	1	X	X	X	X	X	Channel 1 OV
X	X	X	1	X	X	X	X	Channel 1 UV
X	X	X	X	1	X	X	X	Channel 2 OV
X	X	X	X	X	1	X	X	Channel 2 UV
X	X	X	X	X	X	1	X	Channel 3 OV
X	X	X	X	X	X	X	1	Channel 3 UV

Table 37: Channel status register.

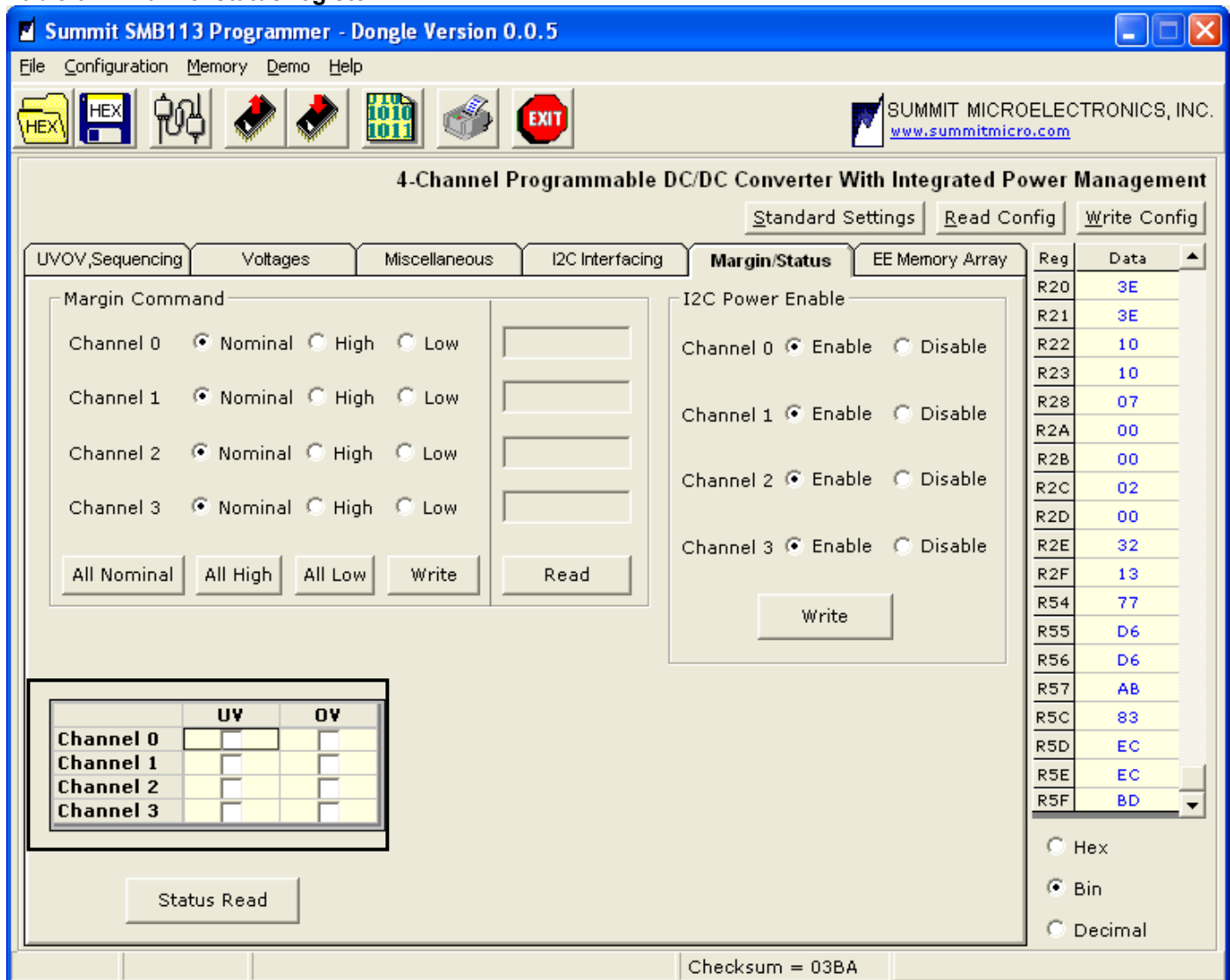


Figure 26: Registers 98 and 99 are volatile read only registers that contain the current state of the outputs.

Register 9C is a volatile margin control register. When a margin high or margin low operation is selected, the voltage on the COMP1 (channels 0-3) pin will be changed to reflect the value stored in the margin high or low threshold register.



Register 9C								Channel[0:3] Margin Control Register
D7	D6	D5	D4	D3	D2	D1	D0	Actions
1	1	X	X	X	X	X	X	Channel 3 Margin High 3 with 9D[7:6] = 11b
1	1	X	X	X	X	X	X	Channel 3 Margin Low 3 with 9D[7:6] = 10b
1	0	X	X	X	X	X	X	Channel 3 Margin High 2 with 9D[7:6] = 11b
1	0	X	X	X	X	X	X	Channel 2 Margin Low 2 with 9D[7:6] = 10b
0	0	X	X	X	X	X	X	Channel 2 Margin High 1 with 9D[7:6] = 11b
0	0	X	X	X	X	X	X	Channel 2 Margin Low 1 with 9D[7:6] = 10b

Table 38: Margin register.

Register 9D								Channel[0:3] Margin Control Register
D7	D6	D5	D4	D3	D2	D1	D0	Actions
1	1	X	X	X	X	X	X	Channel 3 Margin High
1	0	X	X	X	X	X	X	Channel 3 Margin Low
0	0	X	X	X	X	X	X	Channel 3 Margin Nominal
X	X	1	1	X	X	X	X	Channel 2 Margin High
X	X	1	0	X	X	X	X	Channel 2 Margin Low
X	X	0	0	X	X	X	X	Channel 2 Margin Nominal
X	X	X	X	1	1	X	X	Channel 1 Margin High
X	X	X	X	1	0	X	X	Channel 1 Margin Low
X	X	X	X	0	0	X	X	Channel 1 Margin Nominal
X	X	X	X	X	X	1	1	Channel 0 Margin High
X	X	X	X	X	X	1	0	Channel 0 Margin Low
X	X	X	X	X	X	0	0	Channel 0 Margin Nominal

Table 39: Output voltage control register used to switch between different outputs.

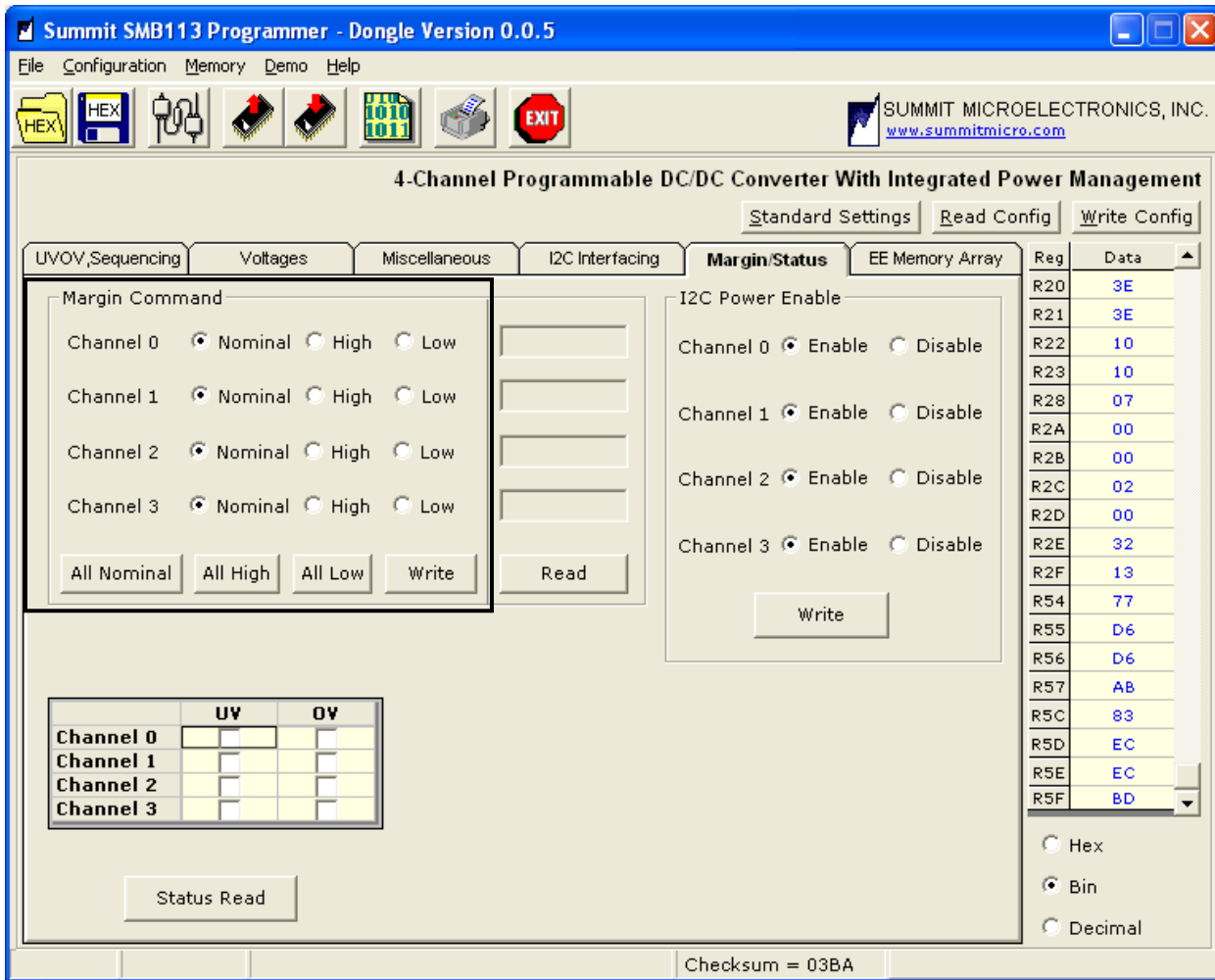


Figure 27: Register 9D is a volatile registers used to margin the output voltages to the margin high and margin low voltage settings.



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