Application Note 60

Achieving High Efficiency in a High-current Integrated Buck Switching Regulator

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Introduction

Many of today's modern mobile electronics require more power and higher current than ever before. Mobile electronics are becoming increasingly feature rich, and power hungry while at the same time, decreasing form factor size- creating a need for an integrated power management solution, that is compact and maintains high levels of efficiency. Upon first thought, one might simply decide to use their existing power management solution, and opt for larger MOSFETs with higher current ratings, and be done with it. Although one may get the current output desired, efficiency will surely take a significant hit. There are three major components in a switching regulator design that must be analyzed to see how they could possibly affect overall system efficiency in a high current application.

Those three components are the switching MOSFETs, output inductor, and output capacitor. This Application Note looks to analyze the effects and implementations of these three components in the SMB113A, a highly integrated, programmable, and flexible power manager. The SMB113A offers four synchronous buck channels, to achieve high efficiency with a high current output, in a platform, integrated solution, while the GUI allows for easy programming of the SMB113A, thereby simplifying and reducing overall system design time.

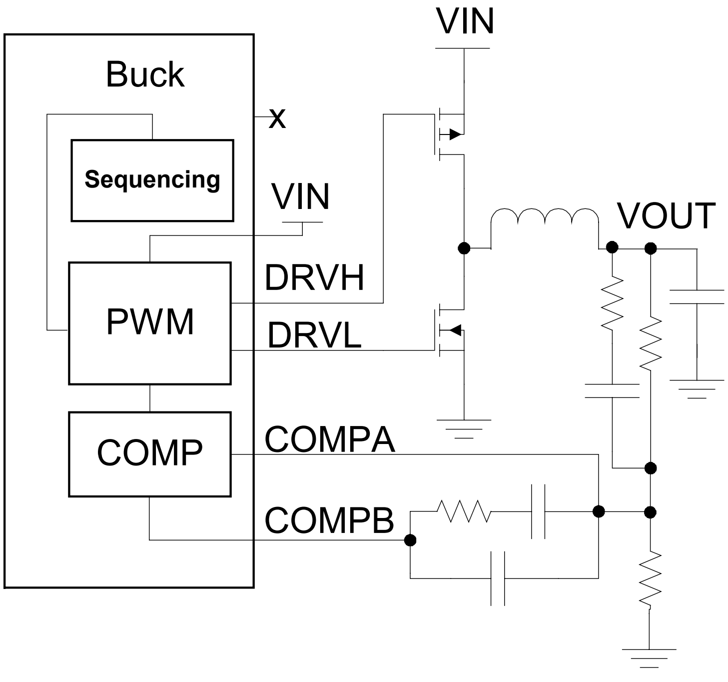

Figure 1: Simple Synchronous Buck Configuration

MOSFETs

The first and most important step in designing a high efficiency buck, switching regulator, is deciding what FETs to use, because most losses in a switching regulator are through the switch itself. In order to achieve a high level of efficiency, FETs with a very low $r_{DS(on)}$ and a relatively low gate charge, will want to be selected. The problem that inevitably arises is that for higher current applications, larger FETs must be selected, resulting in a higher gate charge. This problem is even more severe with the upper P-Channel FET as compared to the lower N-Channel FET, due to the fact that P-Channel FETs naturally have a higher gate charge and $r_{DS(on)}$ as compared to a comparable N-Channel FET. This gets worse as the FETs get larger, ultimately resulting in the upper P-Channel FET becoming a huge limiting factor in achieving a high efficiency design for a high current application. To alleviate this problem, the upper P-Channel FET is replaced with an N-Channel FET. As a general rule of thumb, if the $r_{DS(on)}$ of the P-Channel FET is starting to approach twice the value of the N-Channel FET, using a two N-Channel configuration is the best way to go.

The problem now becomes that the switch node is the source for the upper N-Channel FET, which should be switching between 0V and Vin. If the gate drive to the upper N-Channel FET is switching between 0V and Vin as well, then the FET could never turn on, because the gate to source threshold voltage is not being exceeded, or at least not enough to put the transistor into saturation. This problem is solved by using a bootstrap circuit to increase the drive of the upper N-Channel FET above Vdd, which is often achieved using an amplifier, bootstrap capacitor, and diode among other components. This, however, may not be too practical using discrete components, so available MOSFET drivers that have built in bootstrapping and will require only one input drive to be used is shown in Figure 2.

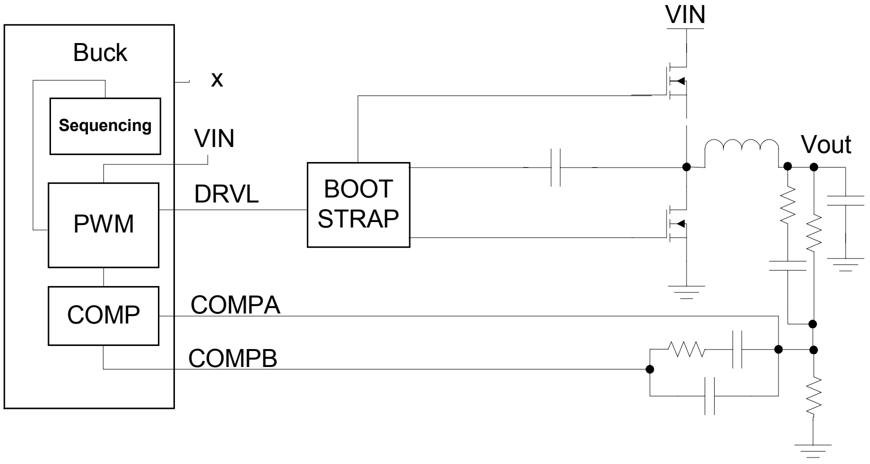

Figure 2: Buck Regulator with bootstrap implementation and two N-FETs

When selecting a FET, the sources of losses must be thoroughly analyzed. The sources of loss can be grouped into two main categories, switching losses and conduction losses. These two parameters can be simply quantified as seen below, and then summed, for the purpose of comparing FETs, to select the one that will yield the least amount of power loss.

$$P_{sw} = t_r V_{ds,\max} I_{Load} f_{sw} + \frac{C_{oss} V_{ds,\max}^2 f_{sw}}{2} + f_{sw} Q_g V_{drive}$$ (Equation 1. Switching Loss)

$$P_{Cond} = R_{DS(on)} I_{Load}^2 D_{\max}$$ (Equation 2. Conduction Loss)

t_r = Turn-On Rise Time
Q_g = Total Gate Charge
V_{drive} =Maximum Gate Driver Voltage
D_{max} = Maximum Duty Cycle
f_{sw} = Switching Frequency

C_{oss} = Output Capacitance
$V_{ds,max}$ = Maximum Vds, for PFET is |Vout-Vin|, for NFET is Vin

Another method of achieving a couple extra percents of efficiency is to connect a schottky diode across the lower N-Channel FET. This prevents the switch node from dropping below GND when switching the FETs and allowing the body diode to conduct, which will hurt efficiency. Once the switch node begins to drop below GND, the Schottky diode could clamp the voltage to ground. There are available N-Channel FETs designed specifically for this application that will have a schottky diode integrated into the package with the FET.

Inductor

The second component that must be accounted for in a high efficiency, high current design, is the inductor, the backbone of a switching regulator. Both physical size and inductance value carry a great deal of significance in the way the inductor affects overall system efficiency and stability. When choosing an inductor, the first thing to look for is whether it is temperature rise saturation current rated (at its most de-rated point) for your particular load application and operating frequency. If an inductor is chosen that is too small and without a high enough current rating, the inductor will saturate, causing core losses in overall switcher efficiency, by increasing I^2R losses due to large peak currents. In analyzing the areas for loss through an inductor, the sources can be grouped into three categories: Hysteresis loss, Eddy Current Loss, and copper loss. Hysteresis loss is essentially the loss incurred by switching the direction of the magnetic field each time the current through the inductor changes direction, and is dependent on the amount of turns in the inductor around the core, the core volume, and the switching frequency. Eddy Current loss occurs when current circulating the core induced by the magnetic field, begin to heat the inductor, forming heat losses. Copper losses are a type of resistive loss that is associated with the resistance of the windings and the DCR of the inductor, and will be the most significant source of losses through the inductor, assuming a proper core has been selected. Using a ferrite core, we may assume, as an estimate, that Hysteresis losses and Eddy Current losses may be neglected. These types of losses are generally very hard to quantify, and result in very little power loss as compared to copper losses, when using a ferrite core. DCR loss is best found by the following equations.

$$P_{D(ESR)} = I_{rms}^{2} R_{DCR}$$

(Equation 3. Inductor Power Loss)

$$I_{rms} = \sqrt{I_{LOAD}^{2} + \frac{\Delta I^{2}}{12}}$$

(Equation 4. RMS current through Inductor)

$$\Delta I = \frac{\left(V_{in} - V_{out}\right)D}{Lf_{SW}}$$

(Equation 5. Peak-Peak Current)

Output Capacitor

Finally, decreasing the inductor value to accommodate for larger currents, may affect the output ripple. The output capacitor has an equivalent series resistance or ESR associated with it, which adds an additional ripple component to the output. The two ripple components are actually out of phase with one another and the ESR component ripple is proportional to the inductor ramp current, which does not bode well in a high current design where the inductor ramp current can be very large. To limit this problem we increase the size of the output capacitor, which is inversely proportional to the ripple voltage but more importantly, we choose a capacitor, like a ceramic, with a low ESR to minimize the effects of large inductor ramp currents. Additionally, choosing a capacitor with low ESR will decrease your power loss as evident in Equation 6.

$$P_{D(ESR)} = I_{Ripple}^{2} R_{ESR}$$

(Equation 6. Output Capacitor Loss)

Conclusion

Using the preceding equations and design philosophies, an efficient, high current power management solution can be designed by selecting appropriate components. To calculate the approximate efficiency for the designed system, the losses are summed together and then divided by the output power, to calculate the estimated percent losses. Using these techniques, a buck switching regulator using a 4-Buck channel Summit Microelectronics SMB113A with input voltage of 5V, output voltage of 1V, a load current of 10Amps, and a switching frequency reduced to 400kHz as to reduce the amount of switching losses due to the higher gate charge MOSFETs, increased its efficiency at 10Amps from 66% to 83% and at 3Amps from 80% to 90%. This was accomplished, while at the same time maintaining a small form-factor in a highly integrated platform solution.

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