

Platform Solution for DDR SDRAM Power Management

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Introduction

In recent years, the most popular, and readily available solution for memory has been the JEDEC DDR SDRAM standard. The DDR (double-data-rate) standard offers superior performance compared to previous memory technologies such as single-data-rate SDRAM, because it transfers data on both the rising and falling edges of the clock signal. DDR is a comparable solution to many other alternatives such as Rambus RDRAM, however DDR is widely used and manufactured by numerous companies and is easy to integrate, whereas RAMBUS may be difficult to implement, and may therefore be impractical for most applications.

The problem that arises with the use of DDR SDRAM is that often times a separate DDR power regulator is required to manage the specific power requirements needed to properly operate the DDR SDRAM, adding both, extra cost and complexity to the design, as well as reducing overall system integration. This application note was written to show how DDR memory

can be integrated into a system, without the addition of a separate DDR power regulator. As an example, DDR memory shall be integrated into a system consisting of a Graphics Processing Unit, GPU, and a single device shall manage the power of both devices, creating a single, simple, platform solution.

The device that will be used to implement this platform solution is the Summit Microelectronics SMB113A, a highly integrated and flexible power manager, primarily used in a wide range of portable applications. The SMB113A integrates 4 synchronous buck converters, whose outputs are $\pm 1.5\%$ accurate or better using proprietary ADOC technology. Additionally, the SMB113A is versatile and easily configurable in part due to the use of the Windows based GUI that programs output voltages, margining, sequencing, power on/off options, and various monitoring and triggering features, among an abundance of others, thus simplifying and reducing development time.

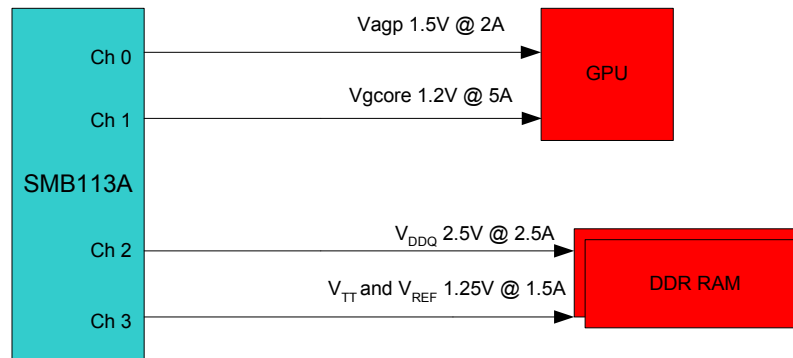


Figure 1: Typical Applications Block Diagram



Overview and Specifications

Currently there are two DDR SDRAM standards available on the market, DDR and DDR2, with a DDR3 standard currently in the works. All three run using the same basic power requirements for operation with a few notable exceptions, one of which being that DDR has an Output Supply Voltage, V_{DDQ} of 2.5V, DDR2 uses a V_{DDQ} of 1.8V and DDR3 is tentatively set to use 1.5V to help reduce power consumption. However, aside from that, all the DDR SDRAM's run using three Voltages, Output Supply Voltage, V_{DDQ} ; Input Reference Voltage, V_{REF} ; and Termination Voltage, V_{TT} . The rules that a DDR power converted must follow for proper operation are as follows:

- 1) $V_{REF} = 0.5 * V_{DDQ}$
- 2) V_{REF} must be able to track any variations in V_{DDQ}
- 3) V_{TT} must equal $V_{REF} \pm 40mV$
- 4) Ripple Voltage on V_{REF} must not exceed $\pm 2\%$
- 5) For DDR2, $V_{DD} = V_{DDL} = V_{DDQ}$
- 6) Power up voltage ramp < 20ms
- 7) Must be able to source and sink current

Implementation

Many of these requirements can already be satisfied using the SMB113A without any modifications or additions. To power the GPU, we assign Channel 0 of the SMB113A to output a voltage of 1.5V, and Channel 1 a voltage of 1.2V. Although the 1.2V

channel requires a significant amount of current, driving larger FETs to supply that current to the output is possible due to the strong drive capability of the SMB113A. For the memory, using DDR SDRAM as an example, we use Channel 2 of the SMB113A to supply $V_{DDQ} = 2.5V$ and Channel 3 to supply V_{TT} and $V_{REF} = 1.25V$, thus satisfying conditions one and three.

Using proper compensation values, as well as a 22 μF output ceramic capacitor in parallel with a 0.1 μF bypass ceramic capacitor, or other low ESR capacitors, will reduce the ripple on the output of the channels to satisfy condition four. As a general rule, the larger the capacitor and the lower the ESR, the better the output ripple will be.

To satisfy condition six, we make use of the programmable Slew Rate control via the Windows GUI to adjust the rate at which each channel of the power manager turns on. To meet the requirements, the Slew Rate should be set to either 200V/s or greater to achieve the desired power up time. The Slew Rate is dependent on the resistor divider of R1 and R2, therefore, increasing R1 (decreasing R2) will also increase the slew rate.

Additionally, the ability to source and sink current is done intrinsically due to the nature of the synchronous buck topology used by the SMB113A.

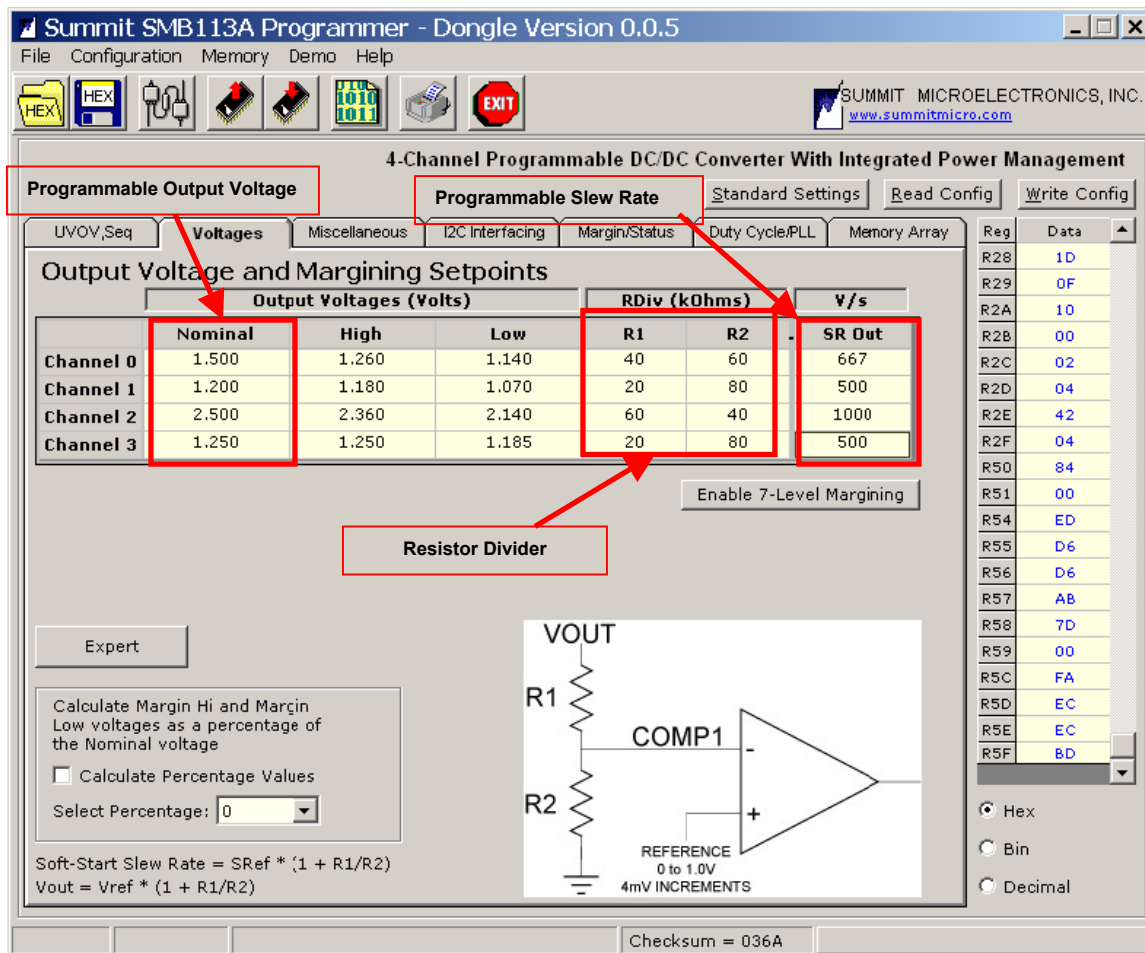


Figure 2: Programmable Output Voltage and Slew Rate using the Windows based GUI

The final requirement that must be satisfied is the condition that V_{REF} must be able to track any variations in V_{DDQ} . This is accomplished by the addition of a high-speed operational amplifier and a resistor divider, as seen in Figure 3.

The operational amplifier will serve to bypass the error amplifier within the SMB113. When configuring the amplifier, a reference voltage must be applied to the positive non-inverting input. This reference voltage will be a portion of the voltage V_{DDQ} to be tracked. While the V_{DDQ} voltage could be divided equally using a resistor divider with equal upper and lower resistors, to reduce the impedance of the negative terminal a 3:2 resistor divider ratio will be used. Assuming that we are using DDR, V_{DDQ} is 2.5V the 3:2 resistor ratio will result in a 1.0V reference at the non-inverting terminal of the operational amplifier. Next, the output of the tracked voltage, V_{REF} , is divided down from 1.25V to

1.0V using the 1:4 resistor internal to the SMB113A. By utilizing the internal resistor divider within the SMB113A we can effectively reduce the input impedance of the inverting terminal of the amplifier, subsequently reducing the impedance at this node and reducing the noise susceptibility of the converter.

Any variations to V_{DDQ} are “sensed” by the non-inverting terminal of the operational amplifier, which is then being “compared” to the divided down version of V_{REF} at the inverting terminal. The output of the amplifier is then fed into the comparator (COMP2), which internally adjusts the duty cycle to enable V_{REF} to track V_{DDQ} .

When selecting an operational amplifier it is critical that it can function Rail-to-Rail (within 50mV of either supply rail) -- and that the specified slew rate exceeds 100V/us.

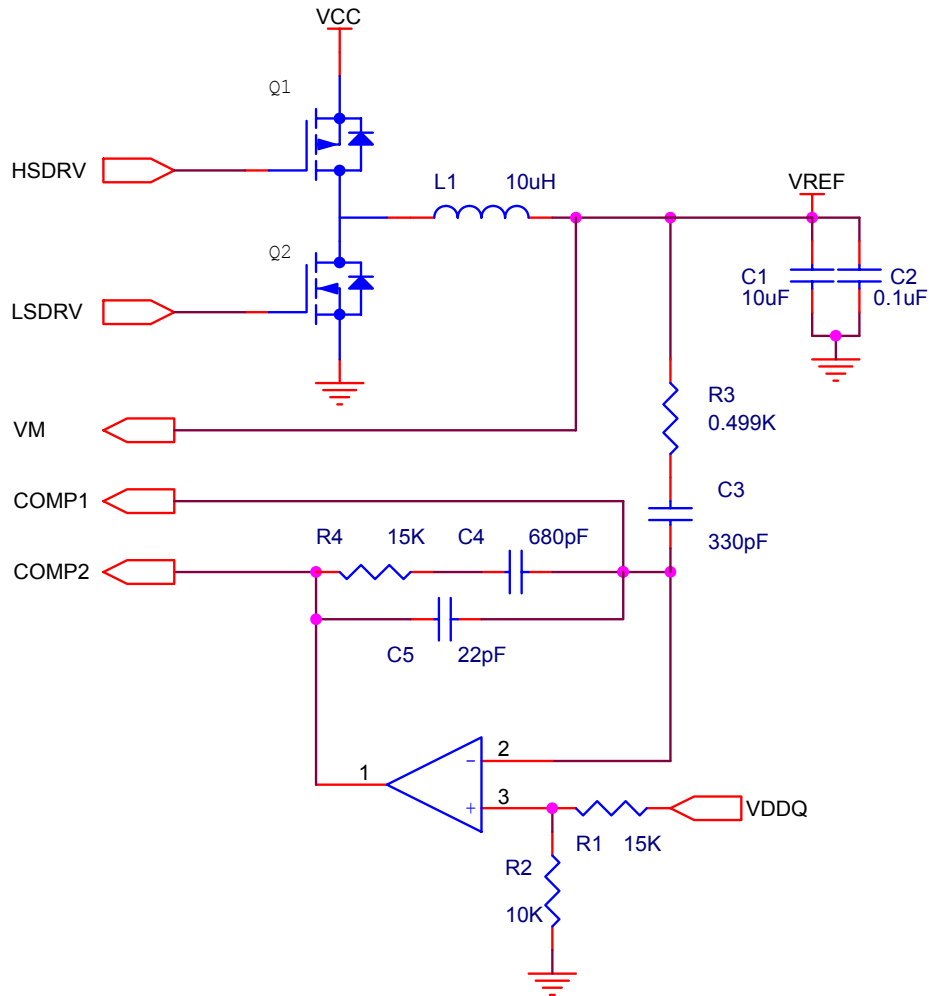


Figure 3: V_{DDQ} Variation tracking circuit

Conclusion

Through the addition of a single hi-speed Op-Amp, DDR compatibility was added to the Summit Microelectronics SMB113A integrated 4-channel synchronous buck power manager, while maintaining a high level of integration and simplicity and reducing

overall system cost. Using this technique it is possible to manage several devices, including a GPU and memory, as seen in Figure 1, using a single power manager, creating a highly integrated, simple and adaptable platform solution for most design needs.



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