SUMMIT MICROELECTRONICS

Application Note 51

SMM766/SMM766B Six-Channel Active DC Output Controller, Monitor, Marginer and Sequencer Windows GUI Users Guide and Configuration Register Descriptions

Introduction

The information contained in Application Note 51 details the Configuration Register settings for the SMM766/SMM766B six-channel supply monitor, controller and sequencer. The SMM766 Windows Graphical User Interface (GUI) is also shown with the associated register and function highlighted. For additional explanation on device functionality related to the configuration registers, refer to the SMM766 and SMM766B Data Sheets.

Register Formats and Functions

There are a total of 154 registers that are separated into five basic register types. The first are those that set a monitoring threshold where the binary value written to the register is used to compute an incremental voltage. The second type enables or disables a function or selects between two specific functions. The third register type allows selection of various timeout intervals or other values. These are not incremental, like the thresholds, but specific bit patterns select specific timer or other values. The fourth register types are volatile status registers that record device conditions. The fifth register type is a volatile Read/Write register that allows I^{2}C software power-on or power-off control of all SMM766/B channels. The device responds to two different slave addresses on the I^{2}C bus. The general-purpose memory responds to slave address 1010_{BIN} or 1011_{BIN}; the configuration and software registers respond to slave address 1010_{BIN} or 1011_{BIN}.

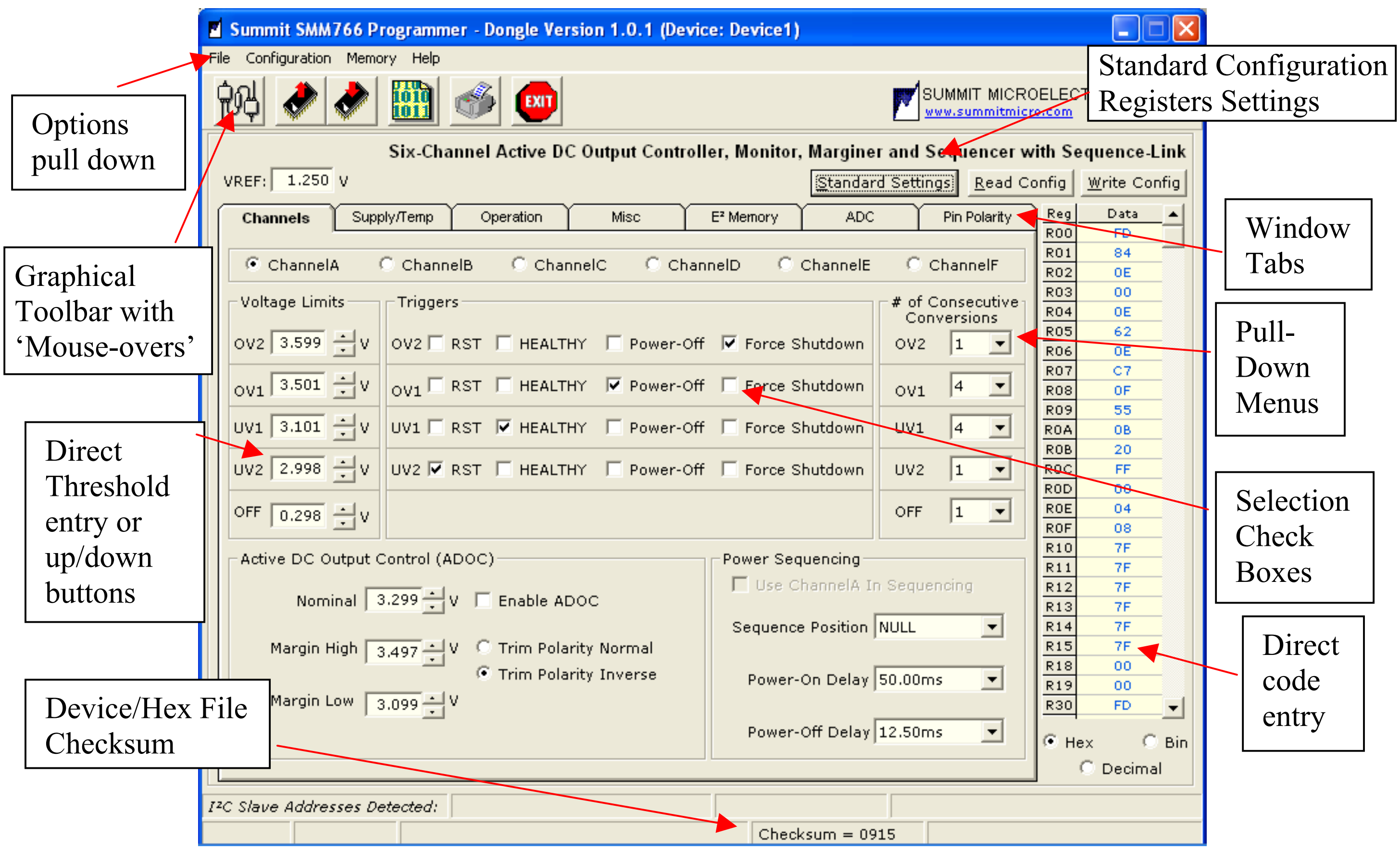

Figure 1 - SMM766 Windows GUI Features (also see figures 6, 7 and 8)

SMM766 Windows Graphical User Interface

The SMM766 Windows GUI (Figure 1) is used with the SMX3200 programming 'Dongle'. It is an easy to use Graphical Interface that is compatible with Windows 95, 98, NT, 2000 and XP operating systems. The GUI consists of pull-down menus, check boxes, up/down buttons, etc. There are "mouse-overs" that define every function and an expert mode for directly entering data into the configuration registers. The GUI generates a checksum that can compare the programmed device configuration register values versus the hex contents.

Help Menu

The Help menu can be used to view the SMM766 Datasheet or this app note while prototyping with the Windows GUI. The 'About' selection will show the GUI version number. Please always go to the Summit web site (www.summitmicro.com) to check for the most current data sheet and GUI software. There are also options if applicable, to View GUI change notices and to check the web site directly for the most current GUI version.

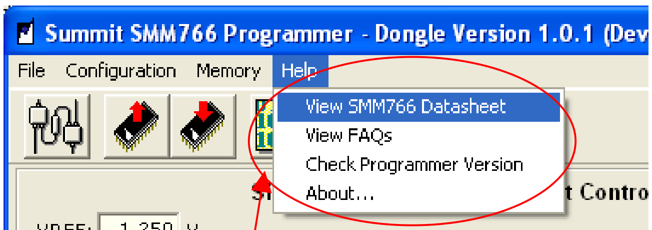

Figure 2 - Help Menu

Configuration Pull Down Menu

This menu (Figure 3A) has an option that will check status tracking code and communications between the device and the PC. This selection should be tried first before changing any options. If the test passes, then all other options can be left in the default condition. If it doesn't pass, check all SMX3200 cable connections to the board and PC. If correct, then slow the I^2C clock frequency as described in the Setup Options paragraph below.

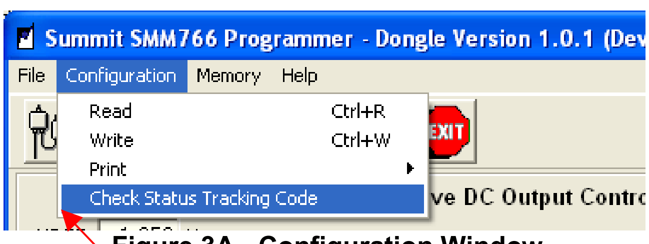

Figure 3A - Configuration Window

Setup Options

In the "File" pull-down menu (Figure 3B), there are options to set the I^2C clock frequency and delays before I^2C Read and Write operations. The default settings work with most PCs, so these settings are only for circumstances where the PC cannot communicate successfully with the SMX3200 programming 'Dongle'. The "Auto-Read Configuration/Memory After Write" check box enables a checksum test, which compares the GUI hex settings or file to the programmed device at the end of a Write sequence. It does this by performing a Read immediately following a Write.

Figure 4 shows the Settings Options Window which includes an additional control for the default state of Pin 6 of the dongle (MR# low or high)

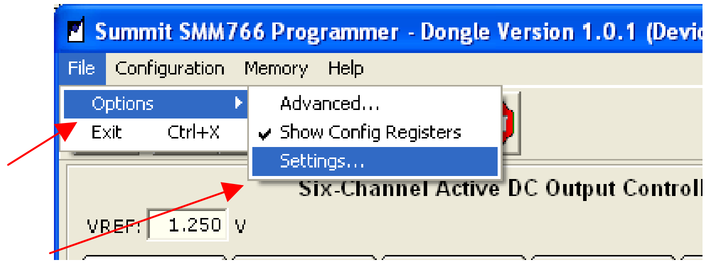

Figure 3B - Settings Window

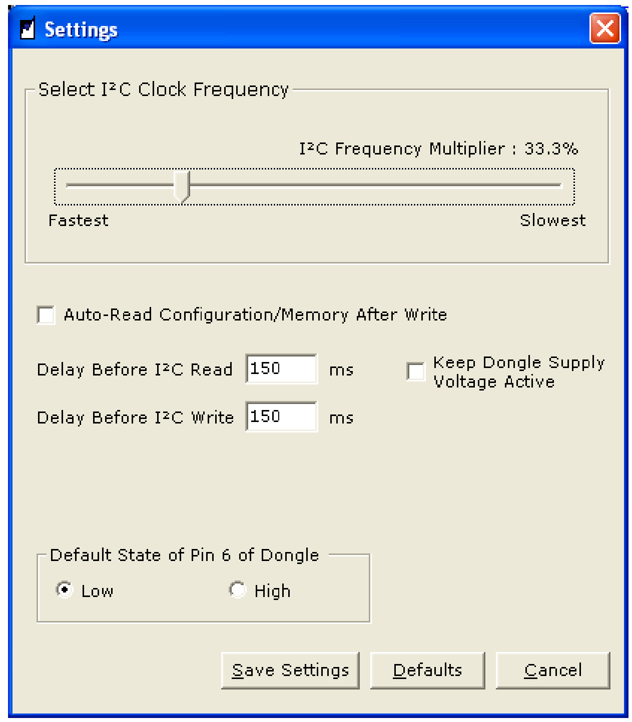

Figure 4 - Settings Options Window

Interfacing Options

The parallel Port Interfacing Window sets different options for programming the device. The 'Parallel Port' address check can verify if the address hex value is correct for the PC used for programming.

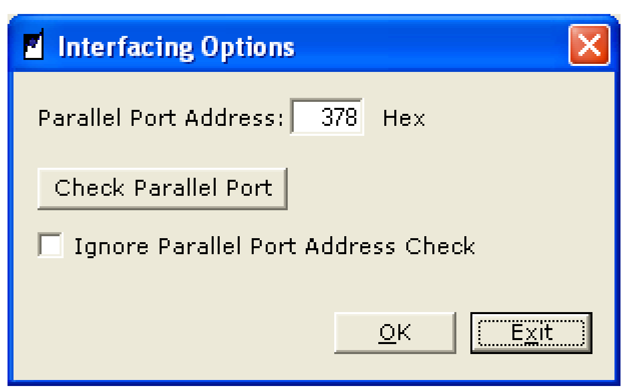

Figure 5 - Interfacing Options Window

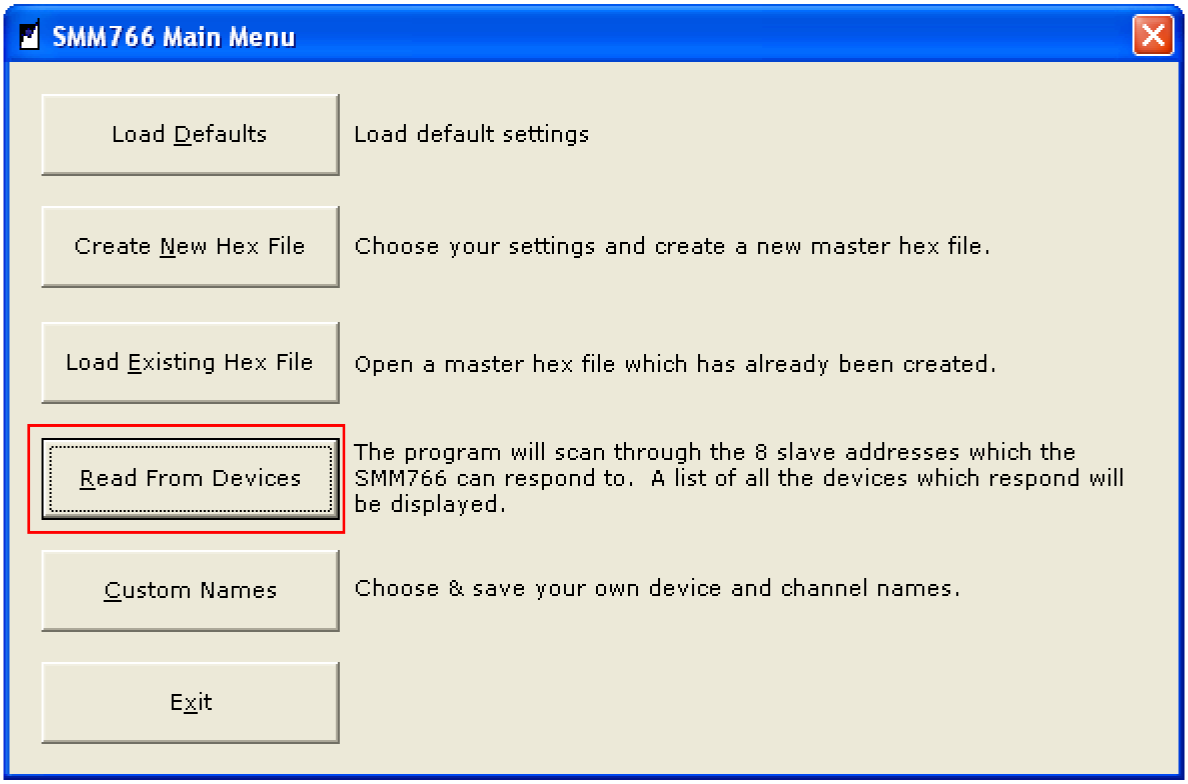

Figure 6: SMM766 Programmer Window with the ‘Read From Devices’ button clicked (see Figure 7).

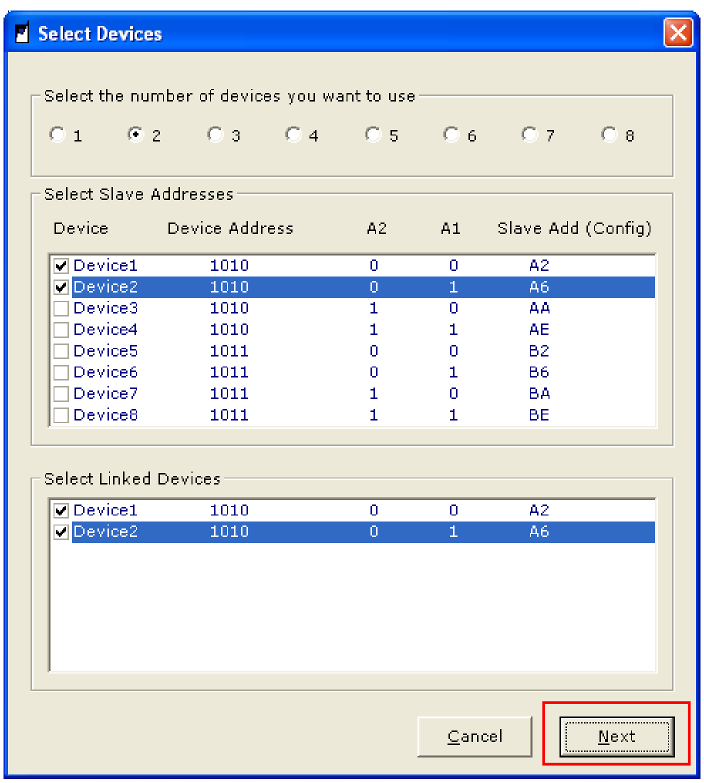

Figure 7: SMM766 ‘Select Devices’ Window opens after clicking ‘Read From Devices’ button (see Fig 6).

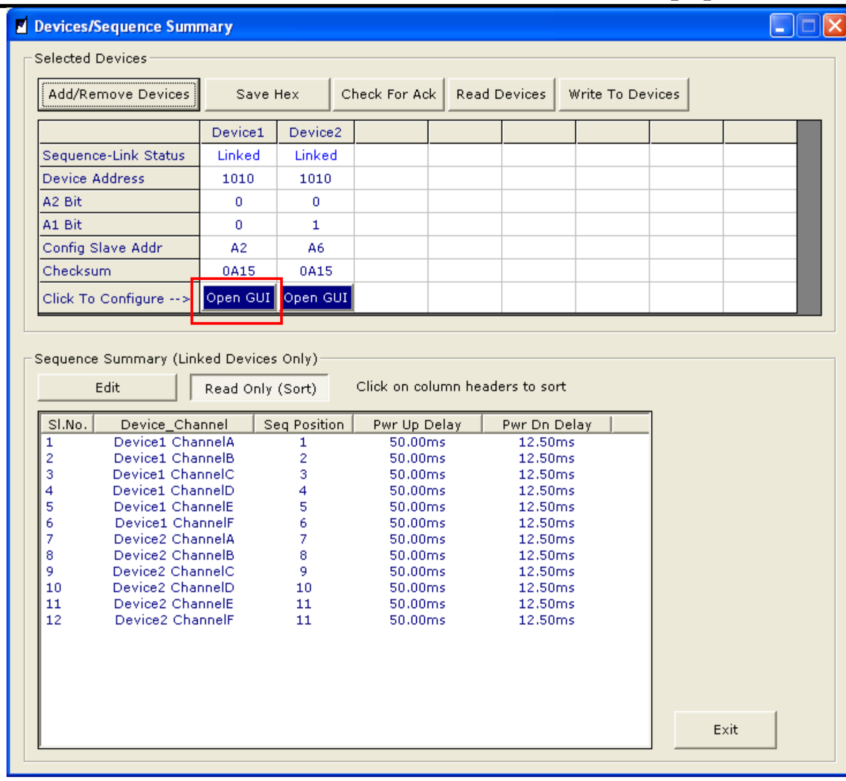

Figure 8: SMM766 'Devices/Sequence Summary' Window opens after clicking the 'Next' button (Fig 7).

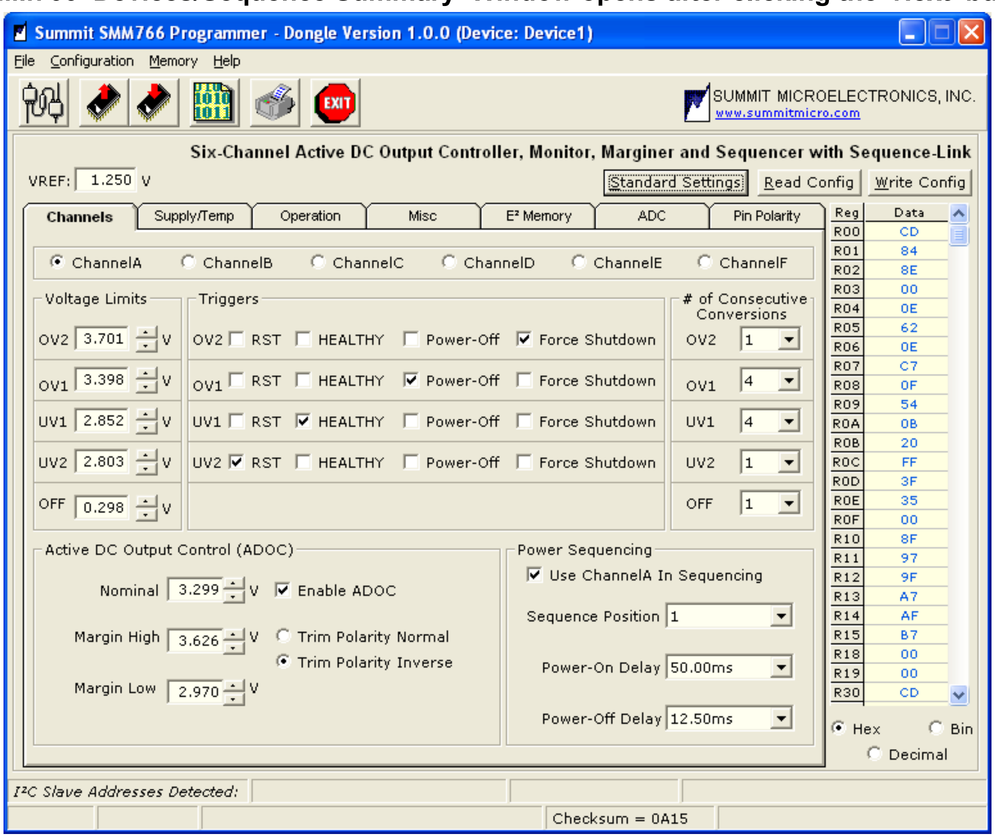

Figure 9: SMM766 Main Programmer Window opens after clicking the 'Open GUI' button (Fig 8).

The following registers are located at slave address 1010_{BIN}, bus address A2 11_{BIN} (A2 = 1_{BIN}) where A2 is either the A2 pin bias or 0 depending on the programmed selection. See register R0E, Fig 11.

Register R00 – Last sequence position plus 1 bits [3:0]. Must match R30[7:4] and R40[7:4]

Register R00[7:4]								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	0	0	0	X	X	X	X	Position 0 or 16
1	1	1	1	X	X	X	X	Position 15 or 31

Register R02 – Last sequence position plus 1 bit [4]. Must match R32[7] and R42[7]
Restart Mode (Number of retries before power off latch) – Must match R32[6:5] and R42[6:5]

Register R02[7:4]								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	X	X	X	X	X	X	X	Positions 16 to 31
1	X	X	X	X	X	X	X	Positions 0 to 15
X	0	0	X	X	X	X	X	Infinite re-tries
X	0	1	X	X	X	X	X	Latched after one fault-triggered power off
X	1	0	X	X	X	X	X	Latched after two fault-triggered power off
X	1	1	X	X	X	X	X	Latched after zero fault-triggered power off
X	X	X	D4	D3	X	X	X	Set these bits to zero

Register R00, R02, R04, R06, R08, R0A, R30, R32, R34, R36, R38, R3A, R40, R42, R44, R46, R48, R4A - ADOC Control Nominal, Margin High and Margin Low Voltage Settings
These registers (R00 through R4A) are combined with registers R01 through R4B to set the 10-bit ADOC Control voltage. An explanation that shows the formula for setting the ADOC Control voltage follows the register descriptions.

Register R00, R02, R04, R06, R08, R0A, R30, R32, R34, R36, R38, R3A, R40, R42, R44, R46, R48, R4A								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
X	X	X	X	1	1	X	X	X=1 VREF Multiplier (X)
X	X	X	X	1	0	X	X	X=0.75 VREF Multiplier (X)
X	X	X	X	0	1	X	X	X=0.50 VREF Multiplier (X)
X	X	X	X	0	0	X	X	X=0.25 VREF Multiplier (X)
X	X	X	X	X	X	C9	C8	Bits [9:8] of 10-bit ADOC Control Setting (see table below)

Register R01, R03, R05, R07, R09, R0B, R31, R33, R35, R37, R39, R3B, R41, R43, R45, R47, R49, R4B - ADOC Control Nominal, Margin High and Margin Low Voltage Settings
These registers are combined with the previous set of registers to set the ADOC Control voltage.

Register R01, R03, R05, R07, R09, R0B, R31, R33, R35, R37, R39, R3B, R41, R43, R45, R47, R49, R4B								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	C6	C5	C4	C3	C2	C1	C0	Bits [7:0] of 10-bit ADOC Control Setting

Example 1: Calculate the Nominal Voltage of Channel A:
Where: Y = Decimal value of [C9:C0] 10-bit ADOC Control Bits from Tables above (R00, R01)
X = VREF Multiplier from Table above.
VREF_CNTL = reference voltage on VREF_CNTL

Channel A ADOC Voltage = ((X ∗ VREF_CNTL) ∗ 1024))/Y
For these examples we use the standard settings on the SMM766 GUI
R00 = 0Dhex, R01= 83hex, VREF_CNTL= 1.250V

R00[3:2] = 11, so X = 1
R00[1:0] = 01, R01[7:0] = 83hex, so 10-bit ADOC Control Bits = 01 1000 0011bin
Y = 387

Channel A Nominal Voltage = ((1 ∗ 1.250) ∗ 1024))/387 = 3.307V

Example 2:
Calculate the Margin High Voltage of Channel C
R00 = 0Dhex, R34=0Ehex, R35=45hex, VREF_CNTL = 1.250
X = 1, 10-bit ADOC Control Bits = 10 0100 0101bin
Y = 581

Channel C Margin High Voltage = ((1 ∗ 1.250) ∗ 1024))/581 = 2.203V

The ADOC Control Reference Voltage bits (D[3:2]) of registers (R00 through R4A) are set using the following table:

If:	**Then = D[3:2]:**
ADOC Control Nominal Voltage > VREF_CNTL	11
VREF_CNTL > ADOC Control Nominal Voltage > 0.80∗VREF_CNTL	10
0.80∗VREF_CNTL > ADOC Control Nominal Voltage > 0.55∗VREF_CNTL	01
0.55∗VREF_CNTL > ADOC Control Nominal Voltage > 0.30∗VREF_CNTL	00

The ADOC Control Voltage setting bits (C[9:0]) are set using the following table:

If D[3:2] =:	**Then C[9:0] =:**
11	1024 ∗ VREF_CNTL / ADOC Control Voltage
10	1024 ∗ 0.75 ∗ VREF_CNTL / ADOC Control Voltage
01	1024 ∗ 0.50 ∗ VREF_CNTL / ADOC Control Voltage
00	1024 ∗ 0.25 ∗ VREF_CNTL / ADOC Control Voltage
For higher accuracy see registers R2A-R2F	

The following table lists the registers with their corresponding Channel and ADOC Control Mode:

Registers	**ADOC Control Setting**	**Registers**	**ADOC Control Setting**	**Registers**	**ADOC Control Setting**
R00:R01	Ch A – Nominal	R30:R31	Ch A – Margin High	R40:R41	Ch A – Margin Low
R02:R03	Ch B – Nominal	R32:R33	Ch B – Margin High	R42:R43	Ch B – Margin Low
R04:R05	Ch C – Nominal	R34:R35	Ch C – Margin High	R44:R45	Ch C – Margin Low
R06:R07	Ch D – Nominal	R36:R37	Ch D – Margin High	R46:R47	Ch D – Margin Low
R08:R09	Ch E – Nominal	R38:R39	Ch E – Margin High	R48:R49	Ch E – Margin Low
R0A:R0B	Ch F – Nominal	R3A:R3B	Ch F – Margin High	R4A:R4B	Ch F – Margin Low

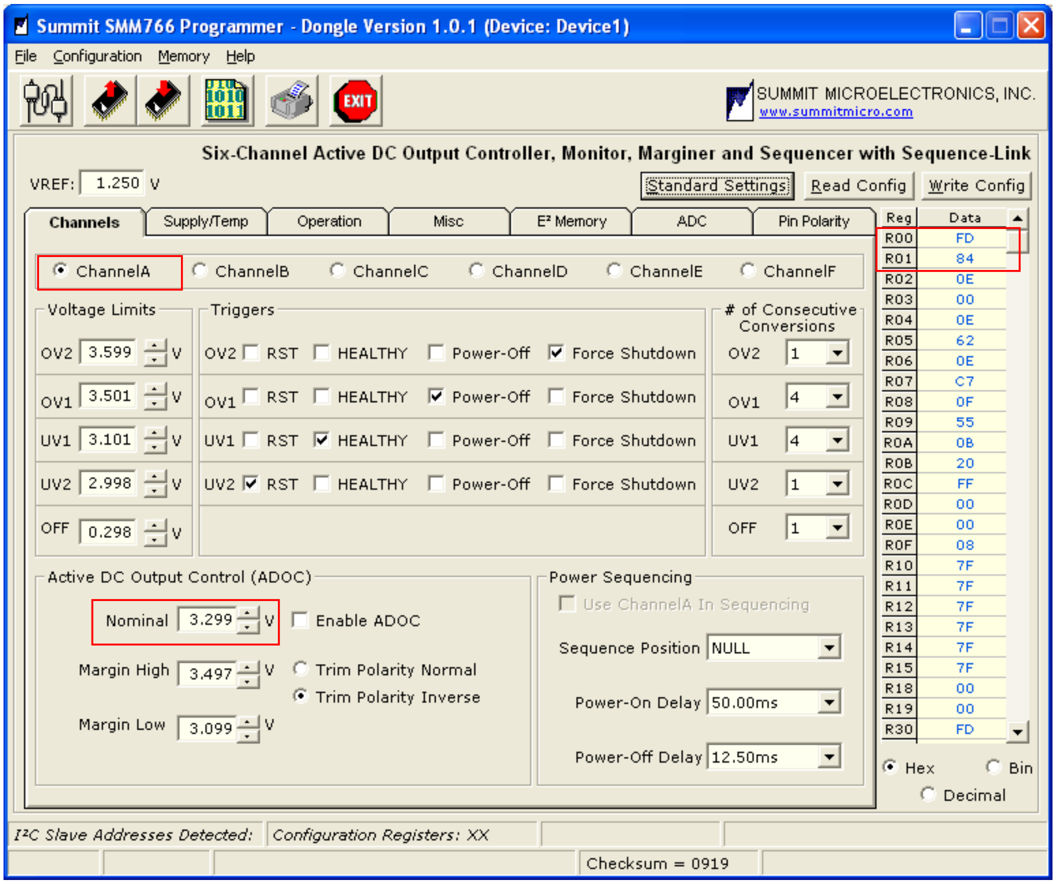

Figure 10 - Register R00, R01 Windows GUI Tab for Channel A

Register R0C - Internal Regulator Output, Fast Convergence, TRIMX Pin Polarity

Bit D[7] of this register selects the output voltage of the internal regulator powered by 12VIN. This voltage will power the SMM766/B if the voltage on the VDD pin is lower than this setting. Bit D[6] enables fast convergence to decrease the time it takes to change between nominal, margin high and margin low voltages. This remaining bits of this register individually selects the polarity of the TRIMX pins for use with different types of converters.

Register R0C								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	X	X	X	X	X	X	X	12VIN regulator output set to 5.5V
0	X	X	X	X	X	X	X	12VIN regulator output set to 3.6V
X	1	X	X	X	X	X	X	Enable Fast Convergence of ADOC Control
X	0	X	X	X	X	X	X	Disable Fast Convergence of ADOC Control
X	X	1	X	X	X	X	X	Channel F TRIMF pin polarity inverse
X	X	0	X	X	X	X	X	Channel F TRIMF pin polarity normal
X	X	X	1	X	X	X	X	Channel E TRIME pin polarity inverse
X	X	X	0	X	X	X	X	Channel E TRIME pin polarity normal
X	X	X	X	1	X	X	X	Channel D TRIMD pin polarity inverse
X	X	X	X	0	X	X	X	Channel D TRIMD pin polarity normal
X	X	X	X	X	1	X	X	Channel C TRIMC pin polarity inverse
X	X	X	X	X	0	X	X	Channel C TRIMC pin polarity normal
X	X	X	X	X	X	1	X	Channel B TRIMB pin polarity inverse
X	X	X	X	X	X	0	X	Channel B TRIMB pin polarity normal
X	X	X	X	X	X	X	1	Channel A TRIMA pin polarity inverse
X	X	X	X	X	X	X	0	Channel A TRIMA pin polarity normal

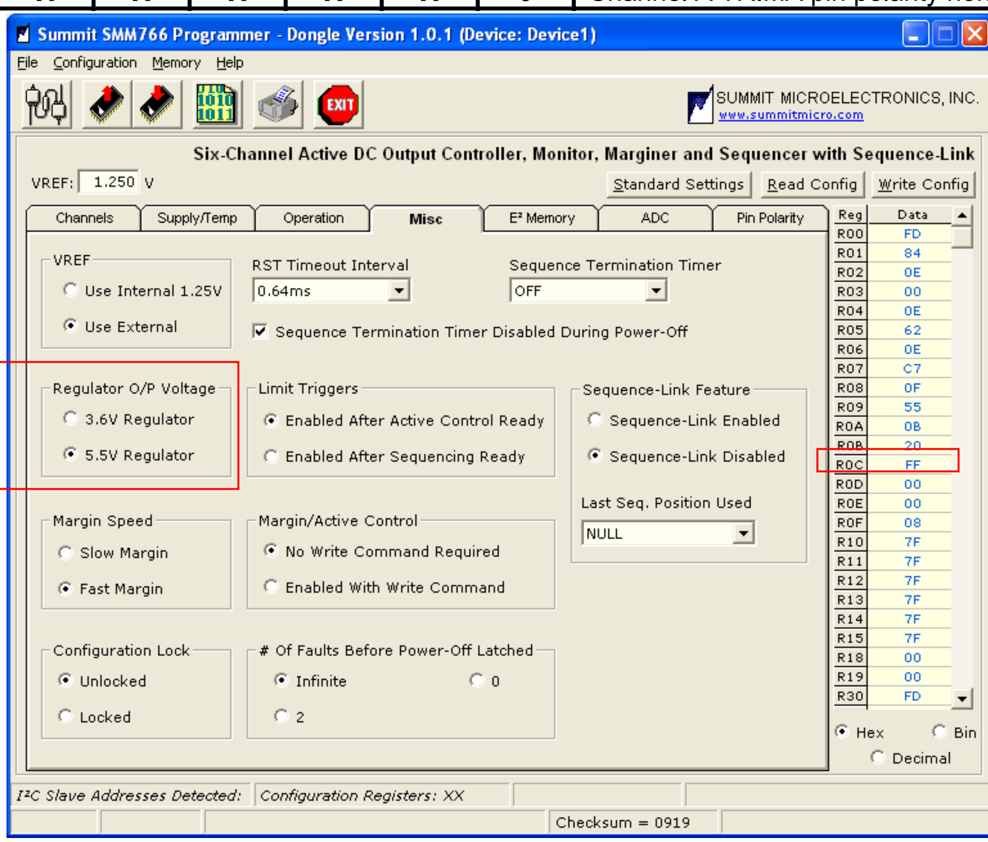

Figure 7 - Register R0C MISC Windows GUI Tab

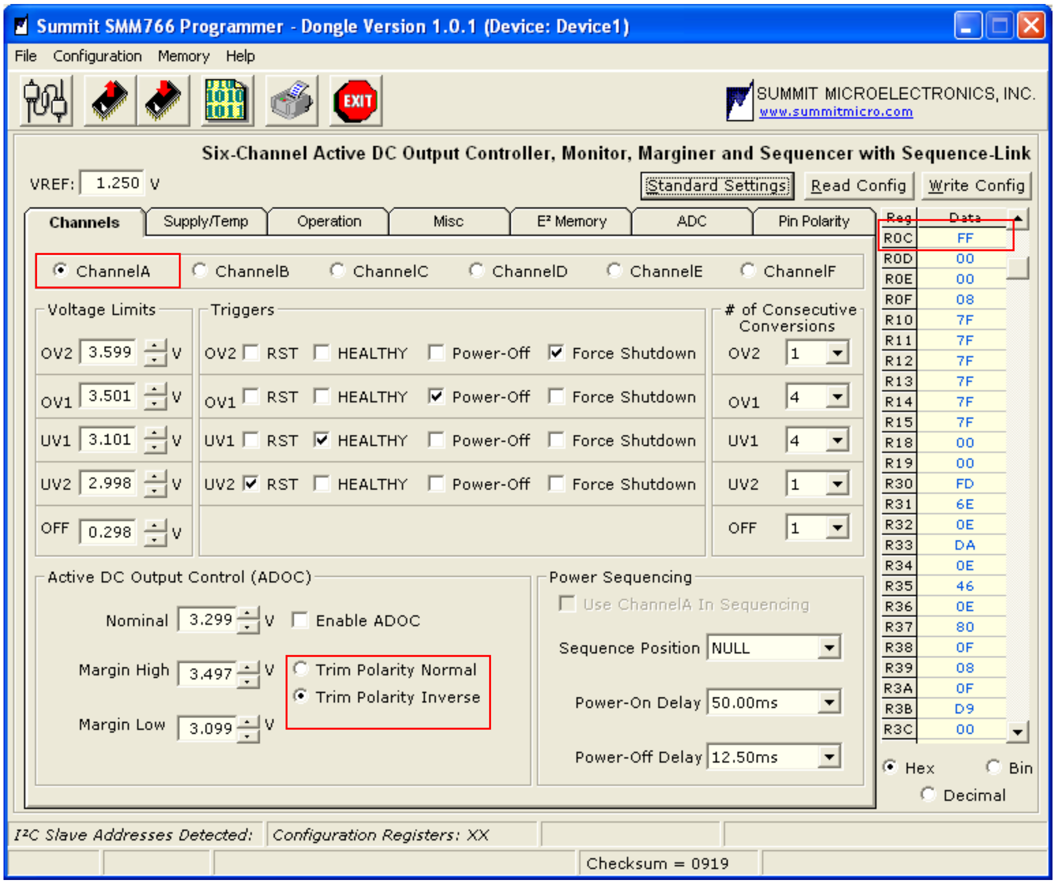

Figure 8 - Register R0C Windows GUI Tab

Register R0D – Configuration Register Lock, ADOC Control Enables

Bit D[7] of this register allows the configuration registers to be locked. Locking the configuration registers is irreversible and therefore this option cannot be selected using the GUI. This register also enables ADOC Control of each channel. The channel must be enabled for any ADOC Control (Nominal, Margin High, Margin Low).

Register R0D								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	X	X	X	X	X	X	X	Configuration registers locked (writes disabled)
0	X	X	X	X	X	X	X	Configuration registers unlocked (writes enabled)
X	X	1	X	X	X	X	X	Channel F ADOC Control enabled
X	X	0	X	X	X	X	X	Channel F ADOC Control disabled
X	X	X	1	X	X	X	X	Channel E ADOC Control enabled
X	X	X	0	X	X	X	X	Channel E ADOC Control disabled
X	X	X	X	1	X	X	X	Channel D ADOC Control enabled
X	X	X	X	0	X	X	X	Channel D ADOC Control disabled
X	X	X	X	X	1	X	X	Channel C ADOC Control enabled
X	X	X	X	X	0	X	X	Channel C ADOC Control disabled
X	X	X	X	X	X	1	X	Channel B ADOC Control enabled
X	X	X	X	X	X	0	X	Channel B ADOC Control disabled
X	X	X	X	X	X	X	1	Channel A ADOC Control enabled
X	X	X	X	X	X	X	0	Channel A ADOC Control disabled

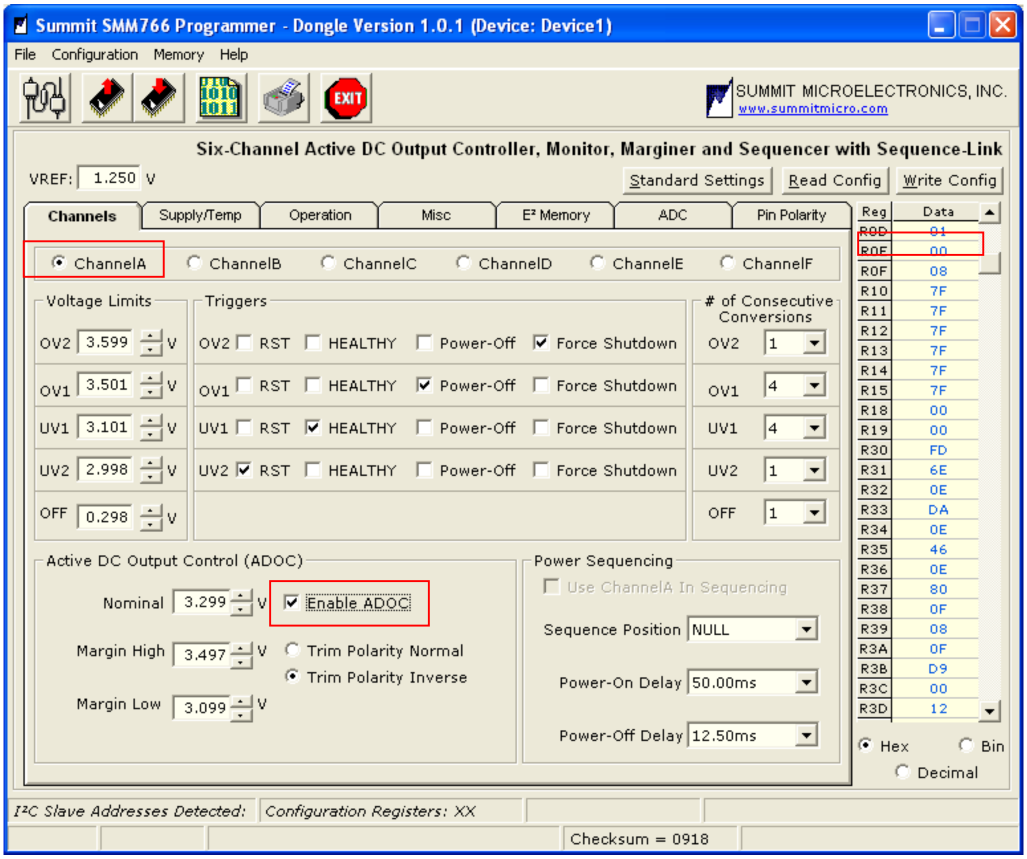

Figure 9 - Register R0D Windows GUI Tab

Register R0E – Sequence Termination Timer, Reset Timeout, Slave Address, Bus Address Bits

Bits D[7:6] of this register set the Sequence Termination Timer which shuts down the PUP outputs if the timeout is exceeded. The register also sets the Reset Timeout Period with bits D[5:4]. The bus address [A2 A1 A0] of the SMM766/B is set by bits D[2:0] of this register.

Register R0E								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	1	X	X	X	X	X	X	Sequence Termination Timeout = 400ms
1	0	X	X	X	X	X	X	Sequence Termination Timeout = 200ms
0	1	X	X	X	X	X	X	Sequence Termination Timeout = 100ms
0	0	X	X	X	X	X	X	Sequence Termination Timer OFF
X	X	1	1	X	X	X	X	Reset Timeout = 200ms
X	X	1	0	X	X	X	X	Reset Timeout = 100ms
X	X	0	1	X	X	X	X	Reset Timeout = 25ms
X	X	0	0	X	X	X	X	Reset Timeout = 0.64ms
X	X	X	X	1	X	X	X	Slave Address = 1011BIN
X	X	X	X	0	X	X	X	Slave Address = 1010BIN
X	X	X	X	X	1	X	X	Bus Address Bit A2 = A2 Pin
X	X	X	X	X	0	X	X	Bus Address Bit A2 = 0
X	X	X	X	X	X	1	X	Bus Address Bit A1 = 1
X	X	X	X	X	X	0	X	Bus Address Bit A1 = 0
X	X	X	X	X	X	X	1	Bus Address Bit A0 = 1
X	X	X	X	X	X	X	0	Bus Address Bit A0 = 0

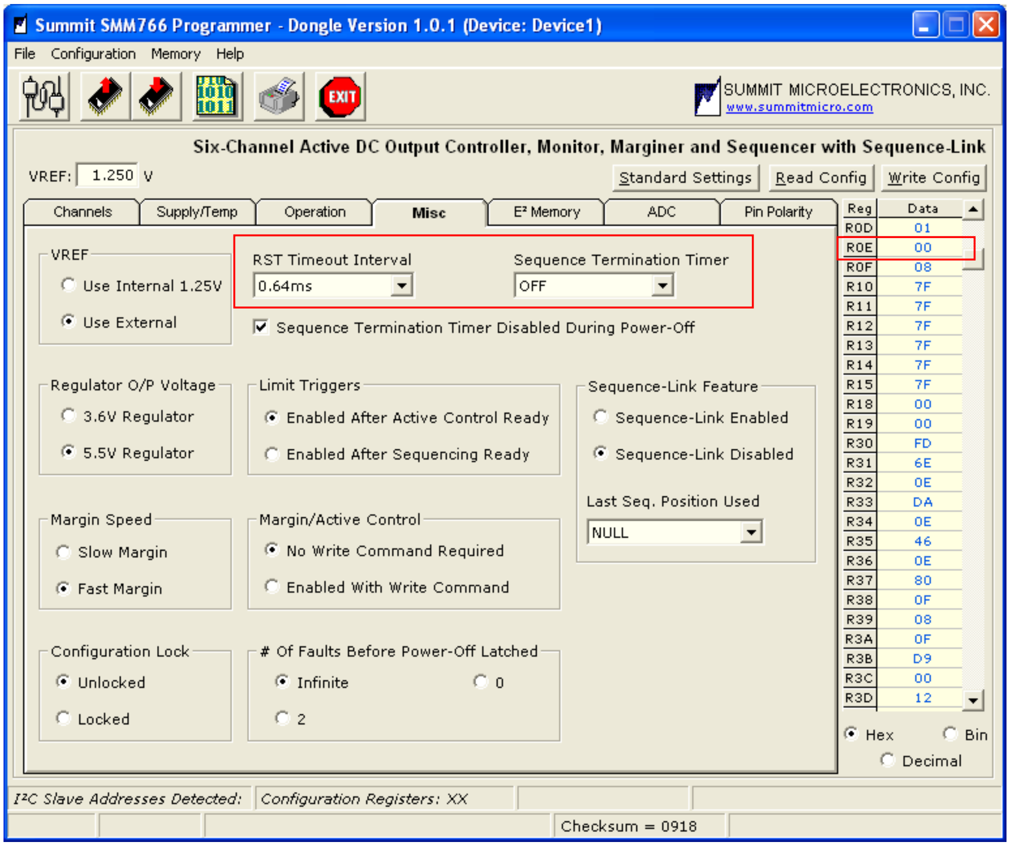

Figure 10 - Register R0E MISC Windows GUI Tab

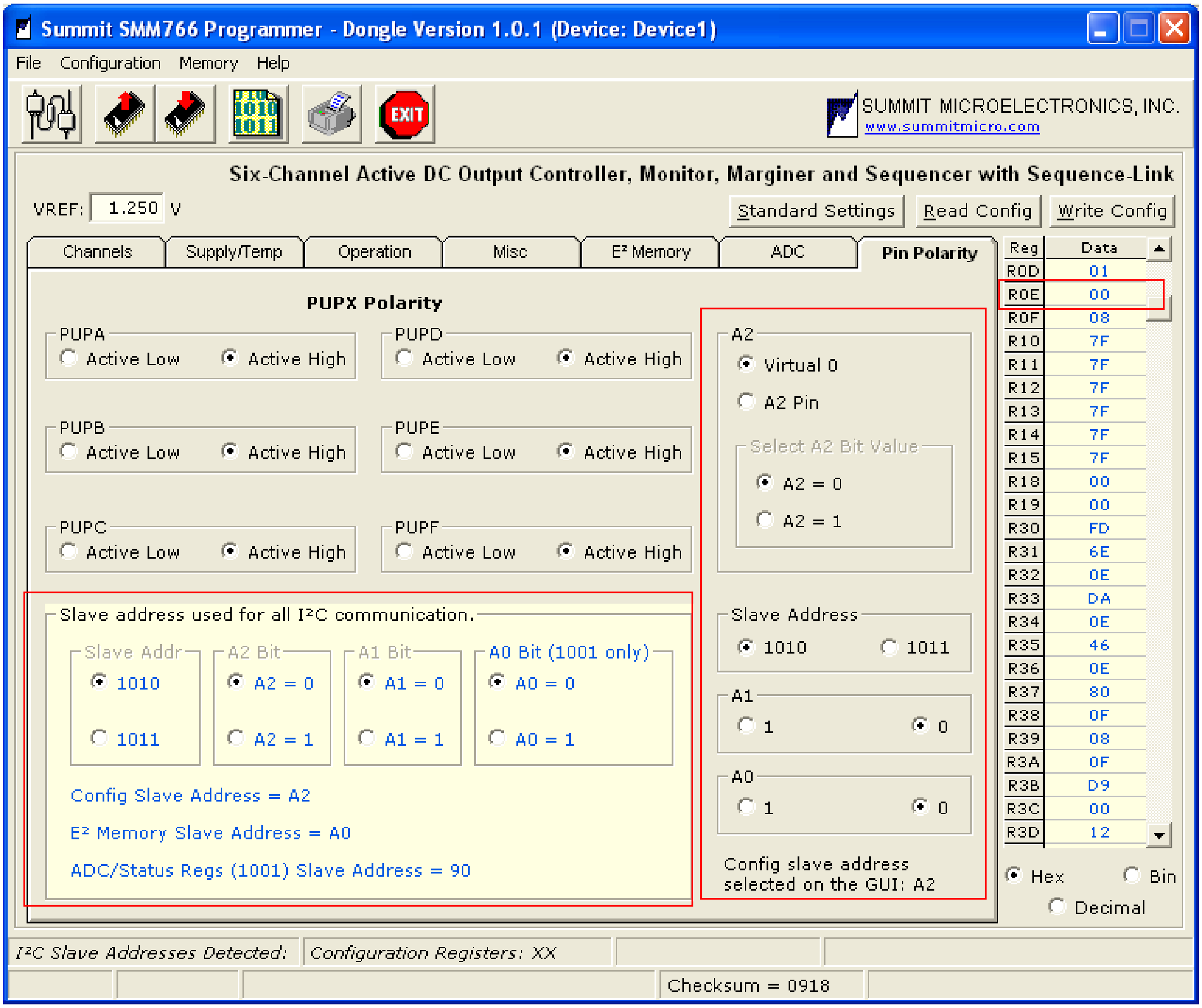

Figure 11 - Register R0E Pin Polarity Windows GUI Tab

Register R0F – ADOC Control Reference Voltage, ADOC Control Command, Automonitor Actions Enable, Link Enabled, Power-Off Sequence Termination, Preconditions for Power-On

Bit D[7] of this register selects the internal or external reference for the VREF_CNTL pin. As an option, the ADOC function may be always enabled upon power-up or require a write command to begin the process. This choice is made by Bit D[6]. The default setting is ‘No Write Command Required’ meaning ADOC begins upon power-up. bit D[4] is not used and set to zero. The Sequence Link feature is selected using bit D[3]. Bit D[2] will disable the Sequence Termination Timer during a Power-Off sequence. Bits D[1:0] enable precursors to the Power-On operation.

Register R0F								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	**X**	**X**	**X**	**X**	**X**	**X**	**X**	ADOC Control Reference Voltage from internal 1.25V reference connected to VREF_CNTL
0	**X**	**X**	**X**	**X**	**X**	**X**	**X**	ADOC Control Reference Voltage provided externally
X	**1**	**X**	**X**	**X**	**X**	**X**	**X**	ADOC Control command required for Active Control
X	**0**	**X**	**X**	**X**	**X**	**X**	**X**	No ADOC Control command required for Active Control
X	**X**	**1**	**X**	**X**	**X**	**X**	**X**	Automonitor actions (FS, Power-Off, RST, HEALTHY) enabled after sequencing completed
X	**X**	**0**	**X**	**X**	**X**	**X**	**X**	Automonitor actions (FS, Power-Off, RST, HEALTHY) enabled after ADOC Control convergence completed
X	**X**	**X**	**0**	**X**	**X**	**X**	**X**	Set this bit to zero
X	**X**	**X**	**X**	**1**	**X**	**X**	**X**	Sequence-Link Enabled
X	**X**	**X**	**X**	**0**	**X**	**X**	**X**	Sequence-Link Disabled
X	**X**	**X**	**X**	**X**	**1**	**X**	**X**	Sequence Termination allowed during Power-Off
X	**X**	**X**	**X**	**X**	**0**	**X**	**X**	Sequence Termination not allowed during Power-Off
X	**X**	**X**	**X**	**X**	**X**	**1**	**X**	Wait for 12VIN within limits before Power-On allowed
X	**X**	**X**	**X**	**X**	**X**	**0**	**X**	Don’t wait for 12VIN within limits before Power-On allowed
X	**X**	**X**	**X**	**X**	**X**	**X**	**1**	Wait for VDD within limits before Power-On allowed
X	**X**	**X**	**X**	**X**	**X**	**X**	**0**	Don’t wait for VDD within limits before Power-On allowed

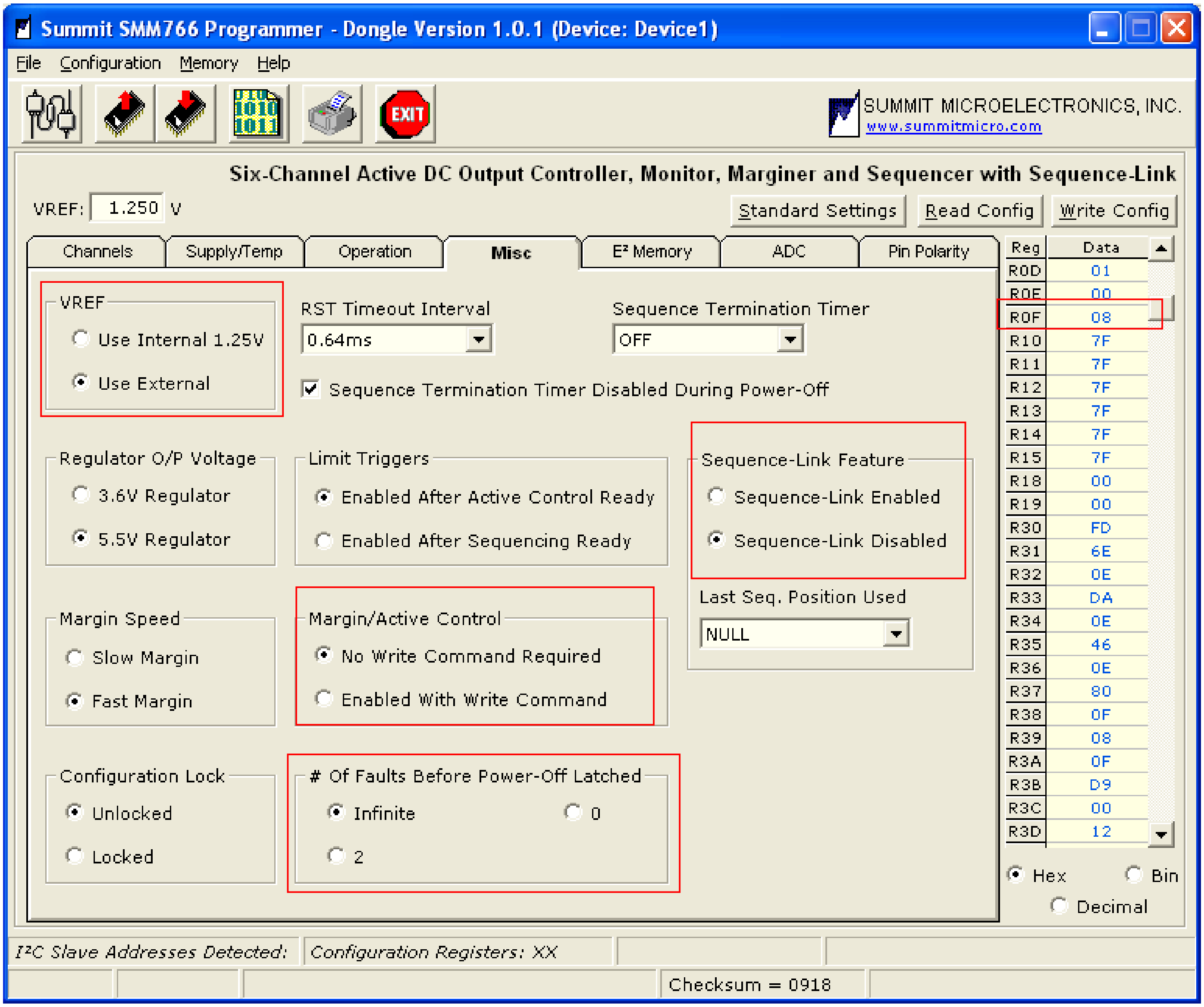

Figure 12 - Register R0F Windows GUI Tab

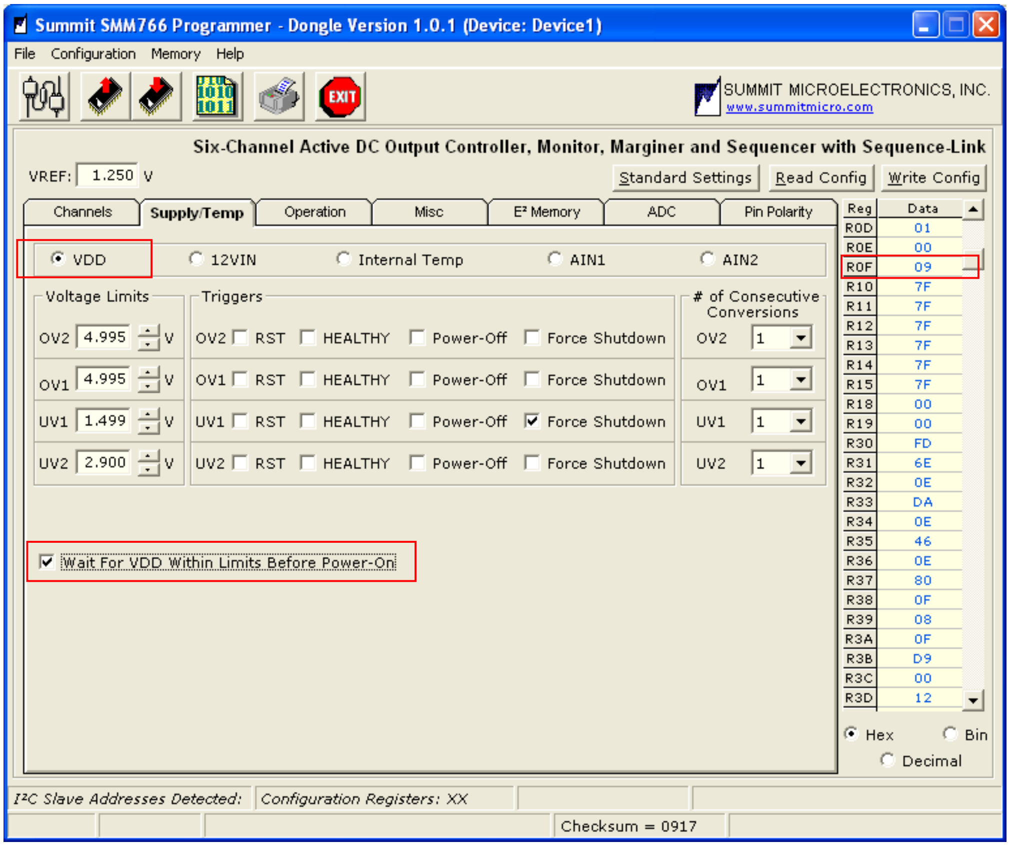

Figure 13 - Register R0F Supply/Temp Windows GUI Tab

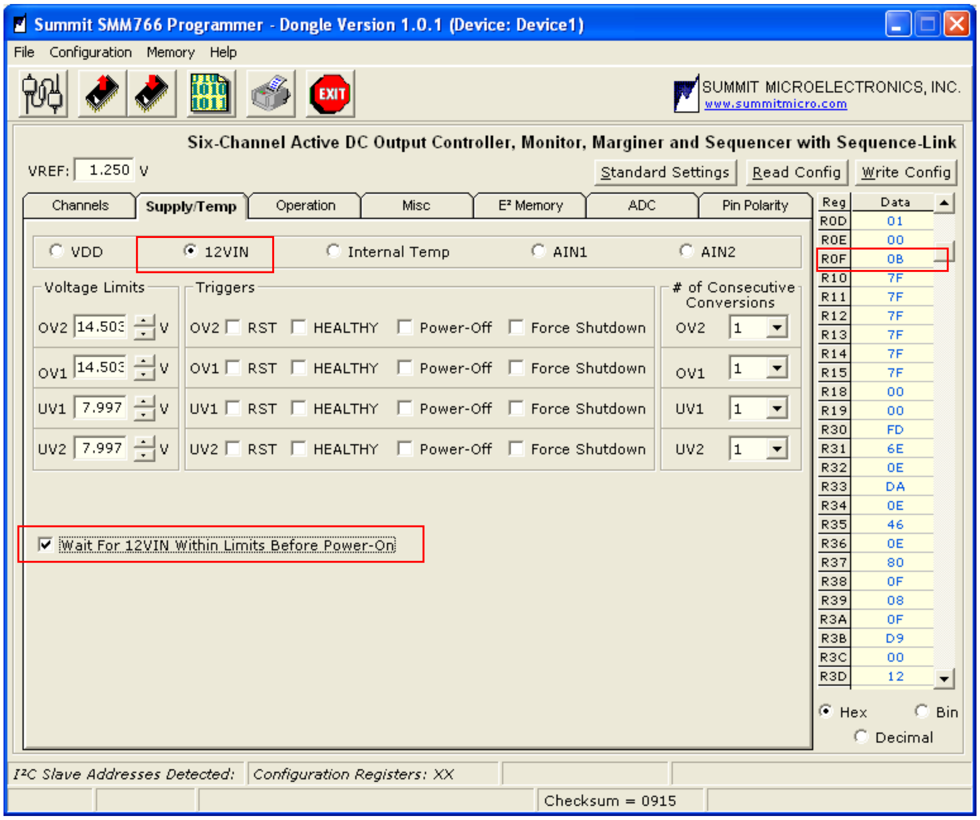

Figure 14 - Register R0F Supply/Temp Windows GUI Tab

Register R10, R11, R12, R13, R14, R15 – Sequence Position, Power-On and Power-Off Delays

Bits D[7:3] set the Sequence Position of the channel. The Power-On delays are set by bits D[2:1] and the Power-Off delays are set by bit D[0].

Register R10, R11, R12, R13, R14, R15								
D7	D6	D5	D4	D3	D2	D1	D0	Action
1	0	0	0	1	X	X	X	Channel X Sequence Position = 1
1	0	0	1	0	X	X	X	Channel X Sequence Position = 2
1	0	0	1	1	X	X	X	Channel X Sequence Position = 3
1	1	0	1	0	X	X	X	Channel X Sequence Position = 10
1	1	1	1	1	X	X	X	Channel X Sequence Position = 15
0	0	0	0	0	X	X	X	Channel X Sequence Position = 16
0	0	0	0	1	X	X	X	Channel X Sequence Position = 17
0	1	1	0	1	X	X	X	Channel X Sequence Position = 29
0	1	1	1	1	X	X	X	Channel X Sequence Position = NULL
X	X	X	X	X	0	0	X	Channel X Power-On Delay = 0.64ms
X	X	X	X	X	0	1	X	Channel X Power-On Delay = 12.5ms
X	X	X	X	X	1	0	X	Channel X Power-On Delay = 25ms
X	X	X	X	X	1	1	X	Channel X Power-On Delay = 50ms
X	X	X	X	X	X	X	1	Channel X Power-Off Delay = 12.5ms
X	X	X	X	X	X	X	0	Channel X Power-Off Delay = 0.64ms

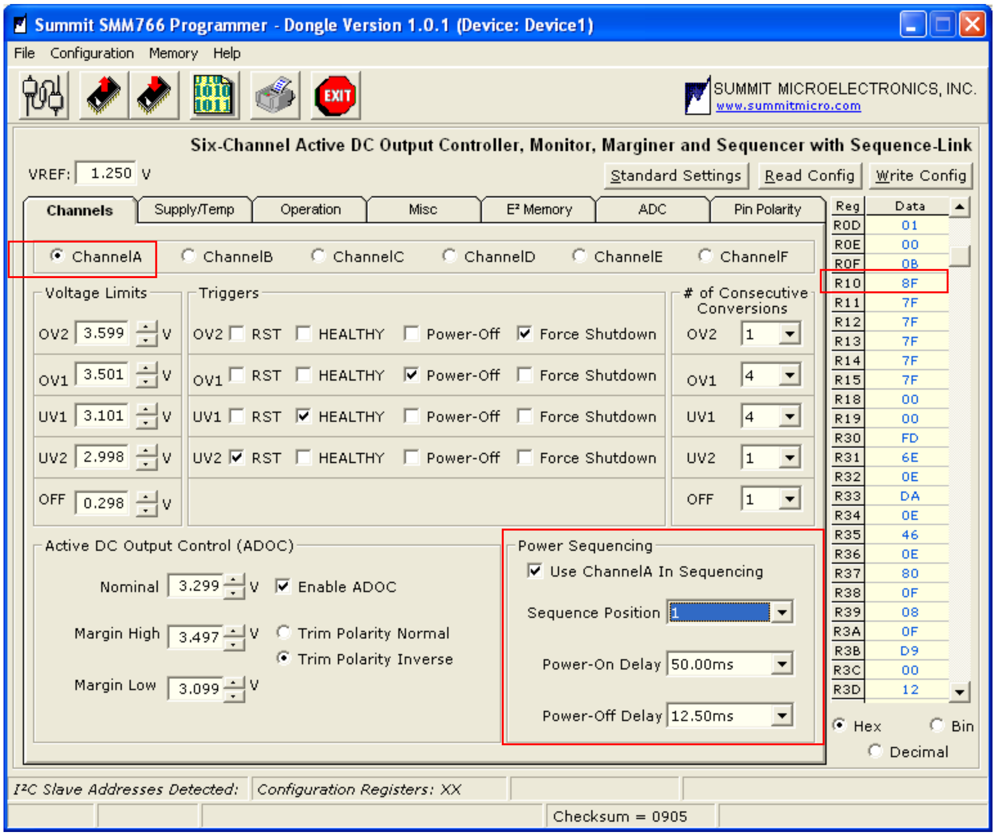

Figure 15 - Register R10 Channels Windows GUI Tab

Register R18, R1A, R1C, R1E – ADOC Control Commands for Channels A, B and C

Writing to any of these registers constitutes a ADOC Control Command. This command initiates control of Channels A, B and C to the desired ADOC Control Mode voltage.

Register R18, R1A, R1C, R1E								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
X	X	1	1	X	X	X	X	Channel A ADOC Control Margin High
X	X	1	0	X	X	X	X	Channel A ADOC Control Margin Low
X	X	0	X	X	X	X	X	Channel A ADOC Control Nominal
X	X	X	X	1	1	X	X	Channel B ADOC Control Margin High
X	X	X	X	1	0	X	X	Channel B ADOC Control Margin Low
X	X	X	X	0	X	X	X	Channel B ADOC Control Nominal
X	X	X	X	X	X	1	1	Channel C ADOC Control Margin High
X	X	X	X	X	X	1	0	Channel C ADOC Control Margin Low
X	X	X	X	X	X	0	X	Channel C ADOC Control Nominal

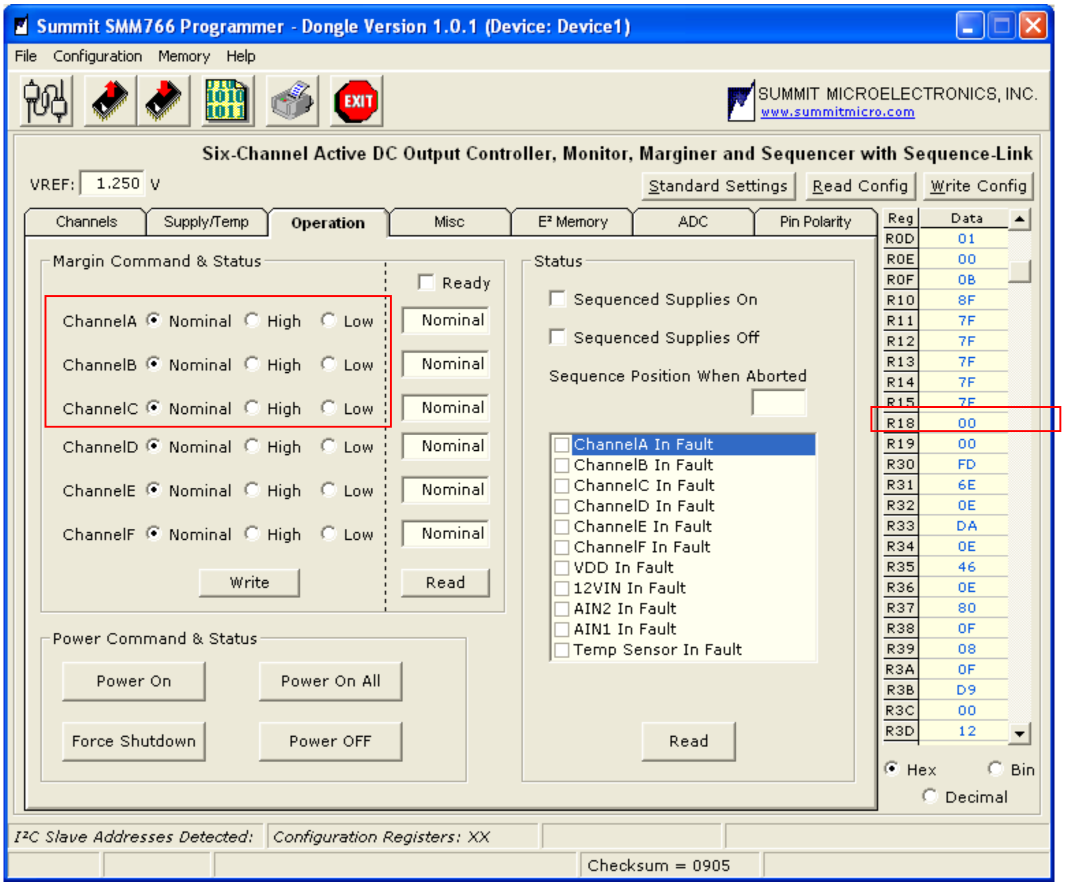

Figure 16 - Register R18 Operation Windows GUI Tab

Register R19, R1B, R1D, R1F – ADOC Control Commands for Channels D, E and F

Writing to any of these registers constitutes an ADOC Control Command. This command initiates control of Channels D, E and F to the desired ADOC Control Mode voltage.

Register R19, R1B, R1D, R1F								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
X	X	1	1	X	X	X	X	Channel D ADOC Control Margin High
X	X	1	0	X	X	X	X	Channel D ADOC Control Margin Low
X	X	0	X	X	X	X	X	Channel D ADOC Control Nominal
X	X	X	X	1	1	X	X	Channel E ADOC Control Margin High
X	X	X	X	1	0	X	X	Channel E ADOC Control Margin Low
X	X	X	X	0	X	X	X	Channel E ADOC Control Nominal
X	X	X	X	X	X	1	1	Channel F ADOC Control Margin High
X	X	X	X	X	X	1	0	Channel F ADOC Control Margin Low
X	X	X	X	X	X	0	X	Channel F ADOC Control Nominal

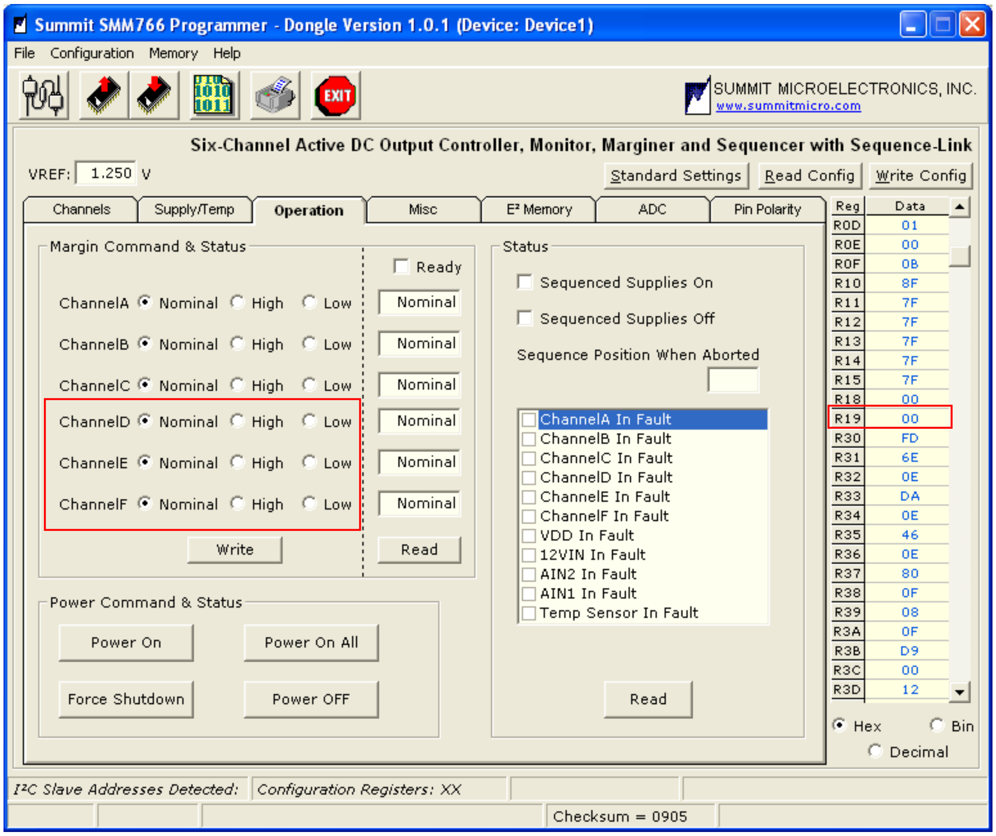

Figure 17 - Register R19 Operation Windows GUI Tab

Register R2A, R2C, R2E – Reserved (READ ONLY)

These registers are Reserved for future use with the ADC readout.

Register R2A, R2C, R2E								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	TBD
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	TBD
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	TBD
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	TBD
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	TBD
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	TBD

Register R2B, R2D, R2F – Reserved (READ ONLY)
These registers are Reserved for future use with the ADC readout.

Register R2B, R2D, R2F								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	TBD
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	TBD
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	TBD
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	TBD

Register R80, R82, R84, R86, R88, R8A, R8C, R8E, R90, R92, R94, R96, R98, R9A, R9C, R9E, RA0, RA2, RA4, RA6, RA8, RAA, RAC, RAE, RB0, RB2, RB4, RB6, RB8, RBA, RBC, RBE – Triggers, Filter, and Voltage Limits for Channels A, B, C, D, E and F, VDD and 12VIN
These registers are combined with the following set of registers to set the over-voltage (OV1 and OV2) and under-voltage (UV1 and UV2) limits. Each limit also has associated triggers and filters.

Register R80, R82, R84, R86, R88, R8A, R8C, R8E, R90, R92, R94, R96, R98, R9A, R9C, R9E, RA0, RA2, RA4, RA6, RA8, RAA, RAC, RAE, RB0, RB2, RB4, RB6, RB8, RBA, RBC, RBE								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	**X**	**X**	**X**	**X**	**X**	**X**	**X**	Triggers RST
0	**X**	**X**	**X**	**X**	**X**	**X**	**X**	Does not trigger RST
X	**1**	**X**	**X**	**X**	**X**	**X**	**X**	Triggers HEALTHY
X	**0**	**X**	**X**	**X**	**X**	**X**	**X**	Does not trigger HEALTHY
X	**X**	**1**	**X**	**X**	**X**	**X**	**X**	Triggers Power-Off
X	**X**	**0**	**X**	**X**	**X**	**X**	**X**	Does not trigger Power-Off
X	**X**	**X**	**1**	**X**	**X**	**X**	**X**	Triggers Force Shutdown
X	**X**	**X**	**0**	**X**	**X**	**X**	**X**	Does not trigger Force Shutdown
X	**X**	**X**	**X**	**1**	**1**	**X**	**X**	Fault on 6 Consecutive Conversions
X	**X**	**X**	**X**	**1**	**0**	**X**	**X**	Fault on 4 Consecutive Conversions
X	**X**	**X**	**X**	**0**	**1**	**X**	**X**	Fault on 2 Consecutive Conversions
X	**X**	**X**	**X**	**0**	**0**	**X**	**X**	Fault on 1 Conversion
X	**X**	**X**	**X**	**X**	**X**	**C9**	**C8**	Bits [9:8] of 10-bit Limit Setting

Register R81, R83, R85, R87, R89, R8B, R8D, R8F, R91, R93, R95, R97, R99, R9B, R9D, R9F, RA1, RA3, RA5, RA7, RA9, RAB, RAD, RAF, RB1, RB3, RB5, RB7, RB9, RBB, RBD, RBF - Voltage Limits for Channels A, B, C, D, E and F, VDD and 12VIN

These registers are combined with the previous set of registers to set the over-voltage (OV1 and OV2) and under-voltage (UV1 and UV2) limits.

Register R81, R83, R85, R87, R89, R8B, R8D, R8F, R91, R93, R95, R97, R99, R9B, R9D, R9F, RA1, RA3, RA5, RA7, RA9, RAB, RAD, RAF, RB1, RB3, RB5, RB7, RB9, RBB, RBD, RBF								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Bits [7:0] of 10-bit Limit Setting

The Limit Setting bits for *Standard Accuracy* (C[9:0]) are set using the following table:

If Channel =:	**Then = C[9:0]:**
A, B, C, D, E, F or VDD	1024 * Limit(V)/(4 * VREF_ADC)
12VIN	1024 * Limit(V)/(12 * VREF_ADC)

The Limit Setting bits for *Improved Accuracy* (C[9:0]) are set using the following table:

If Channel =:	**Then = C[9:0]:**
A, B, C, D, E, F or VDD	1024 * Limit(V)_NEW/(4 * VREF_ADC)
12VIN	1024 * Limit(V)_NEW 12 * VREF_ADC)

Where Limit(V)_NEW = LIMIT(V)*(1.00035 +0.00035*LIMIT(V)) - 0.002 for Channels A-F and VDD.

Where Limit(V)_NEW = LIMIT(V)*(0.99965 +0.00035*LIMIT(V)) - 0.011 for 12V.

The following table lists the registers with their corresponding Channel and Limit:

Registers	Ch. - Limit	Registers	Ch. – Limit	Registers	Ch. – Limit	Registers	Ch. - Limit
R80:R81	Ch A – UV1	R90:R91	Ch C – UV1	RA0:RA1	Ch E – UV1	RB0:RB1	VDD – UV1
R82:R83	Ch A – UV2	R92:R93	Ch C – UV2	RA2:RA3	Ch E – UV2	RB2:RB3	VDD – UV2
R84:R85	Ch A – OV1	R94:R95	Ch C – OV1	RA4:RA5	Ch E – OV1	RB4:RB5	VDD – OV1
R86:R87	Ch A – OV2	R96:R97	Ch C – OV2	RA6:RA7	Ch E – OV2	RB6:RB7	12VIN – OV2
R88:R89	Ch B – UV1	R98:R99	Ch D – UV1	RA8:RA9	Ch F – UV1	RB8:RB9	12VIN – UV1
R8A:R8B	Ch B – UV2	R9A:R9B	Ch D – UV2	RAA:RAB	Ch F – UV2	RBA:RBB	12VIN – UV2
R8C:R8D	Ch B – OV1	R9C:R9D	Ch D – OV1	RAC:RAD	Ch F – OV1	RBC:RBD	12VIN – OV1
R8E:R8F	Ch B – OV2	R9E:R9F	Ch D – OV2	RAE:RAF	Ch F – OV2	RBE:RBF	12VIN– OV2

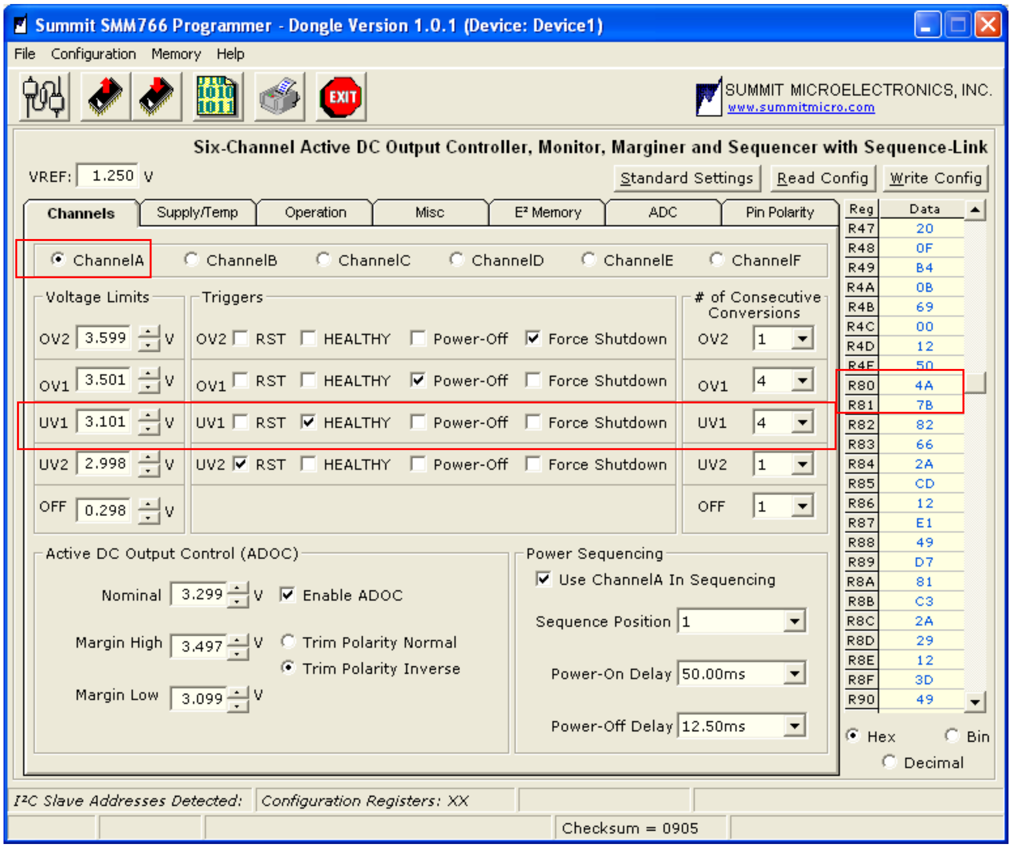

Figure 18 - Register R80, R81 Windows GUI Tab

Register RC0, RC2, RC4, RC6, RC8, RCA, RCC, RCE, RD0, RD2, RD4, RD6 – Triggers, Filter, and Limits for AIN1, AIN2 and the Internal Temperature Sensor

These registers are combined with the following set of registers to set the over-voltage (OV1 and OV2) and under-voltage (UV1 and UV2) limits and the over-temperature (OT1 and OT2) and under-temperature (UT1 and UT2) limits. Each limit also has associated triggers and filters.

Register RC0, RC2, RC4, RC6, RC8, RCA, RCC, RCE, RD0, RD2, RD4, RD6								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	X	X	X	X	X	X	X	Triggers RST
0	X	X	X	X	X	X	X	Does not trigger RST
X	1	X	X	X	X	X	X	Triggers HEALTHY
X	0	X	X	X	X	X	X	Does not trigger HEALTHY
X	X	1	X	X	X	X	X	Triggers Power-Off
X	X	0	X	X	X	X	X	Does not trigger Power-Off
X	X	X	1	X	X	X	X	Triggers FAULT
X	X	X	0	X	X	X	X	Does not trigger FAULT
X	X	X	X	1	1	X	X	Fault on 6 Consecutive Conversions
X	X	X	X	1	0	X	X	Fault on 4 Consecutive Conversions
X	X	X	X	0	1	X	X	Fault on 2 Consecutive Conversions
X	X	X	X	0	0	X	X	Fault on 1 Conversion
X	X	X	X	X	X	C9	C8	Bits [9:8] of 10-bit Limit Setting

Register RC1, RC3, RC5, RC7, RC9, RCB, RCD, RCF, RD1, RD3, RD5, RD7 - Limits for AIN1, AIN2 and the Internal Temperature Sensor

These registers are combined with the previous set of registers to set the over-voltage (OV1 and OV2) and under-voltage (UV1 and UV2) limits and the over-temperature (OT1 and OT2) and under-temperature (UT1 and UT2) limits.

Register RC1, RC3, RC5, RC7, RC9, RCB, RCD, RCF, RD1, RD3, RD5, RD7								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	C6	C5	C4	C3	C2	C1	C0	Bits [7:0] of 10-bit Limit Setting

The Limit Setting bits (C[9:0]) are set using the following table:

If Channel =:	Then = C[9:0]:
AIN1 or AIN2	1024 * Limit(V)/(2 * VREF_ADC)
Internal Temperature Sensor	R/4 (if R<= 511), (R-1024)/4 (if R > 511), Where R = 10-bit value

The following table lists the registers with their corresponding Channel and Limit:

Registers	Ch. - Limit	Registers	Ch. – Limit
RC0:RC1	Int. Temp. Sense – UT1	RD0:R91	AIN2 – UV1
RC2:RC3	Int. Temp. Sense – UT2	RD2:R93	AIN2 – UV2
RC4:RC5	Int. Temp. Sense – OT1	RD4:R95	AIN2 – OV1
RC6:RC7	Int. Temp. Sense – OT2	RD6:R97	AIN2 – OV2
RC8:RC9	AIN1 – UV1		
RCA:R8B	AIN1 – UV2		
RCC:R8D	AIN1 – OV1		
RCE:RCF	AIN1 – OV2		

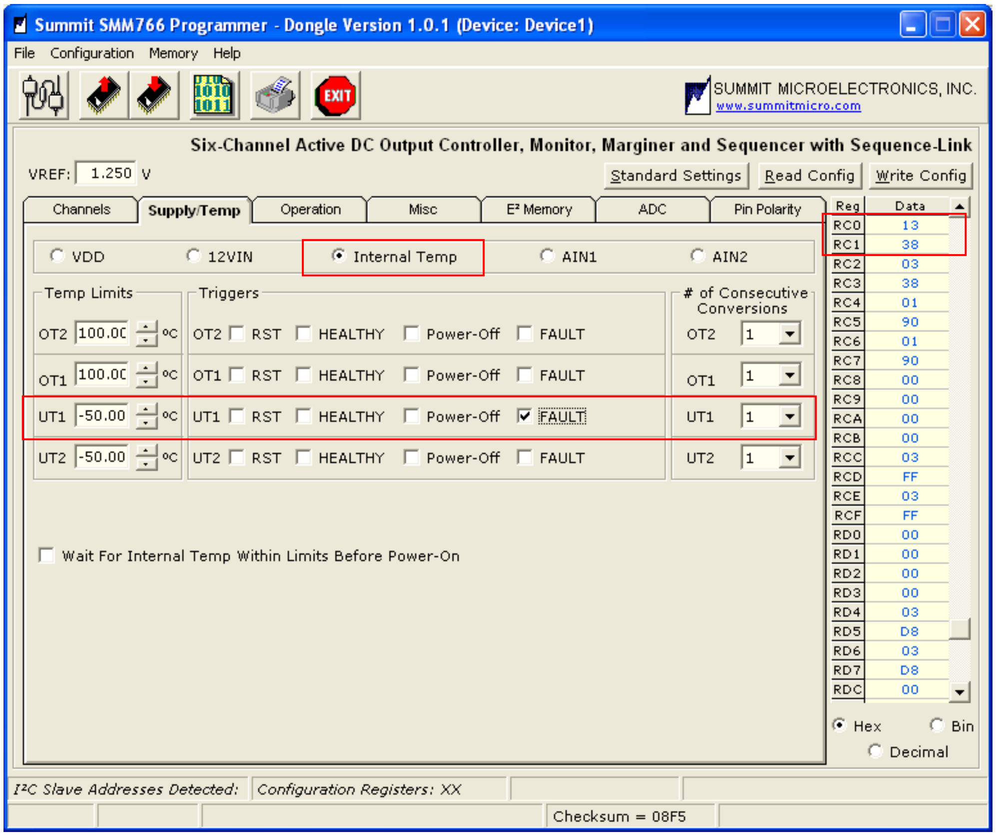

Figure 19 - Register RC0, RC1 Windows GUI Tab

Register RE0, RE2, RE4, RE6, RE8, REA - Filter and Off Limit for Channels A, B, C, D, E and F

These registers are combined with the following set of registers to set the OFF limit used for Power-Off sequencing and Force Shutdown operations.

Register RE0, RE2, RE4, RE6, RE8, REA								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**0**	**0**	**X**	**X**	**X**	**X**	These bits have no control function but must be set to 0.
X	**X**	**X**	**X**	**1**	**1**	**X**	**X**	OFF on 6 Consecutive Conversions
X	**X**	**X**	**X**	**1**	**0**	**X**	**X**	OFF on 4 Consecutive Conversions
X	**X**	**X**	**X**	**0**	**1**	**X**	**X**	OFF on 2 Consecutive Conversions
X	**X**	**X**	**X**	**0**	**0**	**X**	**X**	OFF on 1 Conversion
X	**X**	**X**	**X**	**X**	**X**	**C9**	**C8**	Bits [9:8] of 10-bit Limit Setting

Register RE1, RE3, RE5, RE7, RE9, REB - Off Limit for Channels A, B, C, D, E and F

These registers are combined with the previous set of registers to set the OFF limit used for Power-Off sequencing and Force Shutdown operations.

Register RE1, RE3, RE5, RE7, RE9, REB								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Bits [7:0] of 10-bit Limit Setting

The Limit Setting bits (C[9:0]) are set using the following table:

If Channel =:	**Then = C[9:0]:**
A, B, C, D, E or F	1024 * Limit(V)/(4 * VREF_ADC)

The following table lists the registers with their corresponding Channel and Limit:

Registers	**Ch. – Limit**
RE0:RE1	Ch A – OFF
RE2:RE3	Ch B – OFF
RE4:RE5	Ch C – OFF
RE6:RE7	Ch D – OFF
RE8:RE9	Ch E – OFF
REA:REB	Ch F – OFF

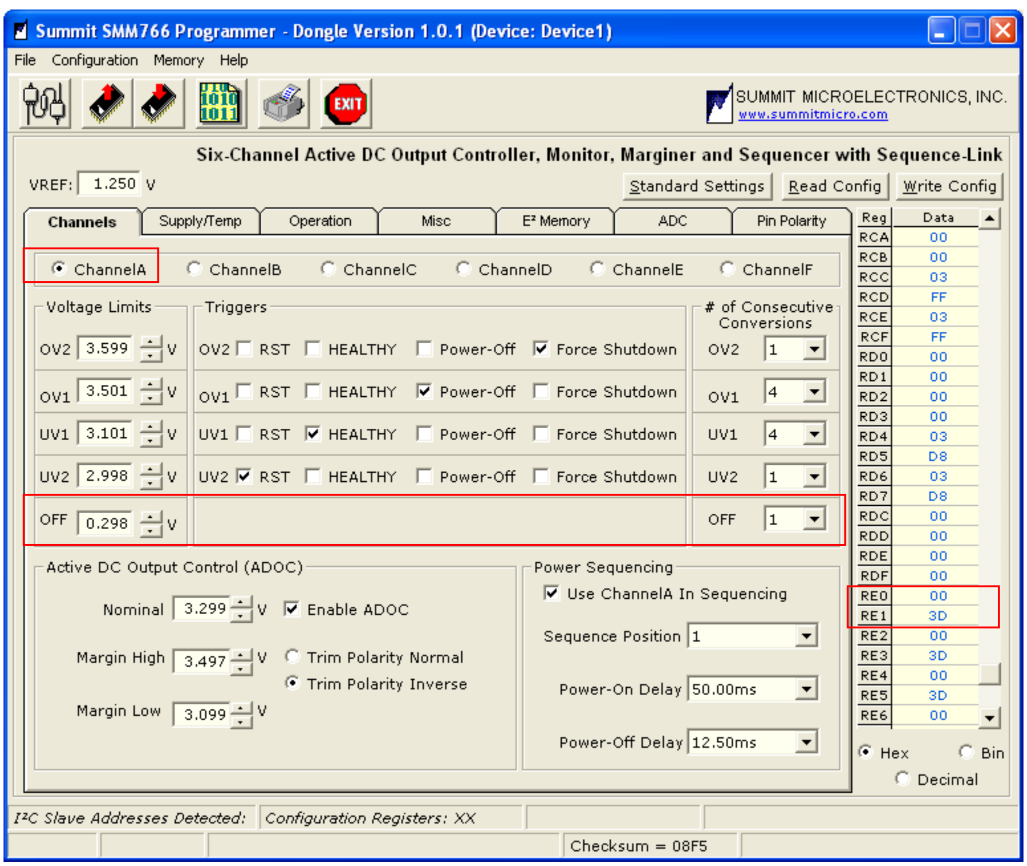

Figure 20 - Register RE0, RE1 Windows GUI Tab

The following registers are located at slave address 1001$_{BIN}$, bus address A2 A1 A0 where A2 is either the A2 pin bias or 0 depending on the programmed selection and A1 A0 are depend on the programmed combination. See register R0E in the above section.

Register R80 – Command and Status Register (Volatile)

This volatile register allows I2C control of the Power-On, Power-Off and Force Shutdown commands. It also contains to status bits which are set when all the sequenced channels are on and when all the sequenced channels are off.

Register R80								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	0	0	X	X	X	X	X	Power-On Command
0	1	0	X	X	X	X	X	Power-Off Command
0	0	1	X	X	X	X	X	Force Shutdown Command
X	X	X	0	X	X	X	X	Not used
X	X	X	X	0	X	X	X	All Sequenced Channels not ON (Read-Only)
X	X	X	X	X	1	X	X	All Sequenced Channels OFF (Read-Only)
X	X	X	X	X	0	X	X	All Sequenced Channels not OFF (Read-Only)

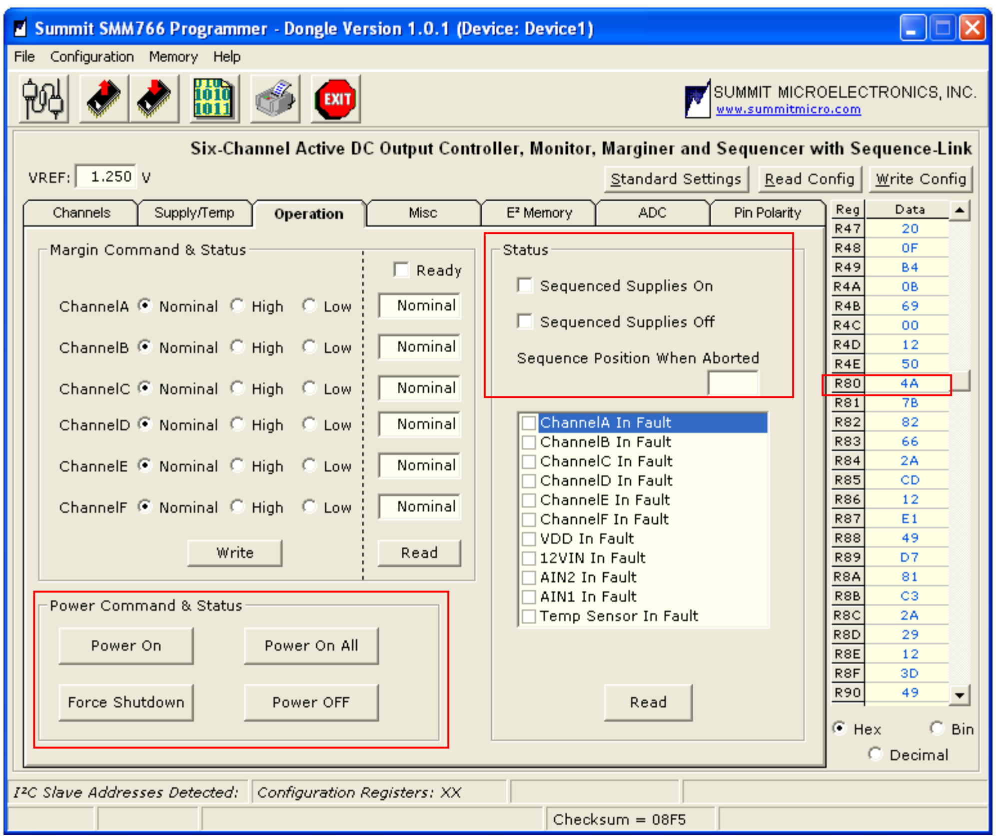

Figure 21 - Register R80 Windows GUI Tab

Register R81 – Status Register (Volatile, Read-Only)

This volatile, read-only register shows the status of AIN1, AIN2 and the Internal Temperature. Bits D[7:4] of the register store information regarding a Sequence Termination.

Register R81								
D7	D6	D5	D4	D3	D2	D1	D0	Action
0	0	1	0	0	X	X	X	Last Sequence Terminated in Position 4
0	0	0	0	0	X	X	X	Last Sequence Terminated in Position 0
X	X	X	X	X	1	X	X	Fault on AIN2
X	X	X	X	X	0	X	X	No Fault on AIN2
X	X	X	X	X	X	1	X	Fault on AIN1
X	X	X	X	X	X	0	X	No Fault on AIN1
X	X	X	X	X	X	X	1	Fault on Internal Temperature Sensor
X	X	X	X	X	X	X	0	No Fault on Internal Temperature Sensor

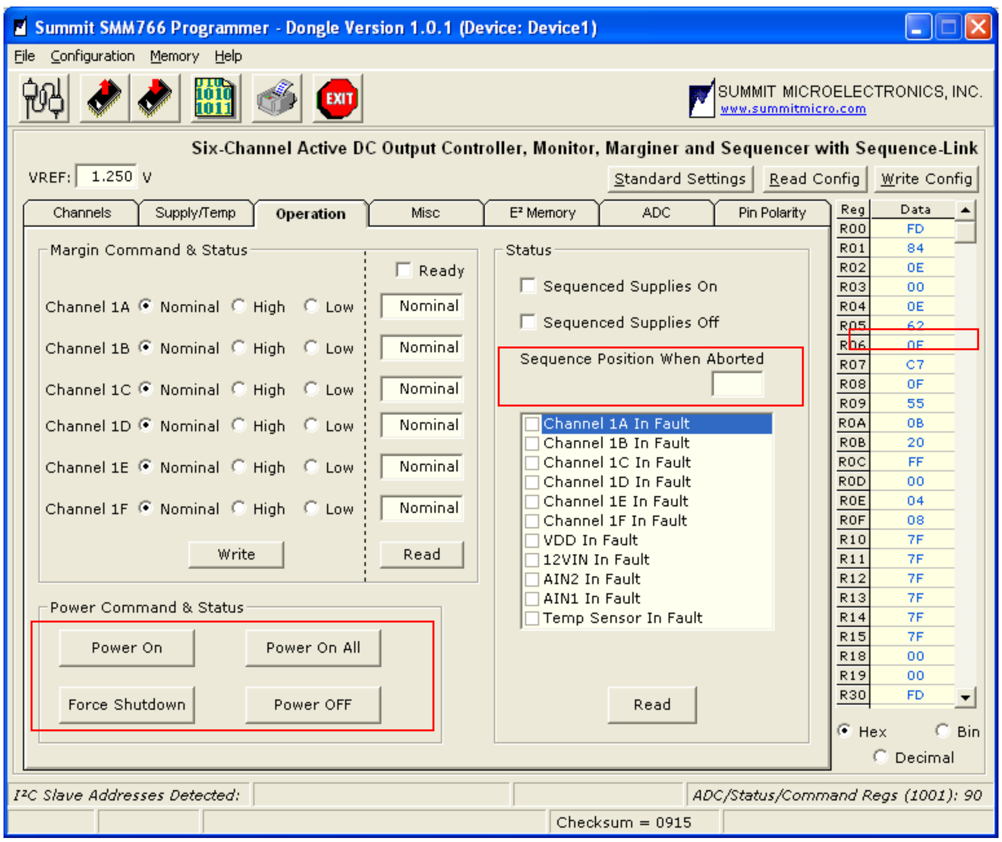

Figure 22 - Register R81 Windows GUI Tab

Register R82 – Status Register (Volatile, Read-Only)

This volatile, read-only register shows the status of Channels A, B, C, D, E and F and the VDD and 12VIN inputs.

Register R82								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	X	X	X	X	X	X	X	Fault on Channel 12VIN
0	X	X	X	X	X	X	X	No Fault on Channel 12VIN
X	1	X	X	X	X	X	X	Fault on Channel VDD
X	0	X	X	X	X	X	X	No Fault on VDD
X	X	1	X	X	X	X	X	Fault on Channel F
X	X	0	X	X	X	X	X	No Fault on Channel F
X	X	X	1	X	X	X	X	Fault on Channel E
X	X	X	0	X	X	X	X	No Fault on Channel E
X	X	X	X	1	X	X	X	Fault on Channel D
X	X	X	X	0	X	X	X	No Fault on Channel D
X	X	X	X	X	1	X	X	Fault on Channel C
X	X	X	X	X	0	X	X	No Fault on Channel C
X	X	X	X	X	X	1	X	Fault on Channel B
X	X	X	X	X	X	0	X	No Fault on Channel B
X	X	X	X	X	X	X	1	Fault on Channel A
X	X	X	X	X	X	X	0	No Fault on Channel A

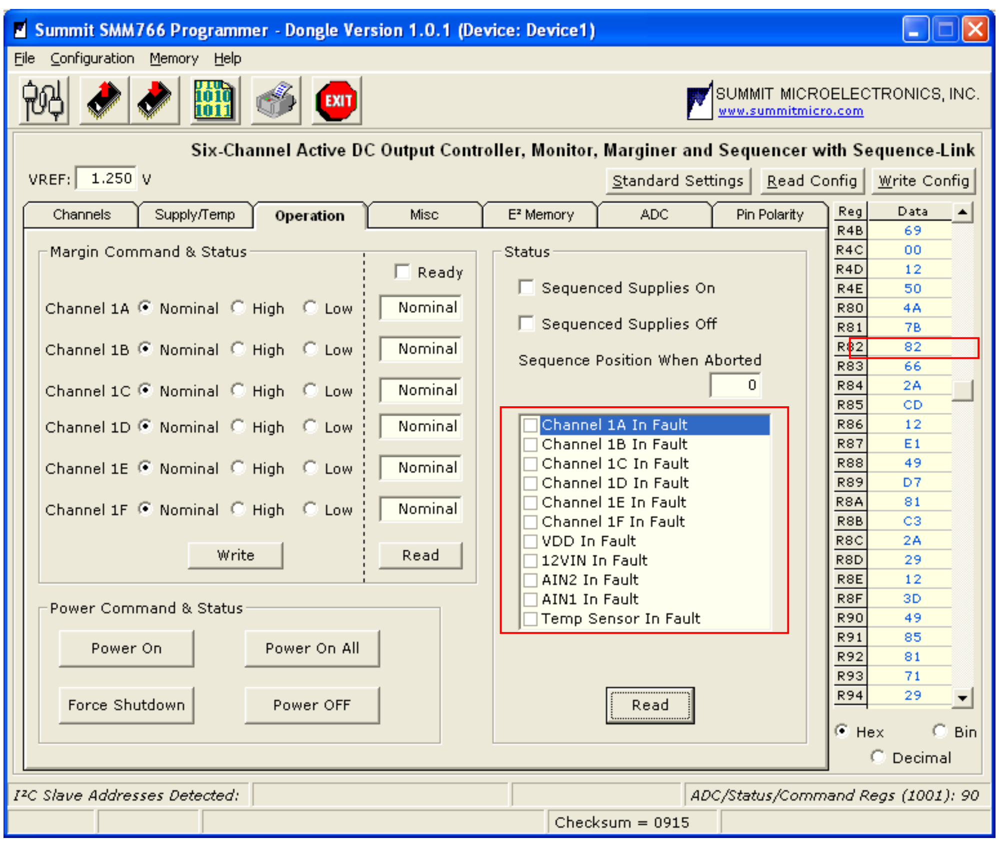

Figure 23 - Register R82 Windows GUI Tab

Register R84 - PUPX Pin Polarities

This register sets the polarity of the PUP outputs.

Register R84								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**X**	**X**	**X**	**X**	**X**	**X**	Set these bits to 0's
X	**X**	**1**	**X**	**X**	**X**	**X**	**X**	PUPF Active High
X	**X**	**0**	**X**	**X**	**X**	**X**	**X**	PUPF Active Low
X	**X**	**X**	**1**	**X**	**X**	**X**	**X**	PUPE Active High
X	**X**	**X**	**0**	**X**	**0**	**X**	**X**	PUPE Active Low
X	**X**	**X**	**X**	**1**	**X**	**X**	**X**	PUPD Active High
X	**X**	**X**	**X**	**0**	**X**	**X**	**X**	PUPD Active Low
X	**X**	**X**	**X**	**X**	**1**	**X**	**X**	PUPC Active High
X	**X**	**X**	**X**	**X**	**0**	**X**	**X**	PUPC Active Low
X	**X**	**X**	**X**	**X**	**X**	**1**	**X**	PUPB Active High
X	**X**	**X**	**X**	**X**	**X**	**0**	**X**	PUPB Active Low
X	**X**	**X**	**X**	**X**	**X**	**X**	**1**	PUPA Active High
X	**X**	**X**	**X**	**X**	**X**	**X**	**0**	PUPA Active Low

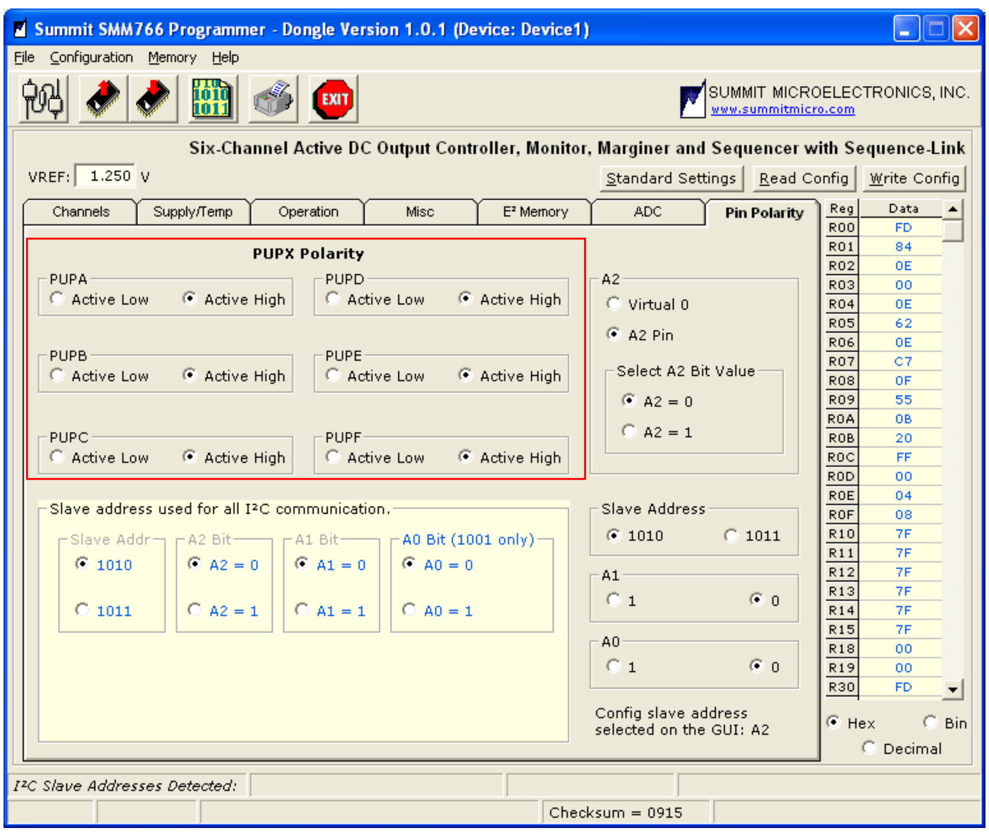

Figure 24 - Register R84 Windows GUI Tab

Register R85 - ADOC Control Mode Status Register (Volatile, Read-Only)

This volatile, read-only register shows the mode of ADOC Control for Channels A, B and C. Bit D[7] of this register is set when all channels are at the desired ADOC Control voltage.

Register R85								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	X	X	X	X	X	X	X	ADOC Control is Ready (Channels at set point)
0	X	X	X	X	X	X	X	ADOC Control is not Ready
X	X	1	1	X	X	X	X	Channel A ADOC Control Mode is Margin High
X	X	1	0	X	X	X	X	Channel A ADOC Control Mode is Margin Low
X	X	0	X	X	X	X	X	Channel A ADOC Control Mode is Nominal
X	X	X	X	1	1	X	X	Channel B ADOC Control Mode is Margin High
X	X	X	X	1	0	X	X	Channel B ADOC Control Mode is Margin Low
X	X	X	X	0	X	X	X	Channel B ADOC Control Mode is Nominal
X	X	X	X	X	X	1	1	Channel C ADOC Control Mode is Margin High
X	X	X	X	X	X	1	0	Channel C ADOC Control Mode is Margin Low
X	X	X	X	X	X	0	X	Channel C ADOC Control Mode is Nominal

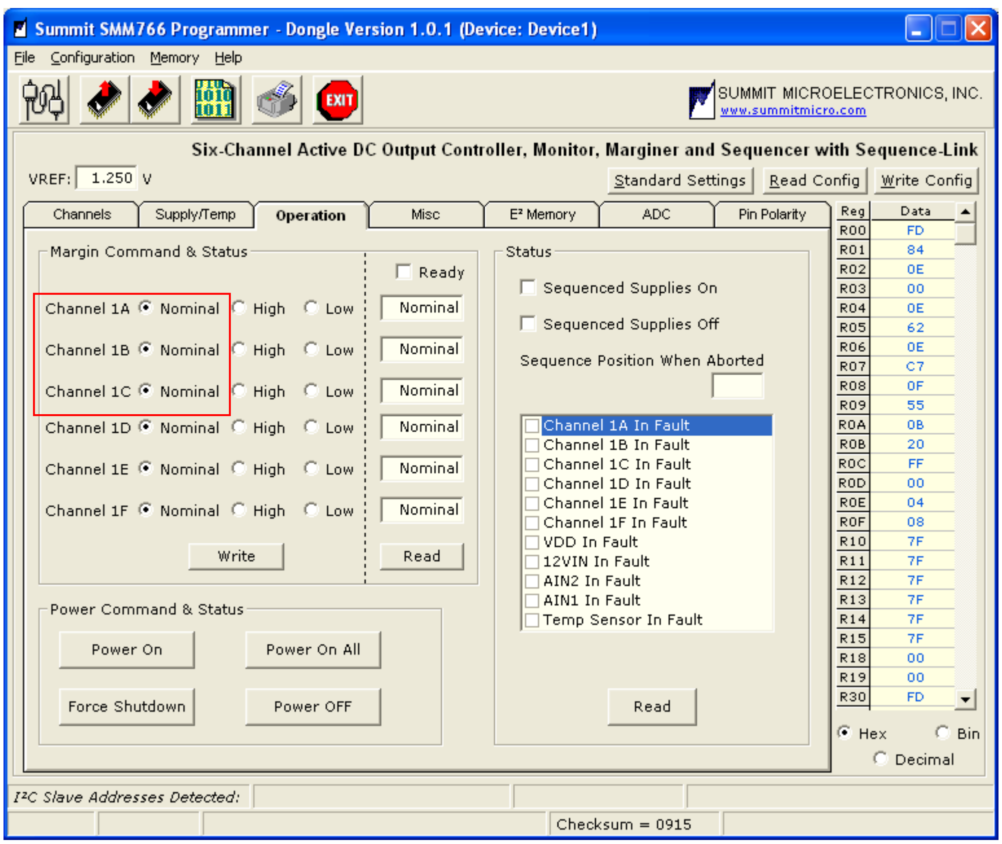

Figure 26 - Register R85 Windows GUI Tab

Register R86 - ADOC Control Mode Status Register (Volatile, Read-Only)

This volatile, read-only register shows the mode of ADOC Control for Channels D, E and F. Bit D[7] of this register is set when all channels are at the desired ADOC Control voltage.

Register R86								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	X	X	X	X	X	X	X	ADOC Control is Ready (Channels at set point)
0	X	X	X	X	X	X	X	ADOC Control is not Ready
X	X	1	1	X	X	X	X	Channel D ADOC Control Mode is Margin High
X	X	1	0	X	X	X	X	Channel D ADOC Control Mode is Margin Low
X	X	0	X	X	X	X	X	Channel D ADOC Control Mode is Nominal
X	X	X	X	1	1	X	X	Channel E ADOC Control Mode is Margin High
X	X	X	X	1	0	X	X	Channel E ADOC Control Mode is Margin Low
X	X	X	X	0	X	X	X	Channel E ADOC Control Mode is Nominal
X	X	X	X	X	X	1	1	Channel F ADOC Control Mode is Margin High
X	X	X	X	X	X	1	0	Channel F ADOC Control Mode is Margin Low
X	X	X	X	X	X	0	X	Channel F ADOC Control Mode is Nominal

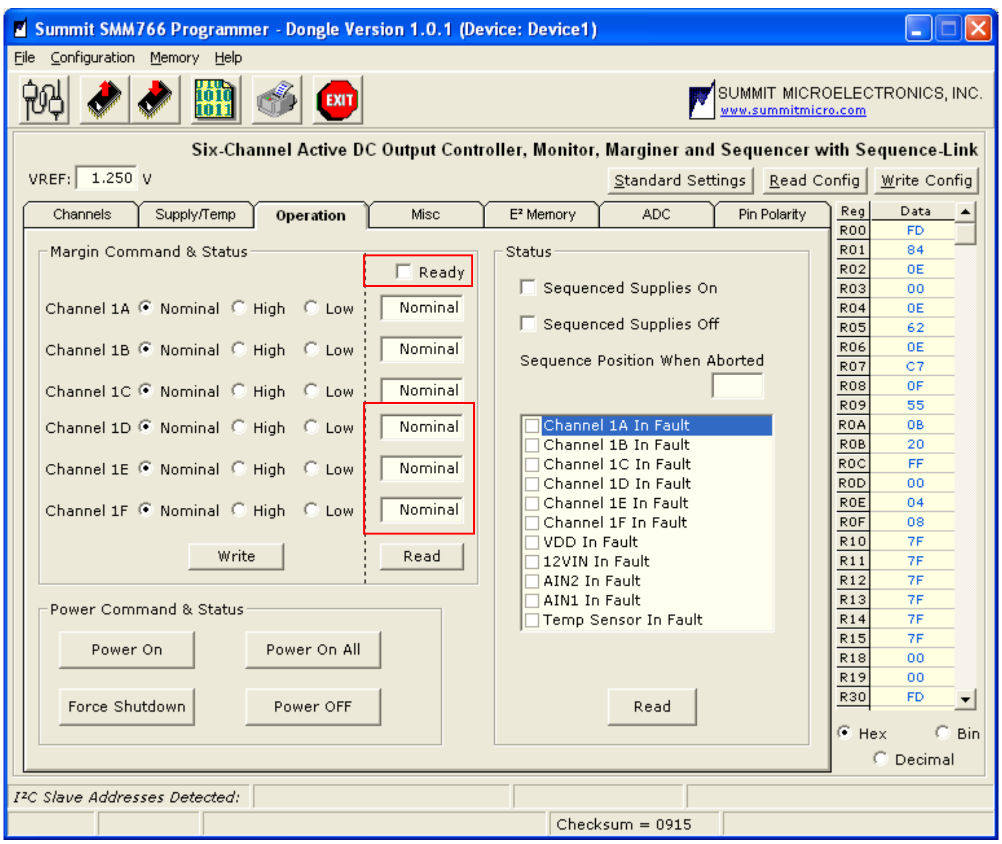

Figure 27 - Register R86 Windows GUI Tab

Register R00, R08, R10, R18, R20, R28, R30, R38, R40, R48, R50 – Channel echo and ADC Data for Channels A, B, C, D, E, F, VDD, 12V, INT_TEMP, AIN1, AIN2 – See Figure 28 and 29.

Register R00, R08, R10, R18, R20, R28, R30, R38, R40, R48, R50								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**X**	**X**	**X**	**X**	**0**	**C9**	**C8**	Bits [9:8] of 10-bit ADC Data
0	**CH3**	**CH2**	**CH1**	**CH0**	**0**	**X**	**X**	Bits [6:3] Channel Address Echo

Register R01, R09, R11, R19, R21, R29, R31, R39, R41, R49, R51 – ADC Data for Channels A, B, C, D, E, F, VDD, 12V, INT_TEMP, AIN1, AIN2 – See Figure 28 and 29.

Register R01, R09, R11, R19, R21, R29, R31, R39, R41, R49, R51								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Bits [7:0] of 10-bit ADC Data

Formulas to calculate ADC Voltages (Standard Accuracy):

V= VREF_ADC, ADCout = 10-bit ADC Value read from device.

1. Voltage A, B, C, D, E, F, VDD = (ADCout * V)/256

2. Voltage 12VIN = (ADCout * V * 3)/256

3. Voltage AIN1, AIN2 = (ADCout * V)/512

4. Temp Sensor = ADCread/4 (if ADCout <= 511)
   = (ADCout - 400hex)/4 (if ADCout > 511)

Formulas to calculate ADC Voltages (Improved Accuracy) VMx, VDD and 12V:

V= VREF_ADC, ADCout = 10-bit ADC Value read from device, ADCread = ADCout converted to units of volts.

For VM_A-VM_F, VDD:

1. V = ADCread*(1.00035+0.00035*ADCread)-0.002
Where: ADCread = (ADCout* VREF_ADC)/256

For 12V:
2. V = ADCread*(0.99965 +0.00045*ADCread)-0.011
Where: ADCread = (3*ADCout* VREF_ADC)/256

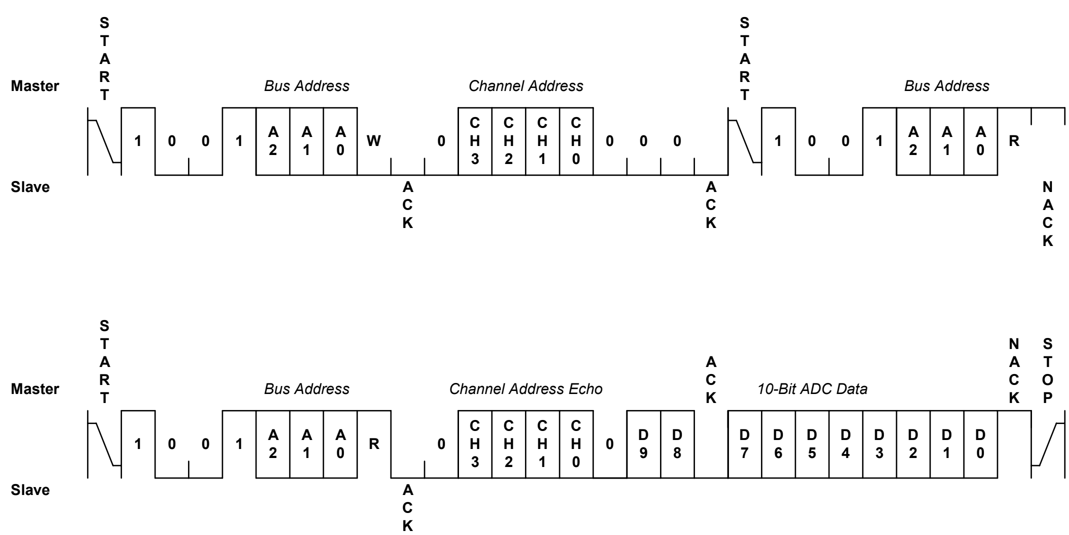

Figure 28 – ADC Conversion Read

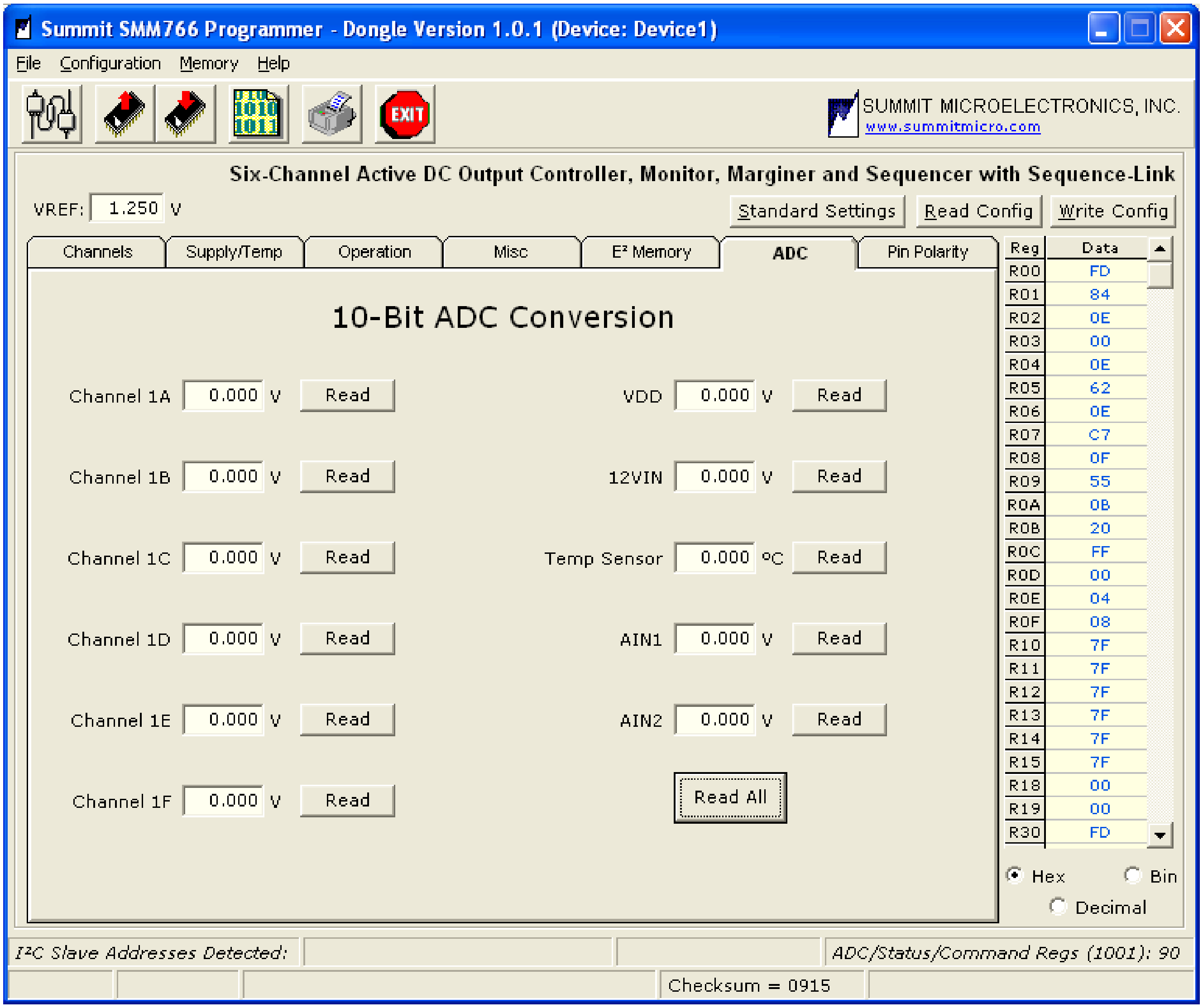

Figure 29 - ADC Windows GUI Tab

Register R87 - Write Protection Register (Write-Only)

This volatile, write-only register disables write protection to the memory and configuration registers. This register powers up into a write protected state. Before a write operation is allowed, the code 0101_{BIN} must be written to this registers memory or configuration bits. The register must then be written with other data (----BIN) to write protect the memory or configuration.

Register R86								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	1	0	1	X	X	X	X	Memory Write Protection Disabled
-	-	-	-	X	X	X	X	Memory Write Protection Enabled
X	X	X	X	0	1	0	1	Configuration Write Protection Disabled
X	X	X	X	-	-	-	-	Configuration Write Protection Enabled

Register R88 - STATUS TRACKING CODE Identification

Register data bits D[7:0] are read-only bits that identify the "STATUS TRACKING CODE" of the SMM766. The command to do this is available in the Configuration pull down menu. The Status Tracking Code will appear in the bottom right side corner of the GUI window. The Status Code will also appear whenever a "Read Config" command is performed with an SMM766 device connected to the target PC.

Register R88								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	0	0	0	0	0	0	1	Status Tracking Code 01
0	0	0	0	0	0	1	0	Status Tracking Code 02
0	0	0	0	0	0	1	1	Status Tracking Code 03
0	0	1	0	0	1	0	1	Status Tracking Code 08

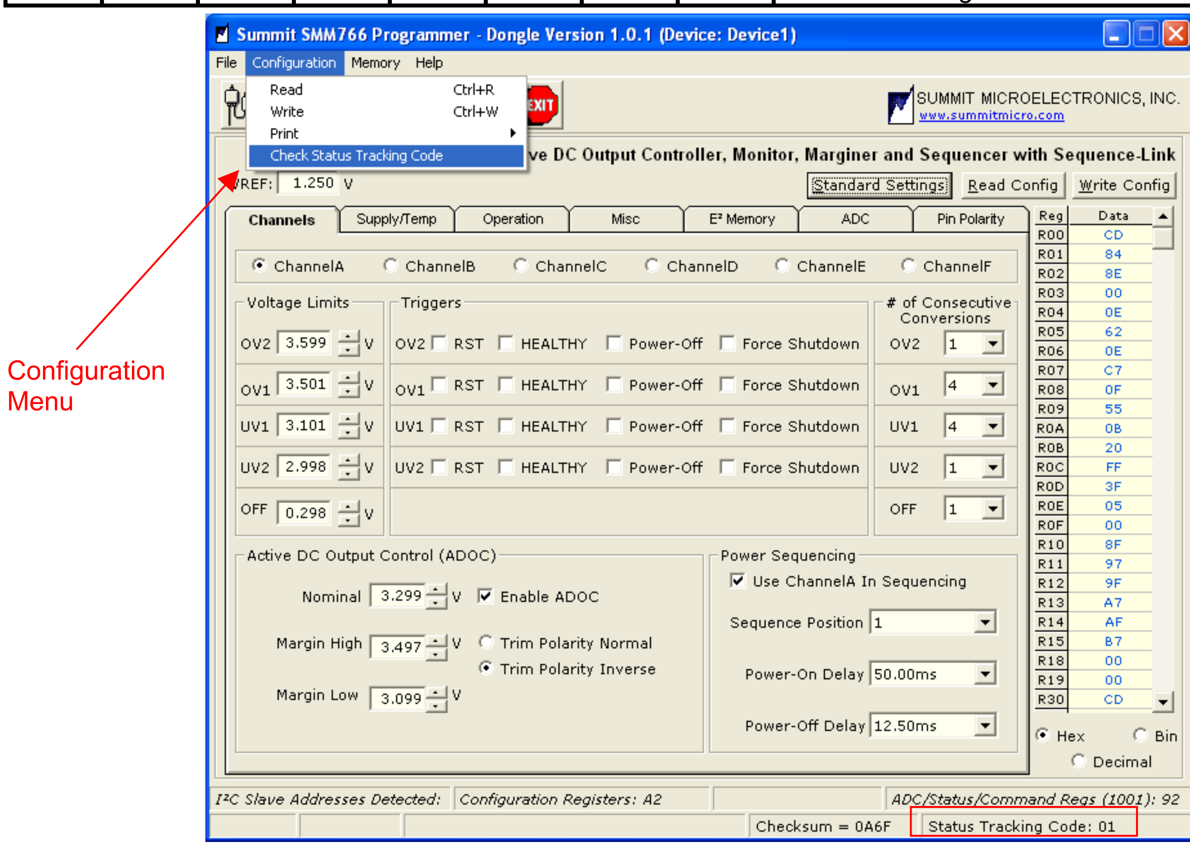

Figure 30 - Register R88 Windows GUI Tab

2k Nonvolatile General Purpose Memory Array

The memory array can be updated by writing data directly into the memory location. To write into a specific location, go to the Hex column location in the Tabular view and press the 'Backspace' key. Type in the new data and then press the 'Enter' key.

A graphic view of the memory can also be displayed for test purposes to check that the entire memory contents has changed or by writing pages or bytes, etc. using the buttons in the Graphic View Memory window.

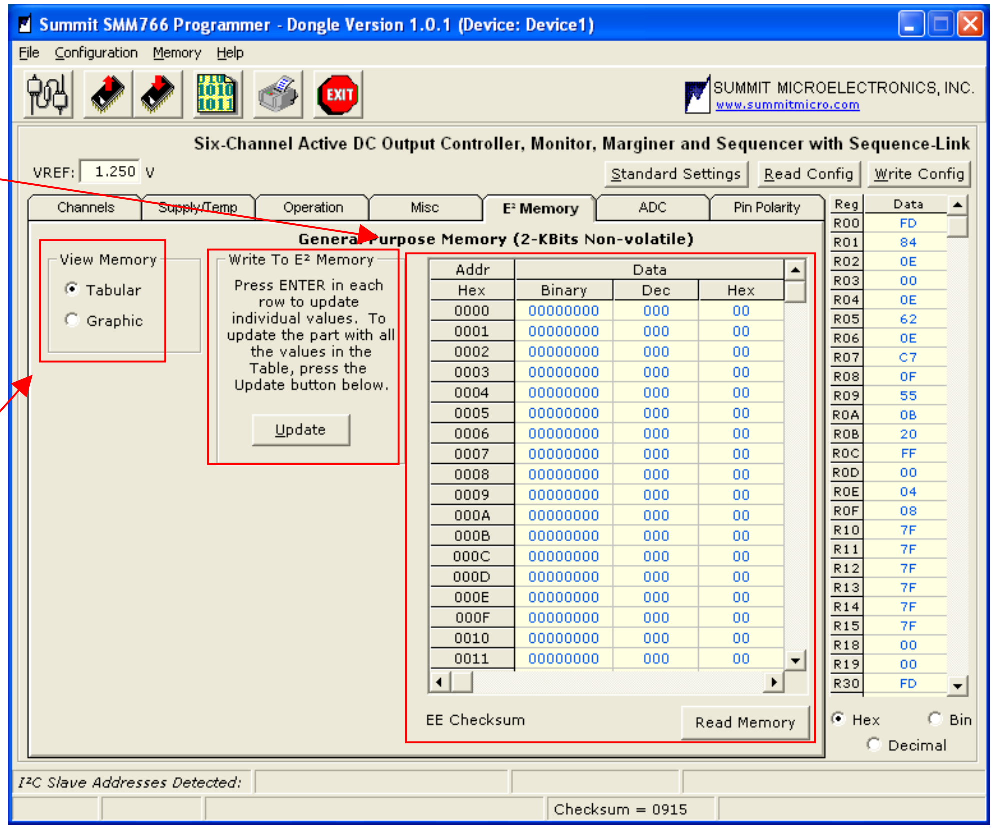

Figure 31 – E^2 Memory Array Windows GUI

Saving the hex file

When clicking on the File Save icon for the SMM766B the following message will appear in Figure 31A below:

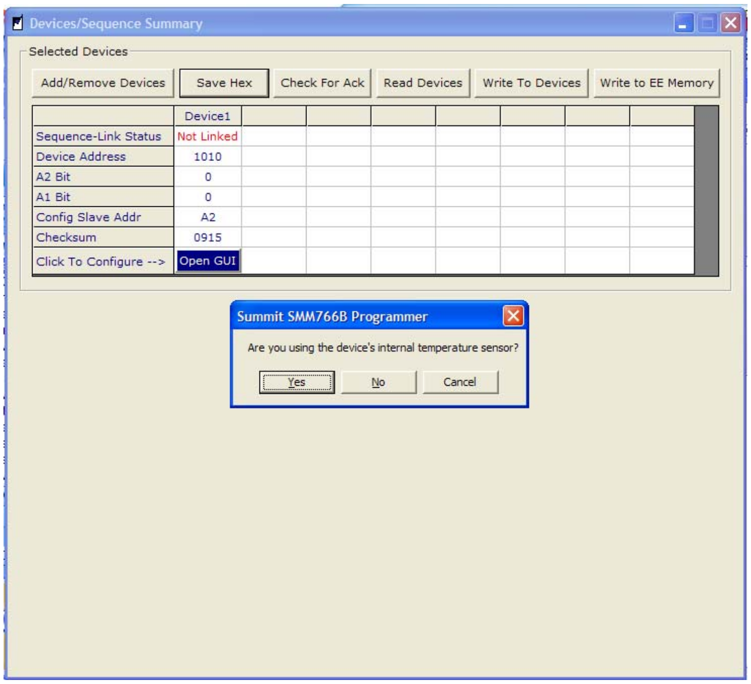

Figure 31A – SMM766B Temperature Sensor selection Window

Choose "Yes" if you are using the SMM766B's internal temperature sensor, "No" if you are not. Once this selection is made the message in Figure 31B appears.

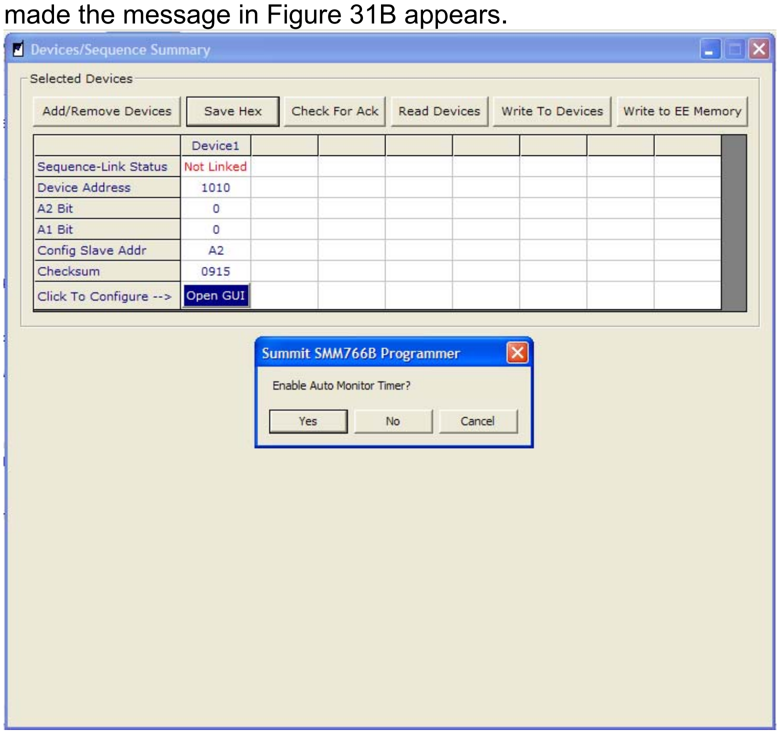

Figure 31B – SMM766B Auto Monitor selection Window

Choose "Yes" if you are not using I^2C delays of greater than 200mS, "No" if you wish the SMM766B to resume ADC activity after 200mS following a failed I^2C sequence.

SMM766 Register Map

The following registers are accessed using slave address 101 SA0 A2 1 1 (SA0 = R0E[3])

R00	[7:4] Last seq position used plus one bits [3:4] [3:2] Channel A Margin Nominal Vref Bits [1:0] [0:1] Channel A Nominal Voltage Bits [9:8]
R01	[0:7] Channel A Nominal Voltage Bits [7:0]
R02	[7] Last seq position used plus one bits [4] [6:5] # of retries before power-off latched [3:2] Channel B Margin Nominal Vref Bits [1:0] [0:1] Channel B Nominal Voltage Bits [9:8]
R03	[0:7] Channel B Nominal Voltage [7:0]
R04	[7:4] Unused [3:2] Channel C Margin Nominal Vref Bits [1:0] [0:1]Channel C Nominal Voltage Bits [9:8]
R05	[0:7] Channel C Nominal Voltage [7:0]
R06	[7:4] Unused [3:2] Channel D Margin Nominal Vref Bits [1:0] [0:1] Channel D Nominal Voltage Bits [9:8]
R07	[0:7] Channel D Nominal Voltage [7:0]
R08	[0:1] Channel E Nominal Voltage Bits [9:8] [3:2] Channel E Margin Nominal Vref Bits [1:0] [7:4] Unused
R09	[0:7] Channel E Nominal Voltage [7:0]
R0A	[7:4] Unused [3:2] Channel F Margin Nominal Vref Bits [1:0] [0:1] Channel F Nominal Voltage Bits [9:8]
R0B	[0:7] Channel F Nominal Voltage [7:0]
R0C	[7] Regulator Output Voltage [6] Fast Convergence [5] Channel F Trim Polarity [4] Channel E Trim Polarity [3] Channel D Trim Polarity [2] Channel C Trim Polarity [1] Channel B Trim Polarity [0] Channel A Trim Polarity

R0D	[7] Configuration Lock [6] Unused [5] Channel F Enable Control [4] Channel E Enable Control [3] Channel D Enable Control [2] Channel C Enable Control [1] Channel B Enable Control [0] Channel A Enable Control
R0E	[7:6] Sequence Termination Timeout Period [5:4] Reset Timeout Period [3] Slave Address Select [2] A2 Address Bit [1] A1 Address Bit [0] A0 Address Bit
R0F	[7] VREF_CNTL [6] Write Command For Margin/Active Ctrl Enabling [5] Limit Triggers Enabled After [4] Not used; always set to zero [3] Sequence Link Feature enabled/disabled [2] Seq. Termination Timer During Power-Off [1] Wait For 12VIN Within Limits Before Power On [0] Wait For VDD Within Limits Before Power On
R10	[7:3] Channel A Sequence Position [2:1] Channel A Power-On Delay [0] Channel A Power-Off Delay
R11	[7:3] Channel B Sequence Position [2:1] Channel B Power-On Delay [0] Channel B Power-Off Delay
R12	[7:3] Channel C Sequence Position [2:1] Channel C Power-On Delay [0] Channel C Power-Off Delay

R13	[7:3] Channel D Sequence Position [2:1] Channel D Power-On Delay [0] Channel D Power-Off Delay
R14	[7:3] Channel E Sequence Position [2:1] Channel E Power-On Delay [0] Channel E Power-Off Delay
R15	[7:3] Channel F Sequence Position [2:1] Channel F Power-On Delay [0] Channel F Power-Off Delay
R16	Unused
R17	Unused
R18, R1A, R1C, R1E	[7:6] Unused [5:4] Channel A Margin Command Bits (Write Only) [3:2] Channel B Margin Command Bits (Write Only) [1:0] Channel C Margin Command Bits (Write Only)
R19, R1B, R1D, R1F	[7:6] Unused [5:4] Channel D Margin Command Bits (Write Only) [3:2] Channel E Margin Command Bits (Write Only) [1:0] Channel F Margin Command Bits (Write Only)
R20-R2F	Unused
R30	[7:4] Last seq. position plus 1 bit [3:0] [3:2] Channel A Margin High Vref Bits [1:0] [0:1] Channel A Margin High Voltage Bits [9:8]
R31	[7:0] Channel A Margin High Bits [7:0]
R32	[7] Last seq. position plus 1 bit [4] [6:5] # of retries before power-off latched [3:2] Channel B Margin High Vref Bits [1:0] [0:1] Channel B Margin High Voltage Bits [9:8]
R33	[7:0] Channel B Margin High Bits [7:0]
R34	[7:4] Unused [3:2] Channel C Margin High Vref Bits [1:0] [0:1] Channel C Margin High Voltage Bits [9:8]
R35	[7:0] Channel C Margin High Bits [7:0]

R36	[7:4] Unused [3:2] Channel D Margin High Vref Bits [1:0] [0:1] Channel D Margin High Voltage Bits [9:8]
R37	[7:0] Channel D Margin High Bits [7:0]
R38	[7:4] Unused [3:2] Channel E Margin High Vref Bits [1:0] [0:1] Channel E Margin High Voltage Bits [9:8]
R39	[7:0] Channel E Margin High Bits [7:0]
R3A	[7:4] Unused [3:2] Channel F Margin High Vref Bits [1:0] [0:1] Channel F Margin High Voltage Bits [9:8]
R3B	[7:0] Channel F Margin High Bits [7:0]
R3C to R3F	Unused
R40	[7:4] Last seq. position plus 1 bit [3:0} [3:2] Channel A Margin Low Vref Bits [1:0] [0:1] Channel A Margin Low Voltage Bits [9:8]
R41	[7:0] Channel A Margin Low Bits [7:0]
R42	[7] Last seq. position plus 1 bit [4] [6:5] # of retries before power-off latched [0:1] Channel B Margin Low Voltage Bits [9:8]
R43	[7:0] Channel B Margin Low Bits [7:0]
R44	[7:4] Unused [3:2] Channel C Margin Low Vref Bits [1:0] [0:1] Channel C Margin Low Voltage Bits [9:8]
R45	[7:0] Channel C Margin Low Bits [7:0]
R46	[7:4] Unused [3:2] Channel D Margin Low Vref Bits [1:0] [0:1] Channel D Margin Low Voltage Bits [9:8]
R47	[7:0] Channel D Margin Low Bits [7:0]
R48	[7:4] Unused [3:2] Channel E Margin Low Vref Bits [1:0] [0:1] Channel E Margin Low Voltage Bits [9:8]
R49	[7:0] Channel E Margin Low Bits [7:0]
R4A	[7:4] Unused [3:2] Channel F Margin Low Vref Bits [1:0] [0:1] Channel F Margin Low Voltage Bits [9:8]
R4B	[7:0] Channel F Margin Low Bits [7:0]

R4C TO R7F	Unused
R80	[7] Channel A UV1 Triggers RST [6] Channel A UV1 Triggers HEALTHY [5] Channel A UV1 Triggers Power Off [4] Channel A UV1 Triggers Force Shutdown [3:2] Channel A UV1 Consecutive Conversions [1:0] UV1 - Channel A Low Limit 1 Bits [9:8]
R81	[7:0] Channel A Low Limit 1 Bits [7:0]
R82	[7] Channel A UV2 Triggers RST [6] Channel A UV2 Triggers HEALTHY [5] Channel A UV2 Triggers Power Off [4] Channel A UV2 Triggers Force Shutdown [3:2] Channel A UV2 Consecutive Conversions [1:0] UV1 - Channel A Low Limit 2 Bits [9:8]
R83	[7:0] Channel A Low Limit 2 Bits [7:0]
R84	[7] Channel A OV1 Triggers RST [6] Channel A OV1 Triggers HEALTHY [5] Channel A OV1 Triggers Power Off [4] Channel A OV1 Triggers Force Shutdown [3:2] Channel A OV1 Consecutive Conversions [1:0] UV1 - Channel A High Limit 1 Bits [9:8]
R85	[7:0] Channel A High Limit 1 Bits [7:0]
R86	[7] Channel A OV2 Triggers RST [6] Channel A OV2 Triggers HEALTHY [5] Channel A OV2 Triggers Power Off [4] Channel A OV2 Triggers Force Shutdown [3:2] Channel A OV2 Consecutive Conversions [1:0] UV1 - Channel A High Limit 2 Bits [9:8]
R87	[7:0] Channel A High Limit 2 Bits [7:0]
R88	[7] Channel B UV1 Triggers RST [6] Channel B UV1 Triggers HEALTHY [5] Channel B UV1 Triggers Power Off [4] Channel B UV1 Triggers Force Shutdown [3:2] Channel B UV1 Consecutive Conversions [1:0] UV1 - Channel B Low Limit 1 Bits [9:8]
R89	[7:0] Channel B Low Limit 1 Bits [7:0]
R8A	[7] Channel B UV2 Triggers RST [6] Channel B UV2 Triggers HEALTHY [5] Channel B UV2 Triggers Power Off [4] Channel B UV2 Triggers Force Shutdown [3:2] Channel B UV2 Consecutive Conversions [1:0] UV1 - Channel B Low Limit 2 Bits [9:8]

R8B	[7:0] Channel B Low Limit 2 Bits [7:0]
R8C	[7] Channel B OV1 Triggers RST [6] Channel B OV1 Triggers HEALTHY [5] Channel B OV1 Triggers Power Off [4] Channel B OV1 Triggers Force Shutdown [3:2] Channel B OV1 Consecutive Conversions [1:0] UV1 - Channel B High Limit 1 Bits [9:8]
R8D	[7:0] Channel B High Limit 1 Bits [7:0]
R8E	[7] Channel B OV2 Triggers RST [5] Channel B OV2 Triggers Power Off [6] Channel B OV2 Triggers HEALTHY [4] Channel B OV2 Triggers Force Shutdown [3:2] Channel B OV2 Consecutive Conversions [1:0] UV1 - Channel B High Limit 2 Bits [9:8]
R8F	[7:0] Channel B High Limit 2 Bits [7:0]
R90	[7] Channel C UV1 Triggers RST [6] Channel C UV1 Triggers HEALTHY [5] Channel C UV1 Triggers Power Off [4] Channel C UV1 Triggers Force Shutdown [3:2] Channel C UV1 Consecutive Conversions [1:0] UV1 - Channel C Low Limit 1 Bits [9:8]
R91	[7:0] Channel C Low Limit 1 Bits [7:0]
R92	[7] Channel C UV2 Triggers RST [6] Channel C UV2 Triggers HEALTHY [5] Channel C UV2 Triggers Power Off [4] Channel C UV2 Triggers Force Shutdown [3:2] Channel C UV2 Consecutive Conversions [1:0] UV1 - Channel C Low Limit 2 Bits [9:8]
R93	[7:0] Channel C Low Limit 2 Bits [7:0]
R94	[7] Channel C OV1 Triggers RST [6] Channel C OV1 Triggers HEALTHY [5] Channel C OV1 Triggers Power Off [4] Channel C OV1 Triggers Force Shutdown [3:2] Channel C OV1 Consecutive Conversions [1:0] UV1 - Channel C High Limit 1 Bits [9:8]
R95	[7:0] Channel C High Limit 1 Bits [7:0]
R96	[7] Channel C OV2 Triggers RST [6] Channel C OV2 Triggers HEALTHY [5] Channel C OV2 Triggers Power Off [4] Channel C OV2 Triggers Force Shutdown [3:2] Channel C OV2 Consecutive Conversions [1:0] UV1 - Channel C High Limit 2 Bits [9:8]
R97	[7:0] Channel C High Limit 2 Bits [7:0]

R98	[7] Channel D UV1 Triggers RST [6] Channel D UV1 Triggers HEALTHY [5] Channel D UV1 Triggers Power Off [4] Channel D UV1 Triggers Force Shutdown [3:2] Channel D UV1 Consecutive Conversions [1:0] UV1 - Channel D Low Limit 1 Bits [9:8]
R99	[7:0] Channel D Low Limit 1 Bits [7:0]
R9A	[7] Channel D UV2 Triggers RST [6] Channel D UV2 Triggers HEALTHY [5] Channel D UV2 Triggers Power Off [4] Channel D UV2 Triggers Force Shutdown [3:2] Channel D UV2 Consecutive Conversions [1:0] UV1 - Channel D Low Limit 2 Bits [9:8]
R9B	[7:0] Channel D Low Limit 2 Bits [7:0]
R9C	[7] Channel D OV1 Triggers RST [6] Channel D OV1 Triggers HEALTHY [5] Channel D OV1 Triggers Power Off [4] Channel D OV1 Triggers Force Shutdown [3:2] Channel D OV1 Consecutive Conversions [1:0] UV1 - Channel D High Limit 1 Bits [9:8]
R9D	[7:0] Channel D High Limit 1 Bits [7:0]
R9E	[7] Channel D OV2 Triggers RST [6] Channel D OV2 Triggers HEALTHY [5] Channel D OV2 Triggers Power Off [4] Channel D OV2 Triggers Force Shutdown [3:2] Channel D OV2 Consecutive Conversions [1:0] UV1 - Channel D High Limit 2 Bits [9:8]
R9F	[7:0] Channel D High Limit 2 Bits [7:0]
RA0	[7] Channel E UV1 Triggers RST [6] Channel E UV1 Triggers HEALTHY [5] Channel E UV1 Triggers Power Off [4] Channel E UV1 Triggers Force Shutdown [3:2] Channel E UV1 Consecutive Conversions [1:0] UV1 - Channel E Low Limit 1 Bits [9:8]
RA1	[7:0] Channel E Low Limit 1 Bits [7:0]
RA2	[7] Channel E UV2 Triggers RST [6] Channel E UV2 Triggers HEALTHY [5] Channel E UV2 Triggers Power Off [4] Channel E UV2 Triggers Force Shutdown [3:2] Channel E UV2 Consecutive Conversions [1:0] UV1 - Channel E Low Limit 2 Bits [9:8]
RA3	[7:0] Channel E Low Limit 2 Bits [7:0]

RA4	[7] Channel E OV1 Triggers RST [6] Channel E OV1 Triggers HEALTHY [5] Channel E OV1 Triggers Power Off [4] Channel E OV1 Triggers Force Shutdown [3:2] Channel E OV1 Consecutive Conversions [1:0] UV1 - Channel E High Limit 1 Bits [9:8]
RA5	[7:0] Channel E High Limit 1 Bits [7:0]
RA6	[7] Channel E OV2 Triggers RST [6] Channel E OV2 Triggers HEALTHY [5] Channel E OV2 Triggers Power Off [4] Channel E OV2 Triggers Force Shutdown [3:2] Channel E OV2 Consecutive Conversions [1:0] UV1 - Channel E High Limit 2 Bits [9:8]
RA7	[7:0] Channel E High Limit 2 Bits [7:0]
RA8	[7] Channel F UV1 Triggers RST [6] Channel F UV1 Triggers HEALTHY [5] Channel F UV1 Triggers Power Off [4] Channel F UV1 Triggers Force Shutdown [3:2] Channel F UV1 Consecutive Conversions [1:0] UV1 - Channel F Low Limit 1 Bits [9:8]
RA9	[7:0] Channel F Low Limit 1 Bits [7:0]
RAA	[7] Channel F UV2 Triggers RST [6] Channel F UV2 Triggers HEALTHY [5] Channel F UV2 Triggers Power Off [4] Channel F UV2 Triggers Force Shutdown [3:2] Channel F UV2 Consecutive Conversions [1:0] UV1 - Channel F Low Limit 2 Bits [9:8]
RAB	[7:0] Channel F Low Limit 2 Bits [7:0]
RAC	[7] Channel F OV1 Triggers RST [6] Channel F OV1 Triggers HEALTHY [5] Channel F OV1 Triggers Power Off [4] Channel F OV1 Triggers Force Shutdown [3:2] Channel F OV1 Consecutive Conversions [1:0] UV1 - Channel F High Limit 1 Bits [9:8]
RAD	[7:0] Channel F High Limit 1 Bits [7:0]
RAE	[7] Channel F OV2 Triggers RST [6] Channel F OV2 Triggers HEALTHY [5] Channel F OV2 Triggers Power Off [4] Channel F OV2 Triggers Force Shutdown [3:2] Channel F OV2 Consecutive Conversions [1:0] UV1 - Channel F High Limit 2 Bits [9:8]
RAF	[7:0] Channel F High Limit 2 Bits [7:0]

RB0	[7] VDD UV1 Triggers RST [6] VDD UV1 Triggers HEALTHY [5] VDD UV1 Triggers Power Off [4] VDD UV1 Triggers Force Shutdown [3:2] VDD UV1 Consecutive Conversions [1:0] UV1 - VDD Low Limit 1 Bits [9:8]
RB1	[7:0] VDD Low Limit 1 Bits [7:0]
RB2	[7] VDD UV2 Triggers RST [6] VDD UV2 Triggers HEALTHY [5] VDD UV2 Triggers Power Off [4] VDD UV2 Triggers Force Shutdown [3:2] VDD UV2 Consecutive Conversions [1:0] UV1 - VDD Low Limit 2 Bits [9:8]
RB3	[7:0] VDD Low Limit 2 Bits [7:0]
RB4	[7] VDD OV1 Triggers RST [6] VDD OV1 Triggers HEALTHY [5] VDD OV1 Triggers Power Off [4] VDD OV1 Triggers Force Shutdown [3:2] VDD OV1 Consecutive Conversions [1:0] UV1 - VDD High Limit 1 Bits [9:8]
RB5	[7:0] VDD High Limit 1 Bits [7:0]
RB6	[7] VDD OV2 Triggers RST [6] VDD OV2 Triggers HEALTHY [5] VDD OV2 Triggers Power Off [4] VDD OV2 Triggers Force Shutdown [3:2] VDD UV2 Consecutive Conversions [1:0] UV1 - VDD High Limit 2 Bits [9:8]
RB7	[7:0] Channel VDD High Limit 2 Bits [7:0]
RB8	[7] 12VIN UV1 Triggers RST [6] 12VIN UV1 Triggers HEALTHY [5] 12VIN UV1 Triggers Power Off [4] 12VIN UV1 Triggers Force Shutdown [3:2] 12VIN UV1 Consecutive Conversions [1:0] UV1 – 12VIN Low Limit 1 Bits [9:8]
RB9	[7:0] 12VIN Low Limit 1 Bits [7:0]
RBA	[7] 12VIN UV2 Triggers RST [6] 12VIN UV2 Triggers HEALTHY [5] 12VIN UV2 Triggers Power Off [4] 12VIN UV2 Triggers Force Shutdown [3:2] 12VIN UV2 Consecutive Conversions [1:0] UV1 – 12VIN Low Limit 2 Bits [9:8]
RBB	[7:0] Channel 12VIN Low Limit 2 Bits [7:0]

RBC	[7] 12VIN OV1 Triggers RST [6] 12VIN OV1 Triggers HEALTHY [5] 12VIN OV1 Triggers Power Off [4] 12VIN OV1 Triggers Force Shutdown [3:2] 12VIN OV1 Consecutive Conversions [1:0] UV1 – 12VIN High Limit 1 Bits [9:8]
RBD	[7:0] 12VIN High Limit 1 Bits [7:0]
RBE	[7] 12VIN OV2 Triggers RST [6] 12VIN OV2 Triggers HEALTHY [5] 12VIN OV2 Triggers Power Off [4] 12VIN OV2 Triggers Force Shutdown [3:2] 12VIN OV2 Consecutive Conversions [1:0] UV1 – 12VIN High Limit 2 Bits [9:8]
RBF	[7:0] Channel 12VIN High Limit 2 Bits [7:0]
RC0	[7] Internal Temp Sense UT1 Triggers RST [6] Internal Temp Sense UT1 Triggers HEALTHY [5] Internal Temp Sense UT1 Triggers Power Off [4] Internal Temp Sense UT1 Triggers Fault [3:2] Internal Temp Sense UT1 Consecutive Conversions [0:1] UV1 - Internal Temp Sense UT1 Bits [9:8]
RC1	[0:7] Internal Temp Sense UT1 Bits [7:0]
RC2	[7] Internal Temp Sense UT2 Triggers RST [6] Internal Temp Sense UT2 Triggers HEALTHY [5] Internal Temp Sense UT2 Triggers Power Off [4] Internal Temp Sense UT2 Triggers Fault [3:2] Internal Temp Sense UT2 Consecutive Conversions [0:1] Internal Temp Sense UT2 Bits [9:8]
RC3	[0:7] Internal Temp Sense UT2 Bits [7:0]
RC4	[7] Internal Temp Sense OT1 Triggers RST [6] Internal Temp Sense OT1 Triggers HEALTHY [5] Internal Temp Sense OT1 Triggers Power Off [4] Internal Temp Sense OT1 Triggers Fault [3:2] Internal Temp Sense OT1 Consecutive Conversions [0:1] Internal Temp Sense OT1 Bits [9:8]

RC5	[0:7] Internal Temp Sense OV1 Bits [7:0]
RC6	[7] Internal Temp Sense OT2 Triggers RST [6] Internal Temp Sense OT2 Triggers HEALTHY [5] Internal Temp Sense OT2 Triggers Power Off [4] Internal Temp Sense OT2 Triggers Fault [3:2] Internal Temp Sense OT2 Consecutive Conversions [0:1] Internal Temp Sense OT2 Bits [9:8]
RC7	[0:7] Internal Temp Sense OT2 Bits [7:0]
RC8	[7] AIN1 UV1 Triggers RST [6] AIN1 UV1 Triggers HEALTHY [5] AIN1 UV1 Triggers Power Off [4] AIN1 UV1 Triggers Fault [3:2] AIN1 UV1 Consecutive Conversions [0:1] AIN1 UV1 Bits [9:8]
RC9	[0:7] AIN1 UV1 Bits [7:0]
RCA	[7] AIN1 UV2 Triggers RST [6] AIN1 UV2 Triggers HEALTHY [5] AIN1 UV2 Triggers Power Off [4] AIN1 UV2 Triggers Fault [3:2] AIN1 UV2 Consecutive Conversions [0:1] AIN1 UV2 Bits [9:8]
RCB	[0:7] AIN1 UV2 Bits [7:0]
RCC	[7] AIN1 OV1 Triggers RST [6] AIN1 OV1 Triggers HEALTHY [5] AIN1 OV1 Triggers Power Off [4] AIN1 OV1 Triggers Fault [3:2] AIN1 OV1 Consecutive Conversions [0:1] AIN1 OV1 Bits [9:8]
RCD	[0:7] AIN1 OV1 Bits [7:0]
RCE	[7] AIN1 OV2 Triggers RST [6] AIN1 OV2 Triggers HEALTHY [5] AIN1 OV2 Triggers Power Off [4] AIN1 OV2 Triggers Fault [3:2] AIN1 OV2 Consecutive Conversions [0:1] AIN1 OV2 Bits [9:8]

RCF	[0:7] AIN1 OV2 Bits [7:0]
RD0	[7] AIN2 UV1 Triggers RST [6] AIN2 UV1 Triggers HEALTHY [5] AIN2 UV1 Triggers Power Off [4] AIN2 UV1 Triggers Fault [3:2] AIN2 UV1 Consecutive Conversions [0:1] AIN2 UV1 Bits [9:8]
RD1	[0:7] AIN2 UV1 Bits [7:0]
RD2	[7] AIN2 UV2 Triggers RST [6] AIN2 UV2 Triggers HEALTHY [5] AIN2 UV2 Triggers Power Off [4] AIN2 UV2 Triggers Fault [3:2] AIN2 UV2 Consecutive Conversions [0:1] AIN2 UV2 Bits [9:8]
RD3	[0:7] AIN2 UV2 Bits [7:0]
RD4	[7] AIN2 OV1 Triggers RST [6] AIN2 OV1 Triggers HEALTHY [5] AIN2 OV1 Triggers Power Off [4] AIN2 OV1 Triggers Fault [3:2] AIN2 OV1 Consecutive Conversions [0:1] AIN2 OV1 Bits [9:8]
RD5	[0:7] AIN2 OV1 Bits [7:0]
RD6	[7] AIN2 OV2 Triggers RST [6] AIN2 OV2 Triggers HEALTHY [5] AIN2 OV2 Triggers Power Off [4] AIN2 OV2 Triggers Fault [3:2] AIN2 OV2 Consecutive Conversions [0:1] AIN2 OV2 Bits [9:8]
RD7	[0:7] AIN2 OV2 Bits [7:0]
RD8 TO RDF	Unused
RE0	[7:4] Not Used but must be set to 0 [3:2] Channel A OFF Limit Consecutive Conversions [0:1] Channel A OFF Limit Bits [9:8]
RE1	[7:0] Channel A OFF Limit Bits [7:0]

RE2	[7:4] Not Used but must be set to 0 [3:2] Channel B OFF Limit Consecutive Conversions [0:1] Channel B OFF Limit Bits [9:8]
RE3	[7:0] Channel B OFF Limit Bits [7:0]
RE4	[7:4] Not Used but must be set to 0 [3:2] Channel C OFF Limit Consecutive Conversions [0:1] Channel C OFF Limit Bits [9:8]
RE5	[7:0] Channel C OFF Limit Bits [7:0]
RE6	[7:4] Not Used but must be set to 0 [3:2] Channel D OFF Limit Consecutive Conversions [0:1] Channel D OFF Limit Bits [9:8]
RE7	[7:0] Channel D OFF Limit Bits [7:0]
RE8	[7:4] Not Used but must be set to 0 [3:2] Channel E OFF Limit Consecutive Conversions [0:1] Channel E OFF Limit Bits [9:8]
RE9	[7:0] Channel E OFF Limit Bits [7:0]
REA	[7:4] Not Used but must be set to 0 [3:2] Channel F OFF Limit Consecutive Conversions [0:1] Channel F OFF Limit Bits [9:8]
REB	[7:0] Channel F OFF Limit Bits [7:0]

The following registers are accessed using slave address 1001 A2 A1 A0

R00	[7:3] = [00000]ADC channel for Channel A [2] = 0 [1:0] Bits [9:8] of ADC data for Channel A
R01	[7:0] Bits [7:0] of ADC data for Channel A
R02 to R07	Unused
R08	[7:3] = [00001]ADC channel for Channel B [2] = 0 [1:0] Bits [9:8] of ADC data for Channel B
R09	[7:0] Bits [7:0] of ADC data for Channel B
R1A to R1F	Unused
R10	[7:3] = [00010]ADC channel for Channel C [2] = 0 [1:0] Bits [9:8] of ADC data for Channel C
R11	[7:0] Bits [7:0] of ADC data for Channel C
R12 to R17	Unused
R18	[7:3] = [00011]ADC channel for Channel D [2] = 0 [1:0] Bits [9:8] of ADC data for Channel D
R19	[7:0] Bits [7:0] of ADC data for Channel D
R1A to R1F	Unused
R20	[7:3] = [00100]ADC channel for Channel E [2] = 0 [1:0] Bits [9:8] of ADC data for Channel E
R21	[7:0] Bits [7:0] of ADC data for Channel E
R22 to R27	Unused
R28	[7:3] = [00101]ADC channel for Channel F [2] = 0 [1:0] Bits [9:8] of ADC data for Channel F
R29	[7:0] Bits [7:0] of ADC data for Channel F

R2A to R2F	Unused
R30	[7:3] = [00110]ADC channel for Channel VDD [2] = 0 [1:0] Bits [9:8] of ADC data for Channel VDD
R31	[7:0] Bits [7:0] of ADC data for Channel VDD
R32 to R37	Unused
R38	[7:3] = [00111]ADC channel for Channel 12VIN [2] = 0 [1:0] Bits [9:8] of ADC data for Channel 12VIN
R39	[7:0] Bits [7:0] of ADC data for Channel 12VIN
R3A to R3F	Unused
R40	[7:3] = [01000]ADC channel for Channel INT_TEMP [2] = 0 [1:0] Bits [9:8] of ADC data for Channel INT_TEMP
R41	[7:0] Bits [7:0] of ADC data for Channel INT_TEMP
R42 to R47	Unused
R48	[7:3] = [01001]ADC channel for Channel AIN1 [2] = 0 [1:0] Bits [9:8] of ADC data for Channel AIN1
R49	[7:0] Bits [7:0] of ADC data for Channel AIN1
R4A to R4F	Unused
R50	[7:3] = [01010]ADC channel for Channel AIN2 [2] = 0 [1:0] Bits [9:8] of ADC data for Channel AIN2
R51	[7:0] Bits [7:0] of ADC data for Channel AIN2

R52 to R7F	Unused
R80	[7:5] I²C Commands: 000X XXXX Clear 100X XXXX I²C Power-On 010X XXXX I²C Power-Off 001X XXXX I²C Force Shutdown [4] Unused [3] Sequenced channels out of fault (read only) [2] Sequenced channels below off limit (read only) [1:0] Unused
R81	[7:3] Sequence Aborted [2] AIN2 Fault [1] AIN1 Fault [0] Int Temp Fault
R82	[7] 12VIN Fault [6] VDD Fault [5] Channel F Fault [4] Channel E Fault [3] Channel D Fault [2] Channel C Fault [1] Channel B Fault [0] Channel A Fault

R83	Unused
R84	[7:6] Unused [5] PUP F Polarity [4] PUP E Polarity [3] PUP D Polarity [2] PUP C Polarity [1] PUP B Polarity [0] PUP A Polarity
R85 (Read Only)	[7] DC Control Status [6] Unused [5:4] Channel A Margin Command Bits [3:2] Channel B Margin Command Bits [1:0] Channel C Margin Command Bits
R86 (Read Only)	[7] DC Control Status [6] Unused [5:4] Channel D Margin Command Bits [3:2] Channel E Margin Command Bits [1:0] Channel F Margin Command Bits
R87	[7:4] Write Protect Memory [3:0] Write Protect Config
R88	Status Tracking Code Revision