SMM150 Single-Channel Supply Voltage Marginer, Monitor and DC Output Controller Windows GUI Users Guide and Configuration Register Descriptions

Introduction

The information contained in Application Note 46 details the Configuration Register settings for the SMM150 single-channel supply voltage marginer and monitor. The SMM150 Windows Graphical User Interface (GUI) is also shown with the associated register and function highlighted as well as the general purpose memory array. For additional explanation on device functionality related to the configuration registers, refer to the SMM150 Data Sheet.

Register Formats and Functions

There are a total of 6 registers that are separated into four basic register types. The first are those that set a margin or nominal threshold where the binary value written to the register is used to compute an incremental voltage.

The second type enables or disables a function or selects between two specific functions. The third are command registers to immediately operate the SMM150 functions. The fourth register types are volatile and non-volatile status registers that record device conditions and device tracking codes.

The device type identifier for the memory array, the configuration registers and the command and status registers are accessible with the same slave address. It can be set to any 4-bit number as defined in Table 1. The bus address bits A[2:0] are hard wired through device address pins (A2, A1 and A0). The bus address accessed in the address byte of the serial data stream must match the setting of the SMM150 address pins. Non-volatile Configuration Registers are located in 00_{HEX} thru 05_{HEX} and volatile registers are located in 30_{HEX} thru $3E_{HEX}$. The General-Purpose Memory array is located in 40_{HEX} thru FF_{HEX} (Table2).

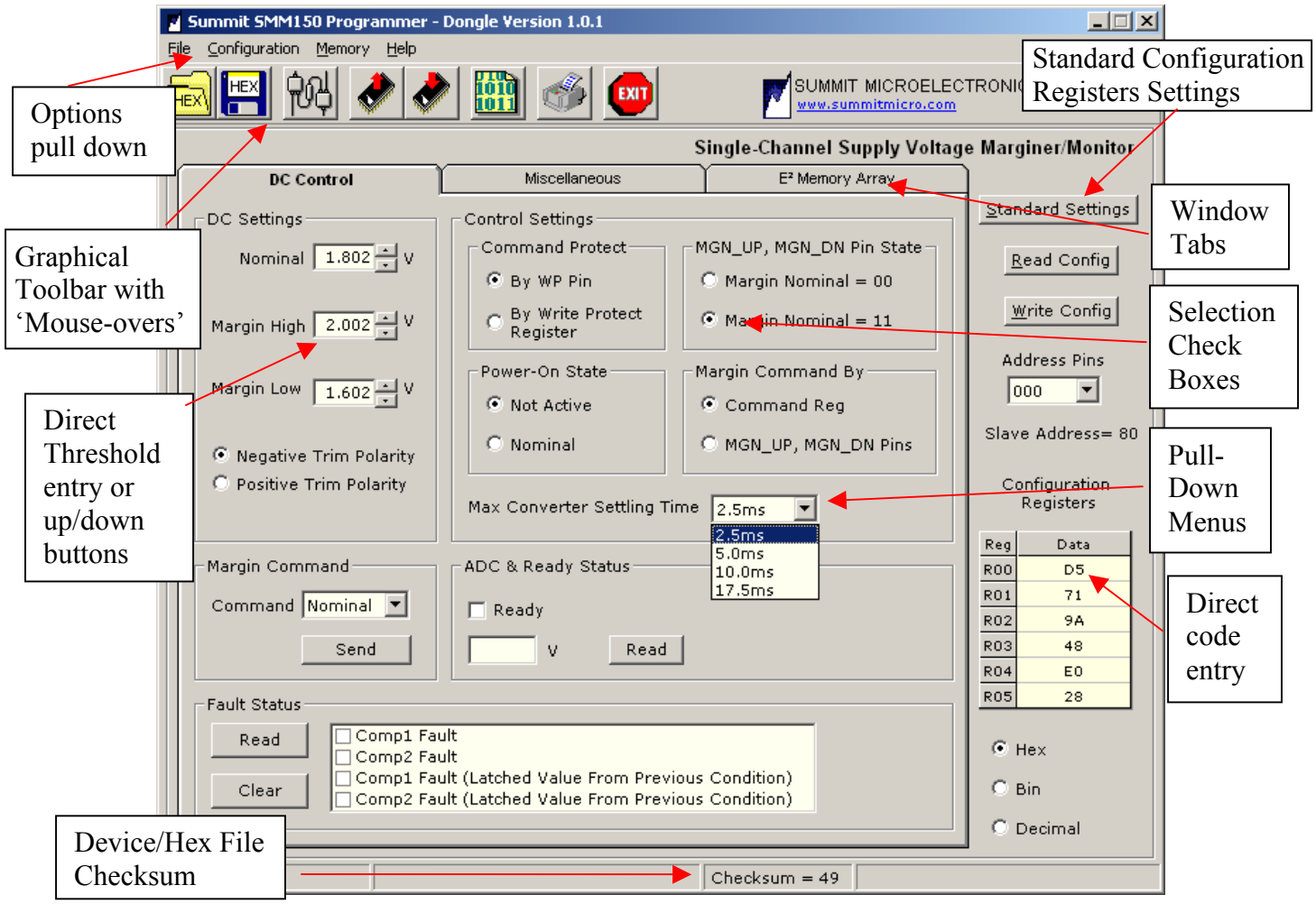

Figure 1 - SMM150 Windows GUI Features

SMM150 Windows Graphical User Interface

The SMM150 Windows GUI (Figure 1) is used with the SMX3200 programming 'Dongle'. It is an easy to use Graphical Interface that is compatible with Windows 95, 98, NT, 2000 and XP operating systems. The GUI consists of pull-down menus, check boxes, up/down buttons, etc. There are "mouse-overs" that define every function and an expert mode for directly entering data into the configuration registers. The GUI generates a checksum that can compare the programmed device configuration register values versus the hex contents.

Help Menu

The Help menu can be used to view the SMM150 Datasheet or this app note while prototyping with the Windows GUI. The 'About' selection menu shows the GUI version number. Please always go to the Summit web site (www.summitmicro.com) for the most current data sheet and GUI software. There are also options if applicable, to view GUI change notices and to check the web site directly for the most current GUI version.

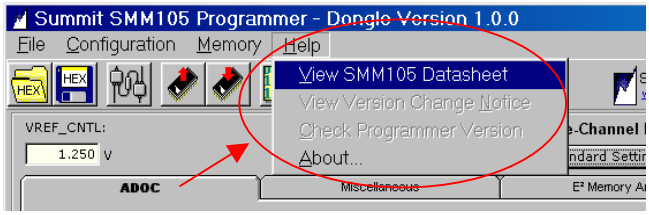

Figure 2 - Help Menu

Configuration Pull Down Menu

This menu (Figure 3A) has an option that will check for communications between the device and the PC. This selection should be tried first before changing any options. If the test passes, then all other options can be left in the default condition. If it doesn't pass, check all SMX3200 cable connections to the board and PC. If correct, then slow the I^2C clock frequency as described in the Setup Options paragraph below.

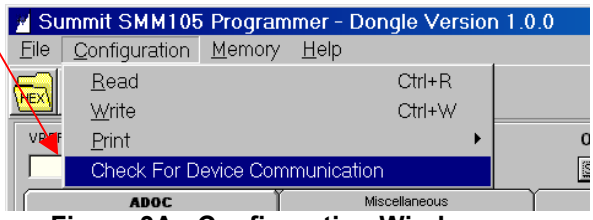

Figure 3A - Configuration Window

Setup Options

In the "File" pull-down menu (Figure 3B), there are options to set the I^2C clock frequency and delays before I^2C Read and Write operations. The default settings work with most PCs, so these settings are only for circumstances where the PC cannot communicate successfully with the SMX3200 programming 'Dongle'. The "Auto-Read Configuration/Memory After Write" check box enables a checksum test which compares the GUI hex settings or file to the programmed device at the end of a Write sequence. It does this by performing a Write immediately following a Read.

The "Keep Dongle Supply Voltage Active" check box is an option to keep the SMX3200 supply always on to power pull-up resistors on the SMM150 board. If the pull-ups are tied to another supply, the Dongle supply is turned on only during programming.

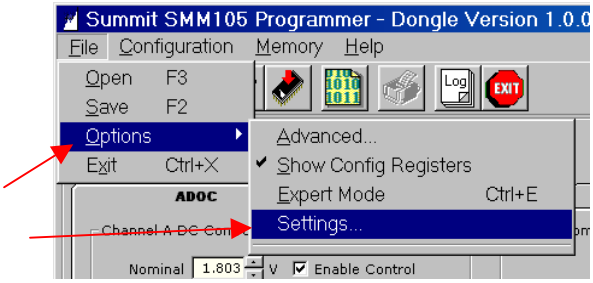

Figure 3B - Settings Window

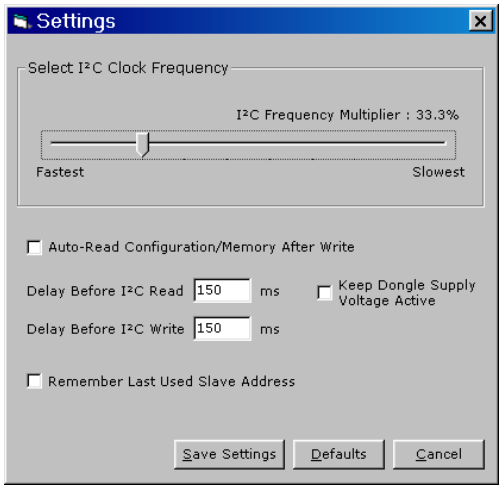

Figure 4 - Settings Options Window

Interfacing Options

The parallel Port Interfacing Window sets different options for programming the device. The 'Parallel Port Interfacing' should always be set to 'Dongle'. The 'Parallel Port Driver' can be changed for laptops if a problem is encountered in Win9X systems.

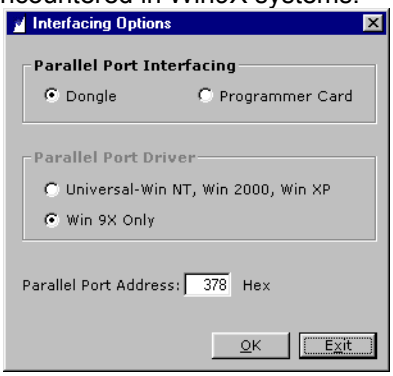

Figure 5 - Interfacing Options Window

Slave Address programmed as 10XX. The Slave address is set using the three address pins, which are three state inputs: 10 SAZ1 SAZ0 AZ2 AZ1 AZ0: (SAZ[1:0] and AZ[2:0] are defined by address pins A[2:0])

Pins A[2:0]				
A2	**A1**	**A0**	**Slave Address**	**Bus Address**
0	0	0	1000	000
0	0	1	1000	001
0	0	Z	1000	010
0	1	0	1000	100
0	1	1	1000	101
0	1	Z	1000	110
0	Z	X	1000	011
1	0	0	1001	000
1	0	1	1001	001
1	0	Z	1001	010
1	1	0	1001	100
1	1	1	1001	101
1	1	Z	1001	110
1	Z	X	1001	011
Z	0	0	1010	000
Z	0	1	1010	001
Z	0	Z	1010	010
Z	1	0	1010	100
Z	1	1	1010	101
Z	1	Z	1010	110
Z	Z	X	1010	011

Table 1 – Example device addresses allowed by the SMM150.

Slave Address	Bus Address	Register Type
10XX	A2 A1 A0	Configuration and Status Registers are located in: 00_{HEX} thru 05_{HEX} and 30_{HEX} thru $3E_{HEX}$
		General-Purpose Memory is located in 40_{HEX} thru FF_{HEX}

Table 2 - Address bytes used by the SMM150.

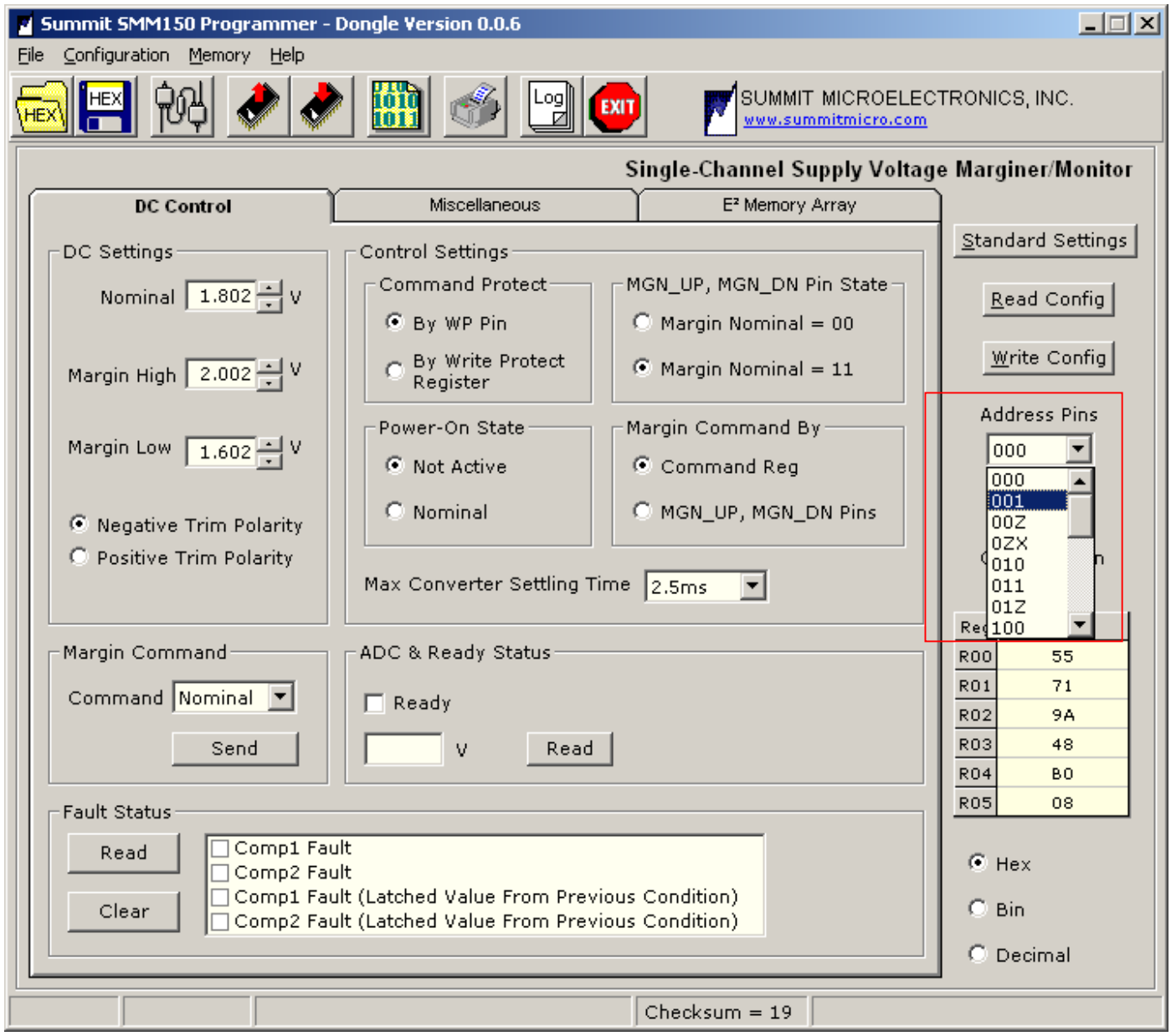

Figure 6 – Address pins Windows GUI Tab.

Register R00 - DC Control Nominal, Margin High, Margin Low Voltage and Glitch Filter Settings

Bits D[7:6] of this register sets the Glitch filter time. Also, Bits D[5:4], Bits D[3:2] and Bits D[1:0] are combined with Bits D[7:0] in corresponding registers R01, R2 and R3 to set the 10-bit DC Control voltage Nominal, High and Low values. An explanation that shows the formula for setting the DC Control voltage follows the register descriptions.

Register R00								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	0	X	X	X	X	X	X	Programmable glitch filter time = 0μs
0	1	X	X	X	X	X	X	Programmable glitch filter time = 15μs
1	0	X	X	X	X	X	X	Programmable glitch filter time = 40μs
1	1	X	X	X	X	X	X	Programmable glitch filter time = 120μs
X	X	C9	C8	X	X	X	X	Bits [9:8] of 10-bit DC Control Margin Low Setting (used with R03)
X	X	X	X	C9	C8	X	X	Bits [9:8] of 10-bit DC Control Margin High Setting (used with R02)
X	X	X	X	X	X	C9	C8	Bits [9:8] of 10-bit DC Control Margin Nominal Setting (used with R01)

Register R01, R02, R03 - DC Control Nominal, Margin High, Margin Low Voltage Settings

These register bits are combined with the register R00 to set the DC Control voltage value. R01 sets margin Nominal, R02 sets margin High and R03 sets the margin Low value.

Register R01, R02, R03								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	C6	C5	C4	C3	C2	C1	C0	Bits [7:0] of 10-bit DC Control Setting lower bits (see formula below)

The DC Control Voltage setting bits (C[9:0]) set the margin voltage using the following formula:

Margin Voltage = $(C[9:0]_{DEC}/1023)X5$

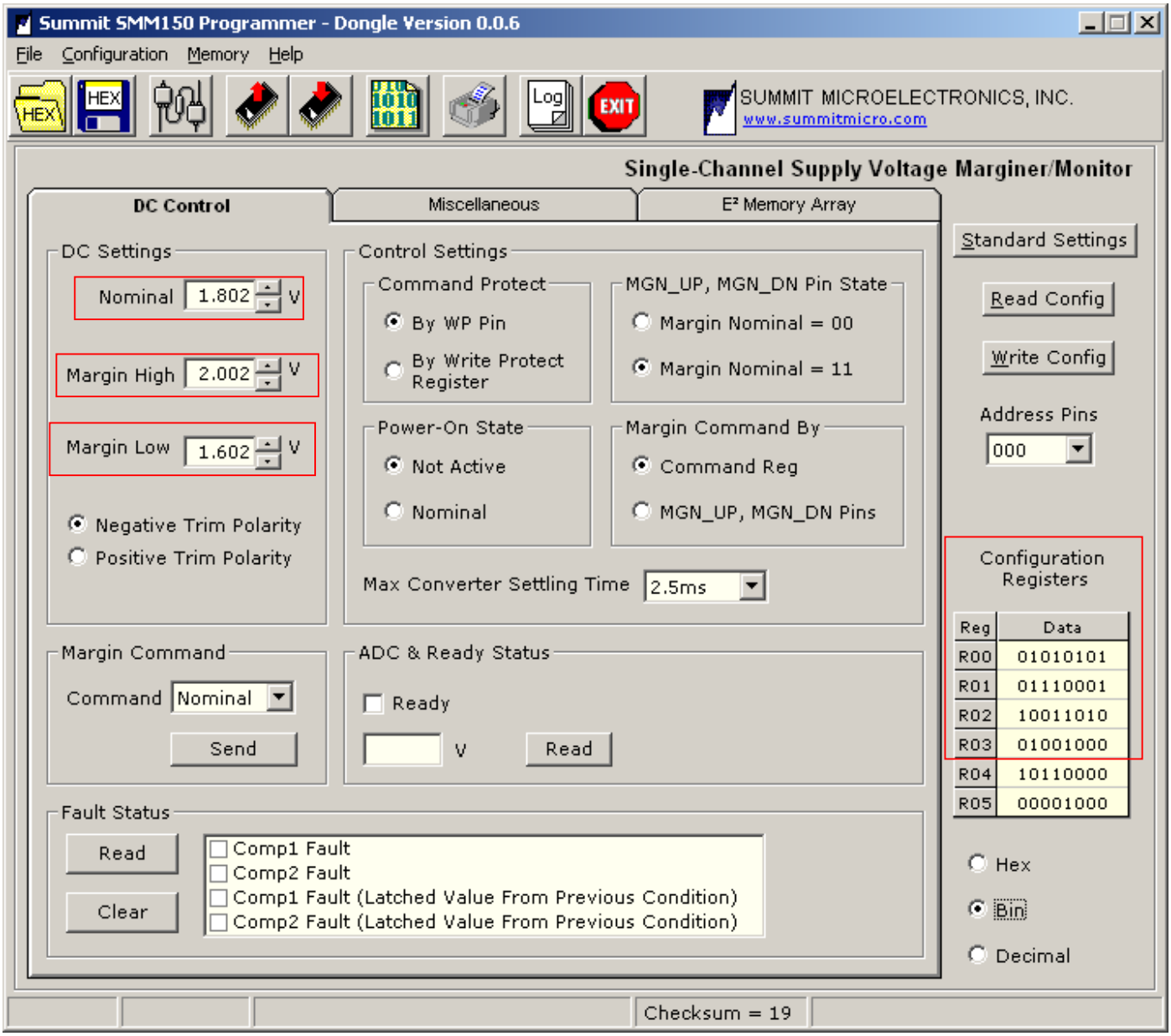

Figure 7 - Register R00, R01, R02, R03 DC Control Value setting Windows GUI Tab.

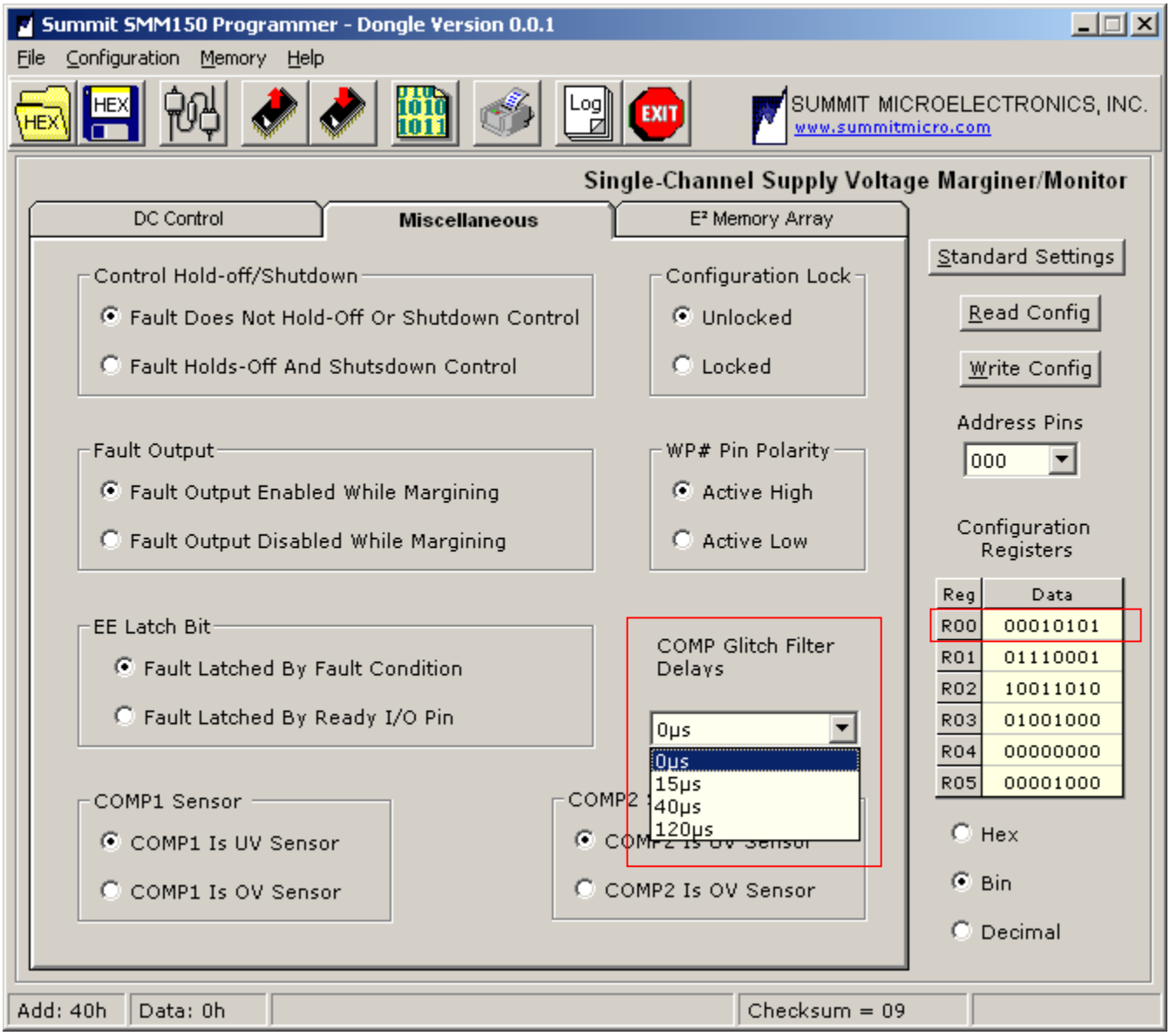

Figure 8 - Register R00 COMP1/2 Glitch Filter Delays GUI Tab.

Register R04 – Fault Latching Event, Fast Convergence, DC Control Enabling, TRIM Pin Polarity

Bit D[7] of this register selects fault on or off during margining, Bit D[6] selects the latching event. Bit D[5:4] sets COMP1/2 as either OV or UV sensors. Bit D[3] sets if the Configuration registers are locked or unlocked. Bits D[2] is unused and should be set to 0. . Bit D[1] selects the polarity of the TRIM pin for use with different types of converters and Bit D[0] selects if a fault shuts down the dc control or not.

Register R04								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**X**	**X**	**X**	**X**	**X**	**X**	**X**	Allow Faults while margining
1	**X**	**X**	**X**	**X**	**X**	**X**	**X**	Disables Faults while margining
X	**0**	**X**	**X**	**X**	**X**	**X**	**X**	Latch on Fault active
X	**1**	**X**	**X**	**X**	**X**	**X**	**X**	Latch on Ready pulled low
X	**X**	**0**	**X**	**X**	**X**	**X**	**X**	COMP2 is a UV sensor
X	**X**	**1**	**X**	**X**	**X**	**X**	**X**	COMP2 is a OV sensor
X	**X**	**X**	**0**	**X**	**X**	**X**	**X**	COMP1 is a UV sensor
X	**X**	**X**	**1**	**X**	**X**	**X**	**X**	COMP1 is a OV sensor
X	**X**	**X**	**X**	**0**	**X**	**X**	**X**	Configuration registers unlocked
X	**X**	**X**	**X**	**1**	**X**	**X**	**X**	Configuration registers locked
X	**X**	**X**	**X**	**X**	**0**	**X**	**X**	Unused (set to 0)
X	**X**	**X**	**X**	**X**	**X**	**0**	**X**	TRIM pin negative polarity
X	**X**	**X**	**X**	**X**	**X**	**1**	**X**	TRIM pin positive polarity
X	**X**	**X**	**X**	**X**	**X**	**X**	**0**	Fault does not hold-off and shut down control
X	**X**	**X**	**X**	**X**	**X**	**X**	**1**	Fault holds-off and shuts down control

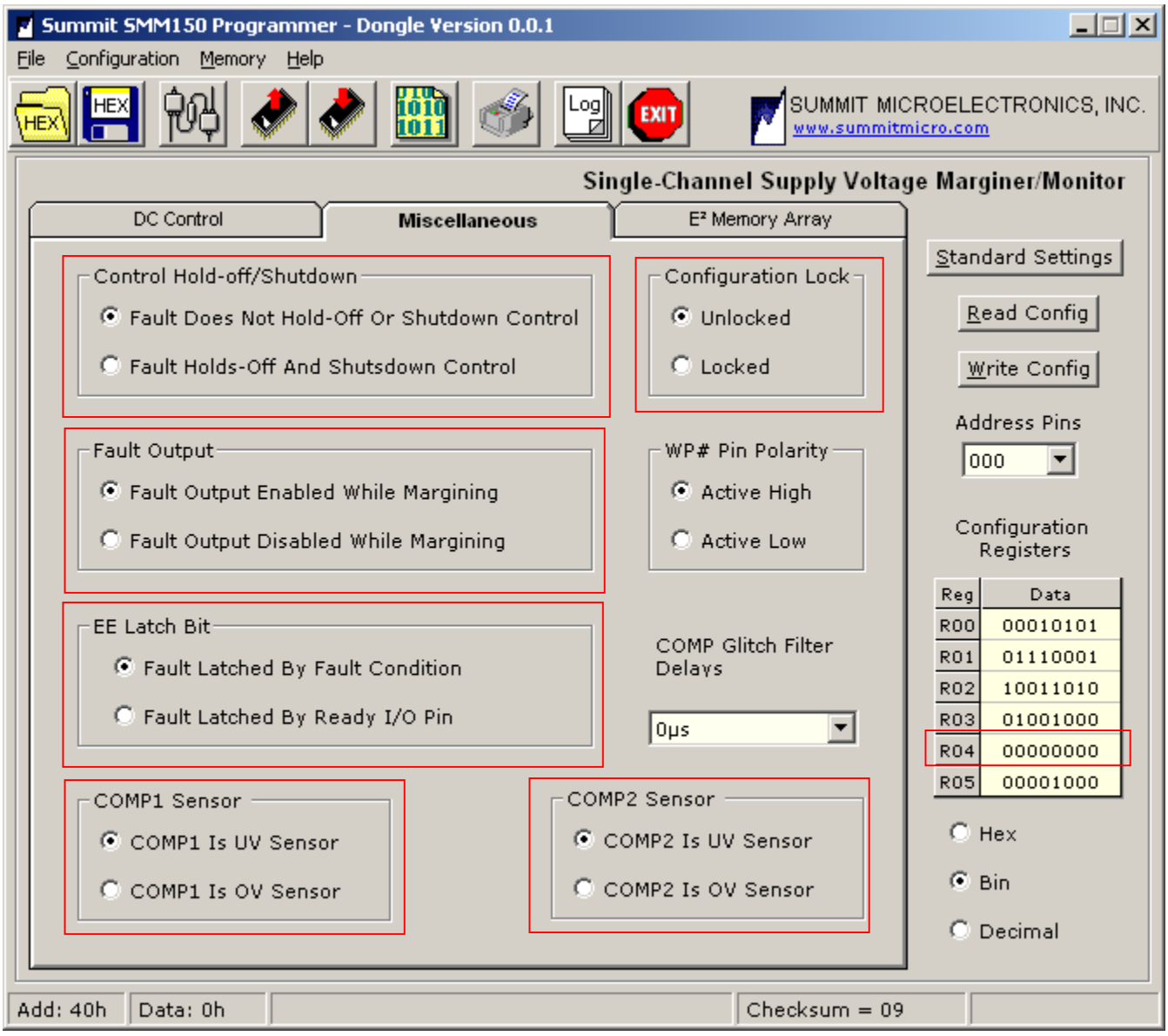

Figure 9 - Register R04 MISC Windows GUI Tab

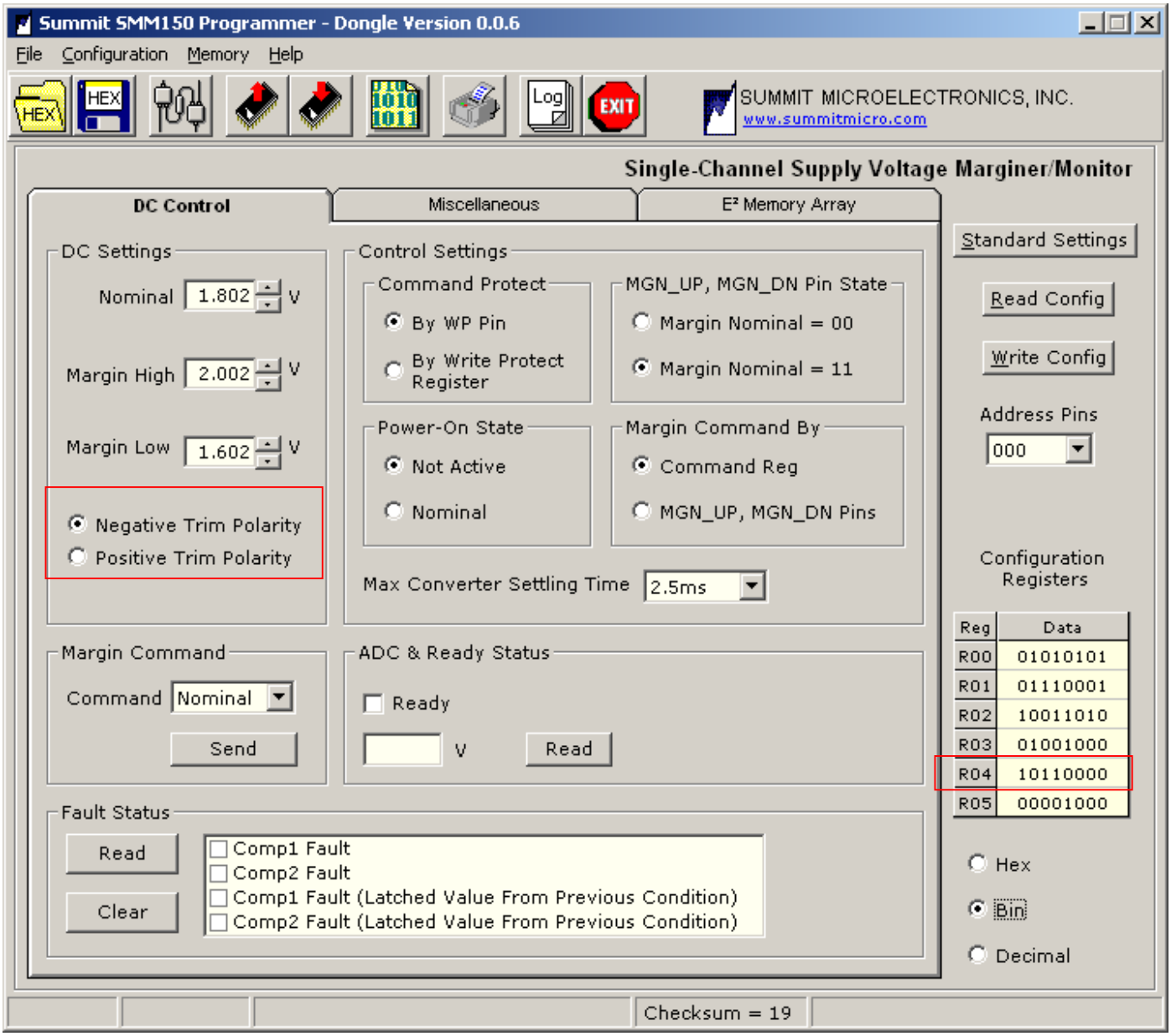

Figure 10 - Register R04 Trim polarity GUI Tab

Register R05 – Margin Commands, power on state, WP polarity and margin delay time

Bit D[7] of this register selects Write protect during margining command to be set by the WP pin or by the Write Protect register, Bit D[6] selects the margin command source. Bit D[5] selects the COMP1/2 VREF value. Bit D[4] sets the power-on state of the margin command register. Bit D[3] sets the state of the MUP and MDN pins. Bits D[2] set the polarity of the WP pin. . Bits D[1:0] selects the active margin command delay time.

Register R05								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**X**	**X**	**X**	**X**	**X**	**X**	**X**	Margin Command Write Protected by WP pin
1	**X**	**X**	**X**	**X**	**X**	**X**	**X**	Margin Command Write Protected by Write protect register
X	**0**	**X**	**X**	**X**	**X**	**X**	**X**	Margin Command uses command register
X	**1**	**X**	**X**	**X**	**X**	**X**	**X**	Margin Command controlled by MUP, MDN pins
X	**X**	**0**	**X**	**X**	**X**	**X**	**X**	VREF (COMP1/2) set for 0.5V
X	**X**	**1**	**X**	**X**	**X**	**X**	**X**	VREF (COMP1/2) set for 1.25V
X	**X**	**X**	**0**	**X**	**X**	**X**	**X**	Power-On State of Margin Command Register not active
X	**X**	**X**	**1**	**X**	**X**	**X**	**X**	Power-On State of Margin Command Register margin nominal
X	**X**	**X**	**X**	**0**	**X**	**X**	**X**	MUP, MDN pin state Margin Nominal = 00
X	**X**	**X**	**X**	**1**	**X**	**X**	**X**	MUP, MDN pin state Margin Nominal = 11
X	**X**	**X**	**X**	**X**	**0**	**X**	**X**	WP Pin Polarity active low
X	**X**	**X**	**X**	**X**	**1**	**X**	**X**	WP Pin Polarity active high
X	**X**	**X**	**X**	**X**	**X**	**0**	**0**	Active Margin Command Delay Time = 2.5ms
X	**X**	**X**	**X**	**X**	**X**	**0**	**1**	Active Margin Command Delay Time = 5.0ms
X	**X**	**X**	**X**	**X**	**X**	**1**	**0**	Active Margin Command Delay Time = 10ms
X	**X**	**X**	**X**	**X**	**X**	**1**	**1**	Active Margin Command Delay Time = 17.5ms

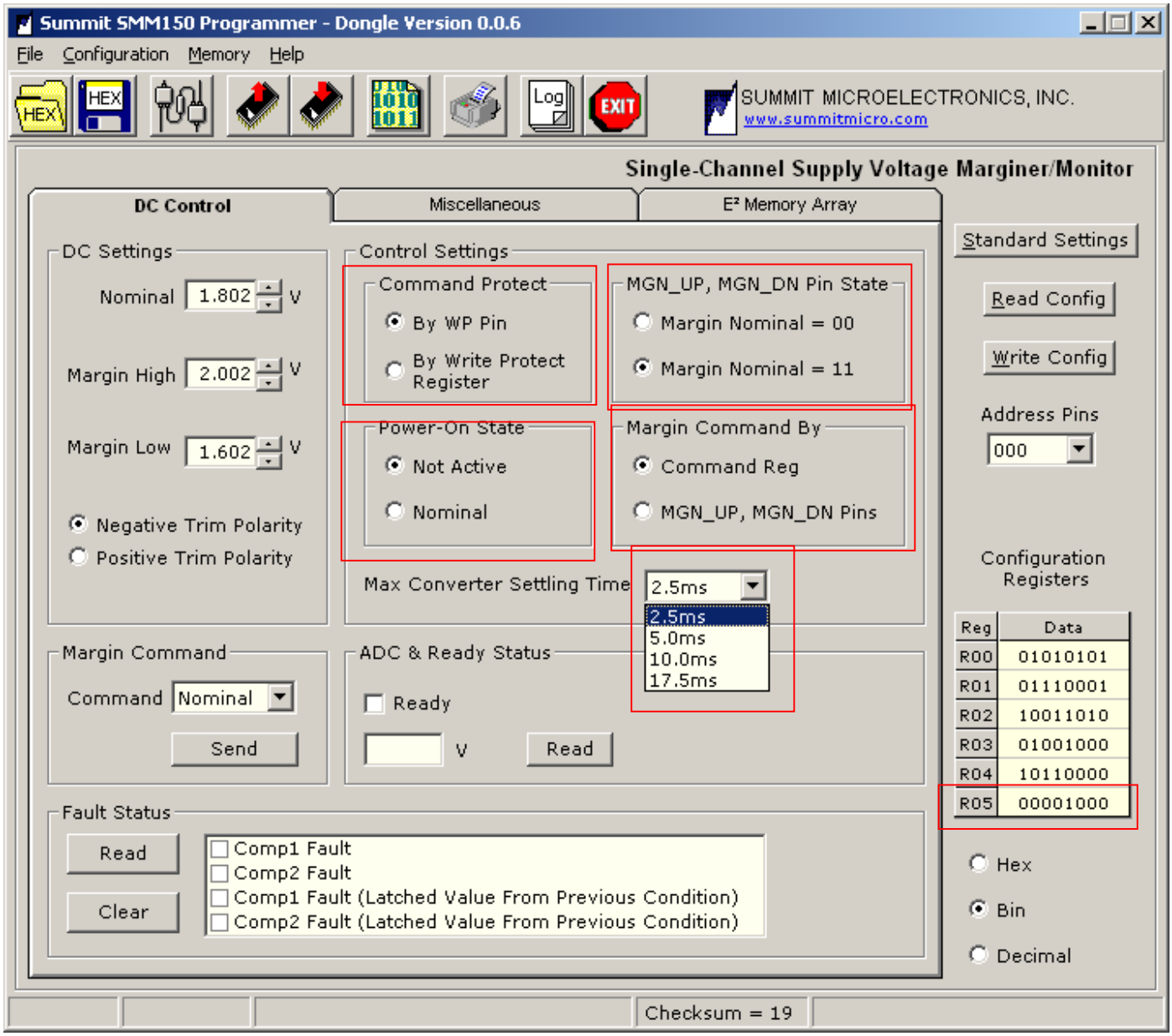

Figure 11 - Register R05 Margin Commands, power on state, WP polarity and margin delay time window.

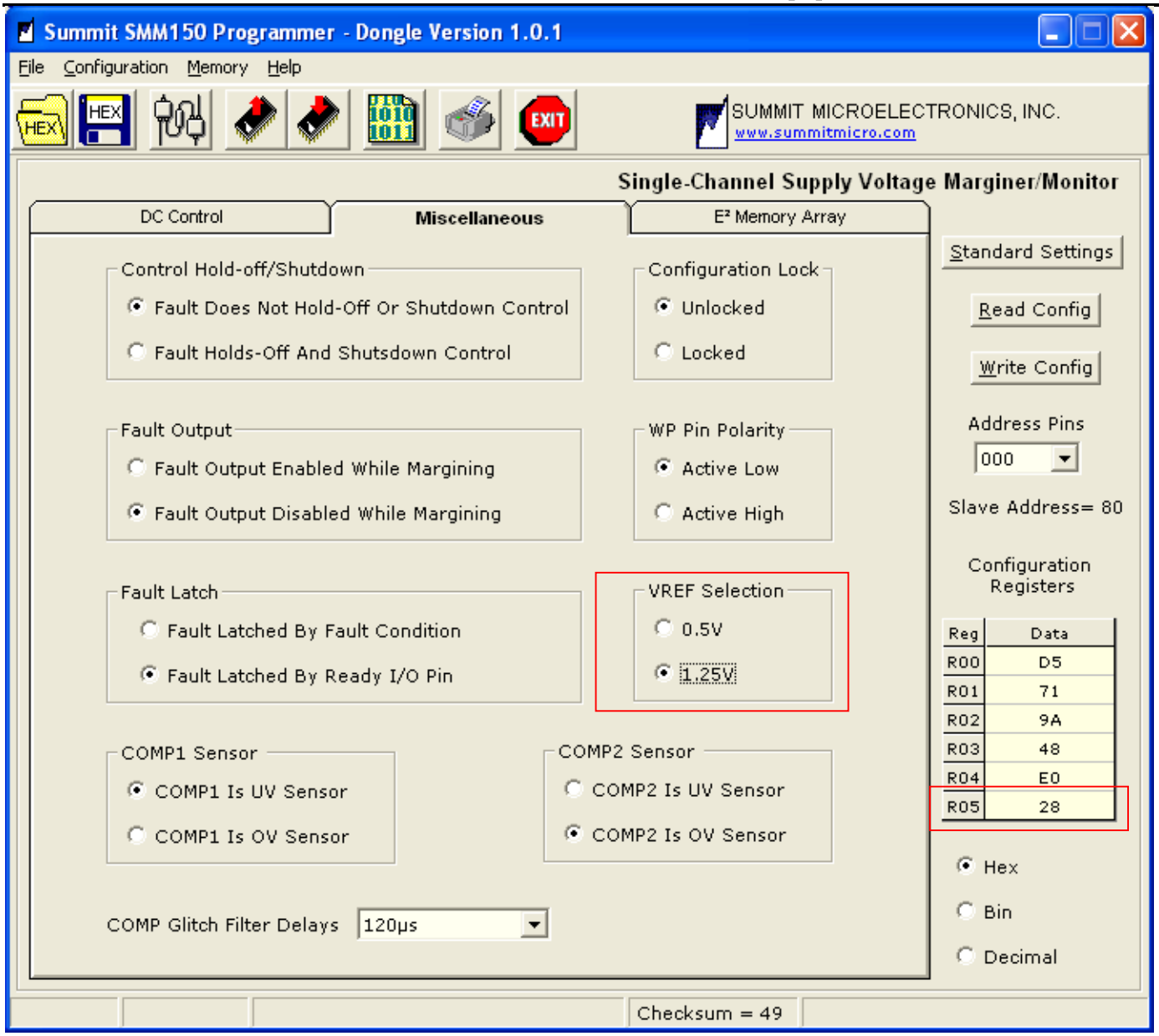

Figure 12 - Register R05 VREF selection.

Register R30, R32, R34, R36 – (Read Only, Requires 2 Byte Read) Ready Status, ADC read results
Bits D[7:6] and D[4:2] are unused and should be set to 0. Bit D[5] indicates Ready status. Bits D[1:0] are combined with Bits D[7:0] in corresponding registers R31, R33, R35 and R37 to read the 10-bit ADC VM Voltage value. An explanation that shows the formula for obtaining the ADC VM voltage follows the register descriptions below.

Register R30, R32, R34, R36								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**X**	**X**	**X**	**X**	**X**	**X**	Unused (set to 0)
X	**X**	**0**	**X**	**X**	**X**	**X**	**X**	Ready Status Inactive
X	**0**	**1**	**X**	**X**	**X**	**X**	**X**	Ready Status Active
X	**X**	**X**	**0**	**0**	**0**	**X**	**X**	Unused (set to 0)
X	**X**	**X**	**X**	**X**	**X**	**D9**	**D8**	ADC Result Bits [9:8]

Register R31, R33, R35, R37 – (Read Only, Requires 2 Byte Read) ADC read results
These register bits are combined with the register R30, R32, R34 and R36 to set the ADC VM voltage value.

Register R31, R33, R35, R37								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	ADC Result Bits [7:0]

The ADC VIN Voltage setting bits (C[9:0]) return the ADC voltage reading using the following formula:

ADC VM Voltage = $(C[9:0]_{DEC}/1023)X5$

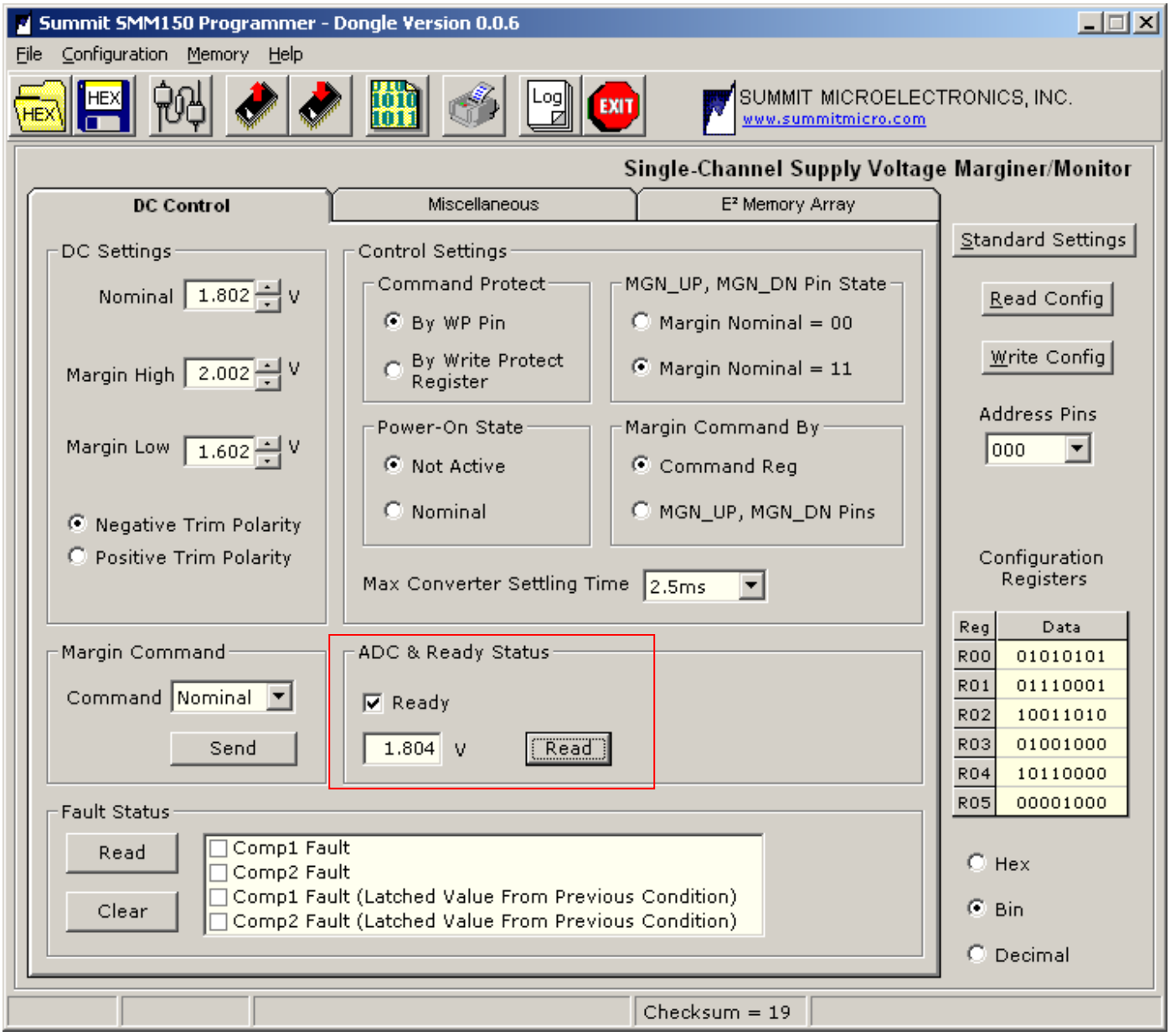

Figure 13 - Register R30, R32, R34, R36, R31, R33, R35, R37 ADC reading and Ready status Windows GUI Tab

Register R38 – (Write Only, Requires 2 Byte Read) Write protect

Bits D[7:4] defaults to write protect memory pages 40 to FF and Bits D[3:0] defaults to write protect configuration registers pages 00 to 3F unless the bits below are written to the corresponding format.

Register R38								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
X	**X**	**X**	**X**	**X**	**X**	**X**	**X**	Write Protect Memory (pages 4-F)
0	**1**	**0**	**1**	**X**	**X**	**X**	**X**	No Write Protect Memory (pages 4-F)
X	**X**	**X**	**X**	**X**	**X**	**X**	**X**	Write Protect Configuration (pages 0–3)
X	**X**	**X**	**X**	**0**	**1**	**0**	**1**	No Write Protect Configuration (pages 0–3)

Register R39 – DC Control Command (Write Only - used with R05 Configuration register)

Writing to this register constitutes a DC Control Command. This command initiates control to the desired DC Control Mode voltage.

Register R39								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**0**	**0**	**0**	**0**	**X**	**X**	Unused (set to 0)
X	**X**	**X**	**X**	**X**	**X**	**0**	**0**	Margin OFF (R05[4]=0)
X	**X**	**X**	**X**	**X**	**X**	**0**	**0**	Margin Nominal Command (R05[4]=1)
X	**X**	**X**	**X**	**X**	**X**	**0**	**1**	Margin Low Command
X	**X**	**X**	**X**	**X**	**X**	**1**	**0**	Margin High Command
X	**X**	**X**	**X**	**X**	**X**	**1**	**1**	Margin Nominal Command (R05[4]=0)
X	**X**	**X**	**X**	**X**	**X**	**1**	**1**	Margin OFF (R05[4]=1)

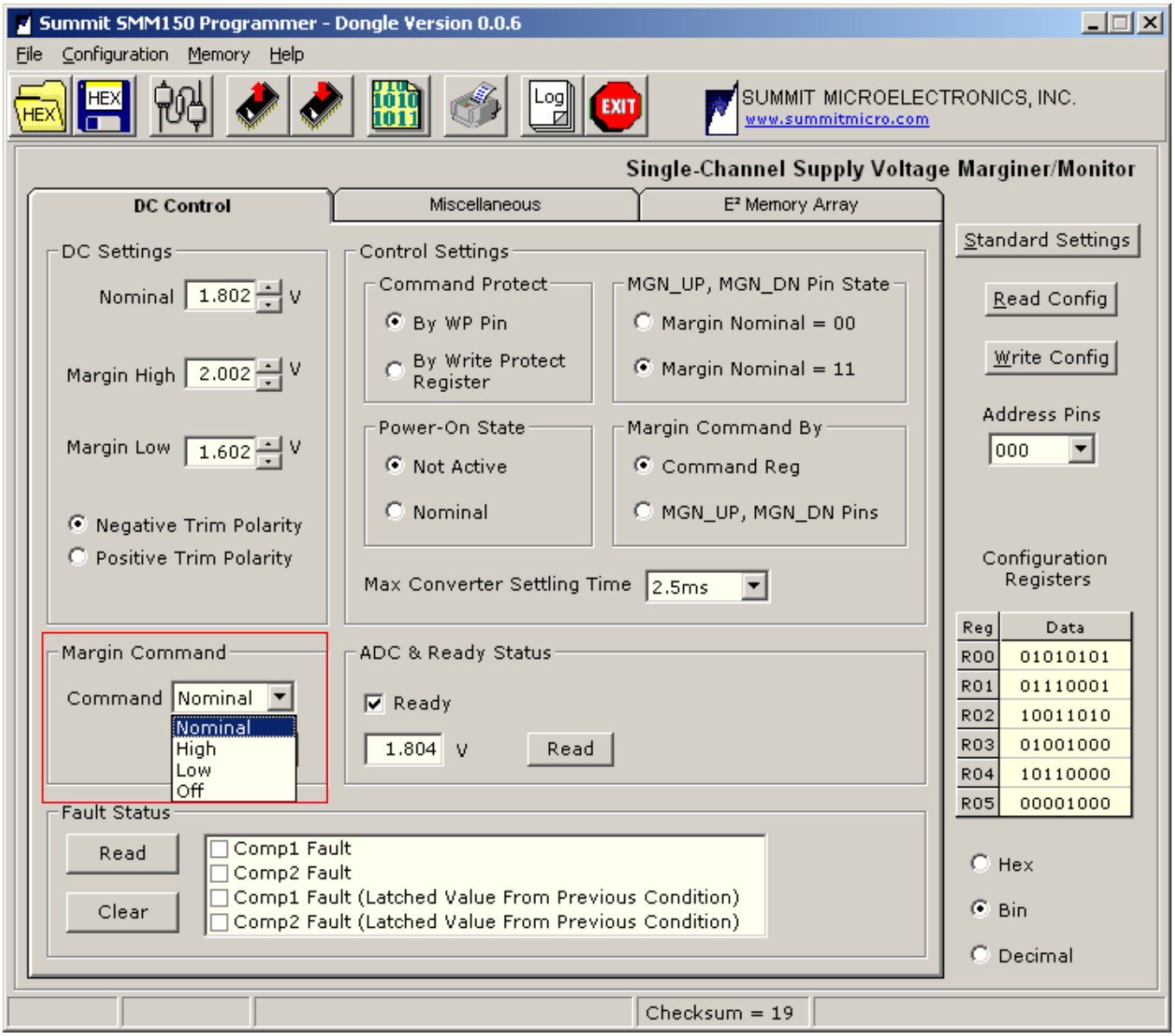

Figure 14 - Register R39 Margin command Windows GUI Tab

Register R3A – COMP1/2 Fault Status

Bits D[7:4] are unused and should be set to 0. Bit D[3] indicates COMP1 Fault status. Bit D[2] indicates COMP2 Fault status. Bit D[1] indicates COMP1 Latched Fault status. Bit D[0] indicates COMP2 Latched Fault status.

Register R3A								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**0**	**0**	**X**	**X**	**X**	**X**	Unused (set to 0)
X	**X**	**X**	**X**	**0**	**X**	**X**	**X**	COMP1 Fault Status – not in Fault
X	**X**	**X**	**X**	**1**	**X**	**X**	**X**	COMP1 Fault Status – in Fault
X	**X**	**X**	**X**	**X**	**0**	**X**	**X**	COMP2 Fault Status – not in Fault
X	**X**	**X**	**X**	**X**	**1**	**X**	**X**	COMP2 Fault Status – in Fault
X	**X**	**X**	**X**	**X**	**X**	**0**	**X**	COMP1 Latched Fault Status – not in Fault
X	**X**	**X**	**X**	**X**	**X**	**1**	**X**	COMP1 Latched Fault Status – in Fault
X	**X**	**X**	**X**	**X**	**X**	**X**	**0**	COMP2 Latched Fault Status – not in Fault
X	**X**	**X**	**X**	**X**	**X**	**X**	**1**	COMP2 Latched Fault Status – in Fault

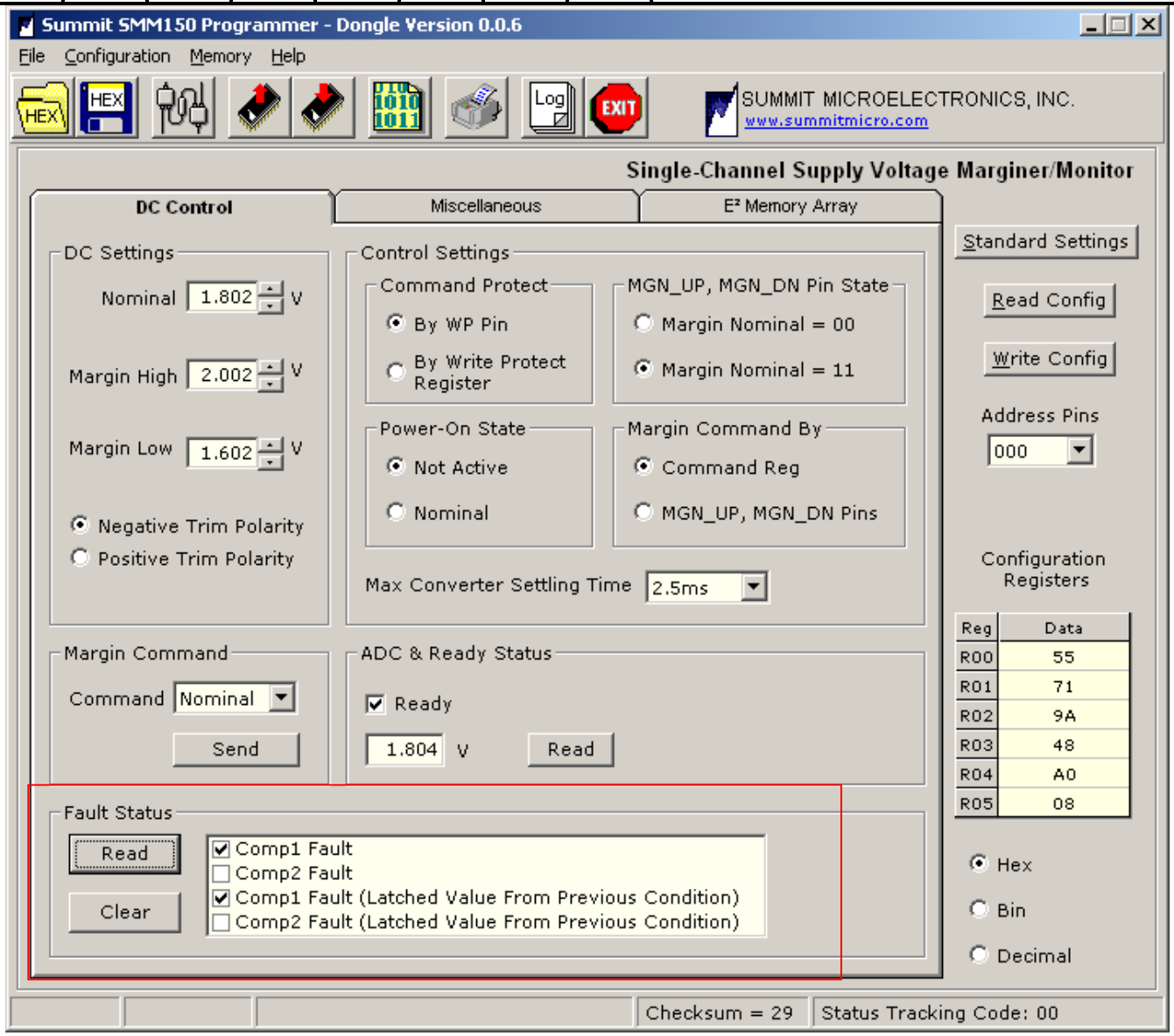

Figure 15 - Register R3A COMP1/2 Fault Status Windows GUI Tab

Register R3E – STATUS TRACKING CODE Identification – Read Only

Identifying the "STATUS TRACKING CODE" of the SMM150 is accomplished by reading register R3E, D0 through D7. The command is also available in the Configuration pull down menu. After the GUI determines the code, only the programming options available for that code are shown in the Windows GUI. An additional Session Log Window will appear with further information regarding the Status Tracking Code. The status code will only appear if an actual device is read by the GUI, otherwise it will return "XX".

Register R43								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	Status Tracking Code 00
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**	Status Tracking Code 03

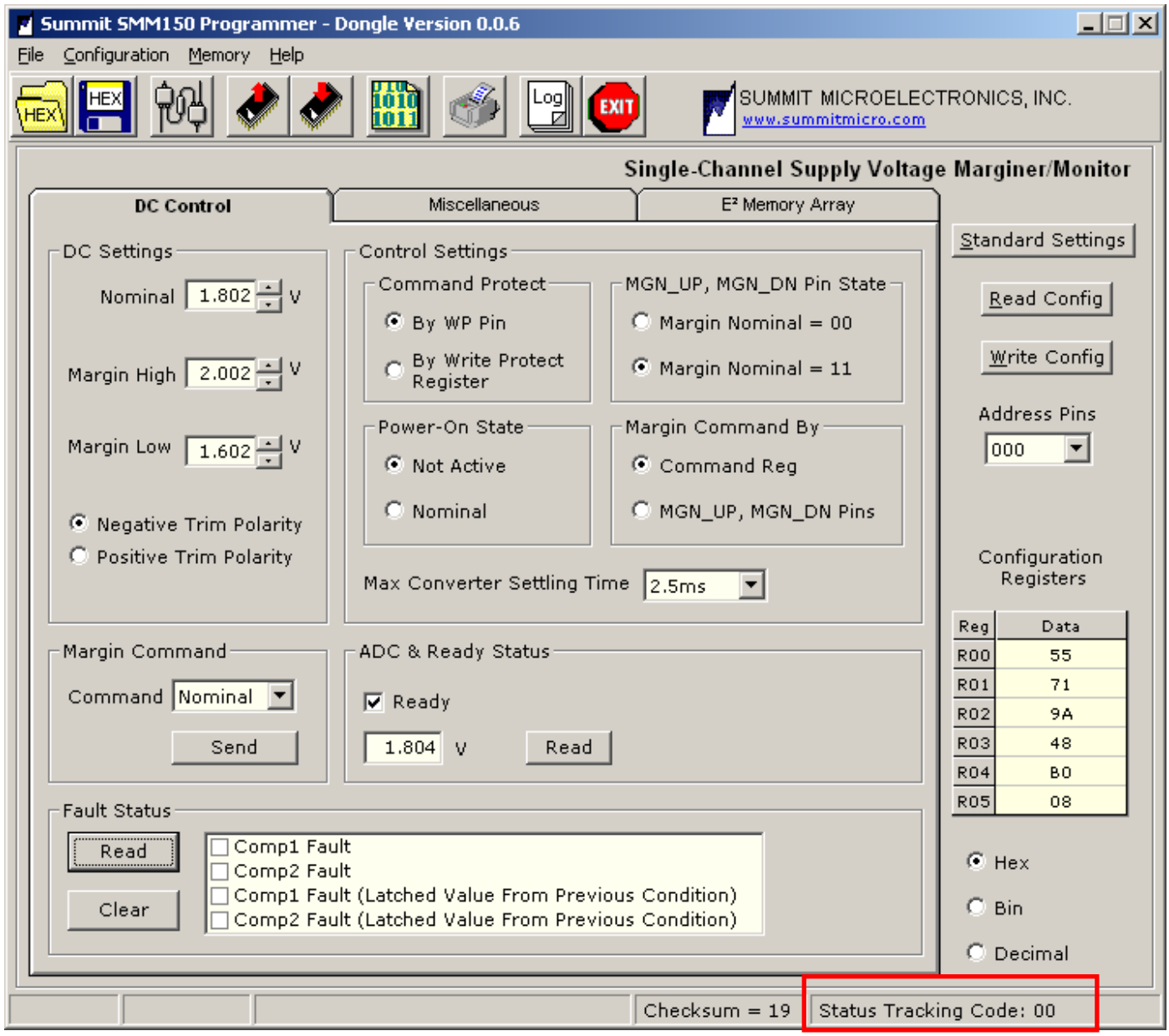

Figure 16 - Register R3E Status Tracking Code Windows GUI Tab

1k Nonvolatile Memory Array

The general-Purpose Memory array is located at address 40_{HEX} thru FF_{HEX}

The memory array can be updated by writing data directly into the memory location. To write into a specific location, go to the Hex column location in the Tabular view. Type in the new data and then press the 'Enter' key.

A graphic view of the memory can also be displayed for test purposes to check that the entire memory contents has changed or by writing pages or bytes, etc. using the buttons in the Graphic View Memory window.

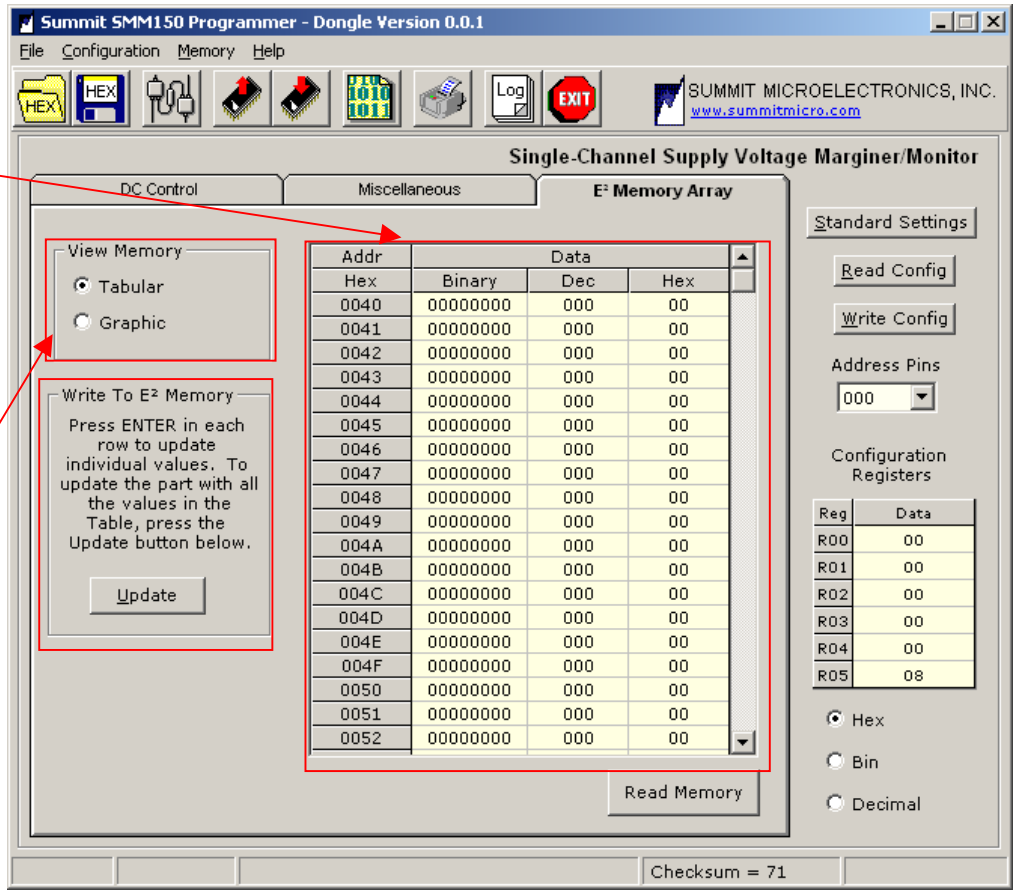

Figure 17 – E^2 Memory Array Windows GUI TAB.

NOTICE