SMS66 Six-Channel Power Supply Supervisor and Cascade Sequence Controller Windows GUI Users Guide and Configuration Register Descriptions

Introduction

The information contained in Application Note 43 details the Configuration Register settings for the SMS66 six-channel supply monitor, controller and sequencer. The SMS66 Windows Graphical User Interface (GUI) is also shown with the associated register and function highlighted. For additional explanation on device functionality related to the configuration registers, refer to the SMS66 Data Sheet.

Register Formats and Functions

There are a total of 142 registers that are separated into five basic register types. The first are those that set a monitoring threshold where the binary value written to the register is used to compute an incremental voltage. The second type enables or disables a function or selects between two specific functions. The third register type allows selection of various timeout intervals or other values. These are not incremental, like the thresholds, but specific bit patterns select specific timer or other values. The fourth register type are volatile status registers that record device conditions. The fifth register type is a volatile Read/Write register that allows I^2C software power-on or power-off control of all SMS66 channels. The device responds to two different slave addresses on the I^2C bus. The general purpose memory responds to slave address 1010_{BIN} or 1011_{BIN}; the configuration and software registers respond to slave address 1010_{BIN} or 1011_{BIN}.

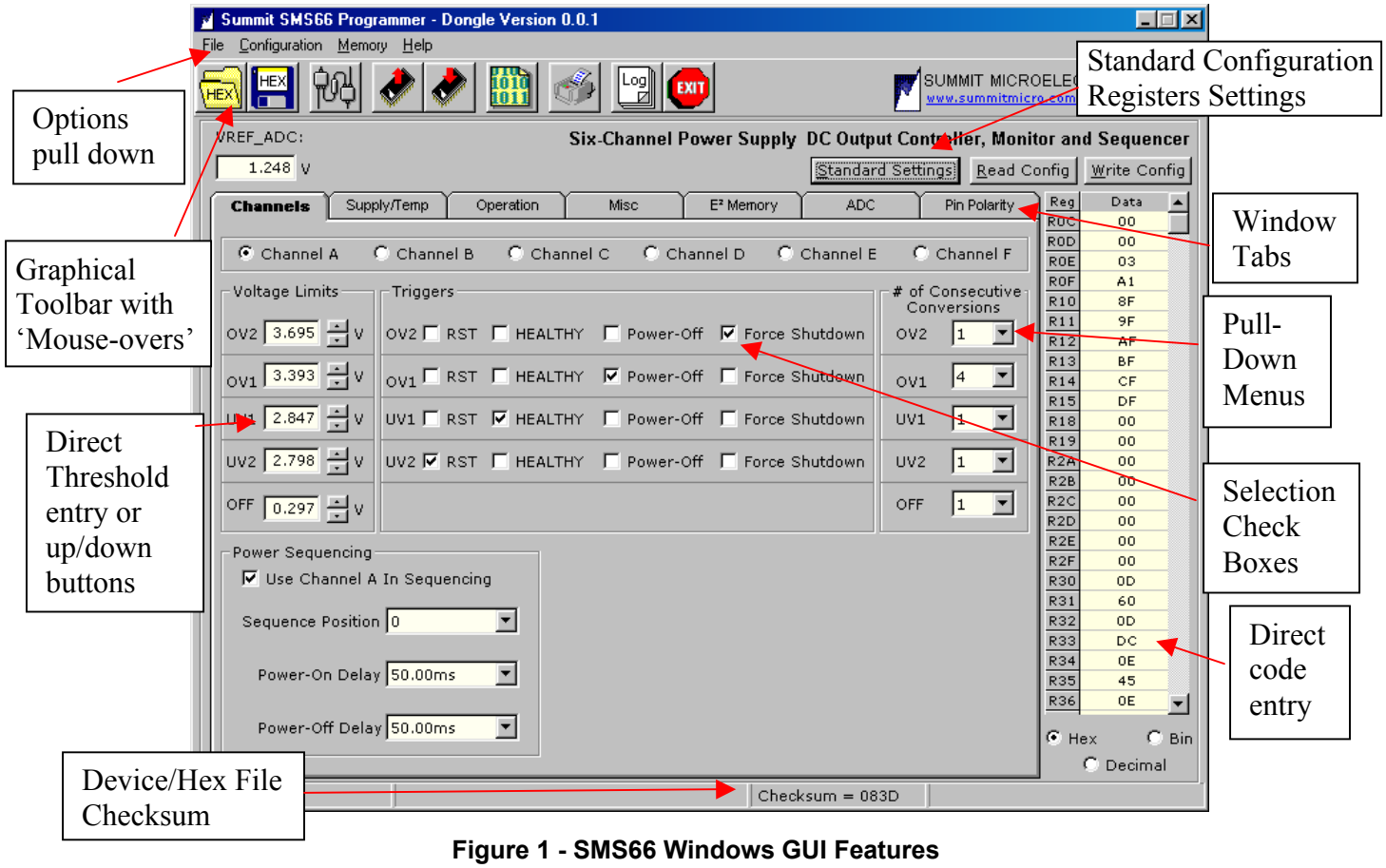

Figure 1 - SMS66 Windows GUI Features

SMS66 Windows Graphical User Interface

The SMS66 Windows GUI (Figure 1) is used with the SMX3200 programming 'Dongle'. It is an easy to use Graphical Interface that is compatible with Windows 95, 98, NT, 2000 and XP operating systems. The GUI consists of pull-down menus, check boxes, up/down buttons, etc.. There are "mouse-overs" that define every function and an expert mode for directly entering data into the configuration registers. The GUI generates a checksum that can compare the programmed device configuration register values versus the hex contents.

Help Menu

The Help menu can be used to view the SMS66 Datasheet or this app note while prototyping with the Windows GUI. The 'About' selection will show the GUI version number. Please always go to the Summit web site (www.summitmicro.com) to check for the most current data sheet and GUI software. There are also options if applicable, to View GUI change notices and to check the web site directly for the most current GUI version.

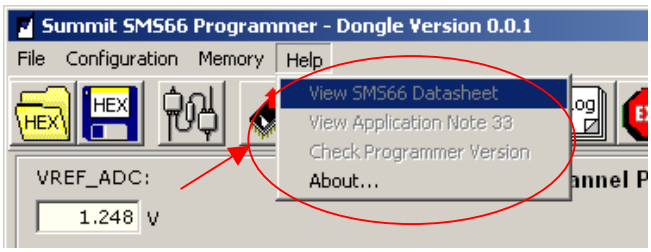

Figure 2 - Help Menu

Configuration Pull Down Menu

This menu (Figure 3A) has an option that will check for communications between the device and the PC. This selection should be tried first before changing any options. If the test passes, then all other options can be left in the default condition. If it doesn't pass, check all SMX3200 cable connections to the board and PC. If correct, then slow the I^2C clock frequency as described in the Setup Options paragraph below.

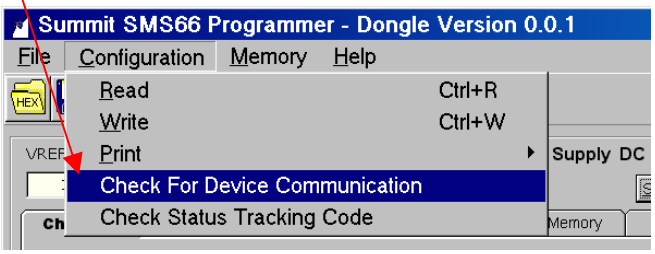

Figure 3A - Configuration Window

Setup Options

In the "File" pull-down menu (Figure 3B), there are options to set the I^2C clock frequency and delays before I^2C Read and Write operations. The default settings work with most PCs, so these settings are only for circumstances where the PC cannot communicate successfully with the SMX3200 programming 'Dongle'. The "Auto-Read Configuration/Memory After Write" check box enables a checksum test which compares the GUI hex settings or file to the programmed device at the end of a Write sequence. It does this by performing a Read immediately following a Write.

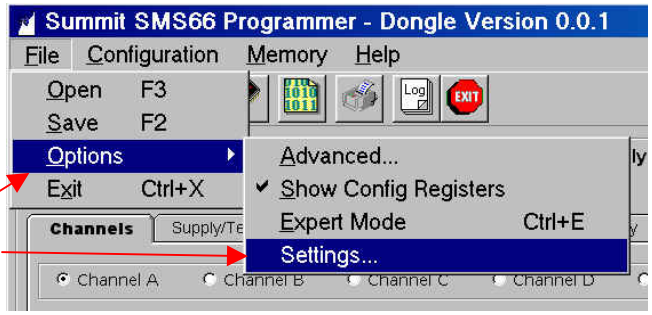

Figure 3B - Settings Window

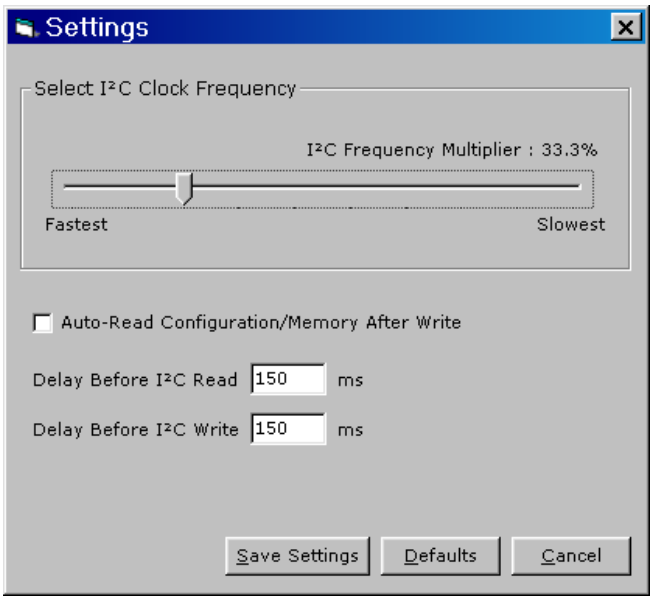

Figure 4 - Settings Options Window

Interfacing Options

The parallel Port Interfacing Window sets different options for programming the device. The 'Parallel Port Interfacing' should always be set to 'Dongle'. The 'Parallel Port Driver' can be changed for laptops if a problem is encountered in Win9X systems.

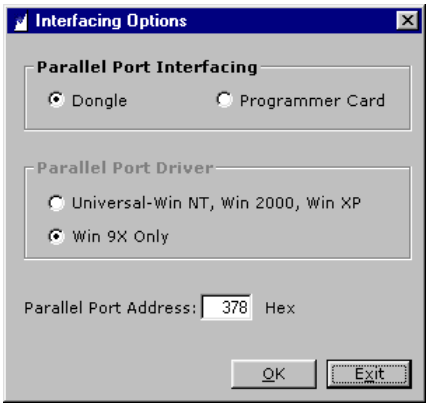

Figure 5 - Interfacing Options Window

The following registers are located at slave address 1010_{BIN}, or 1011_{BIN} bus address A2 11_{BIN} (A2 = 1_{BIN}) where A2 is either the A2 pin bias or 0 depending on the programmed selection. See register R0E, Fig 11.

Register R0C - Internal Regulator Output Voltage Select

Bit D[7] of this register selects the output voltage of the internal regulator powered by 12VIN. The remaining bits of this register are unused and must default to '0'.

Register R0C								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	12VIN regulator output set to 5.5V
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	12VIN regulator output set to 3.6V

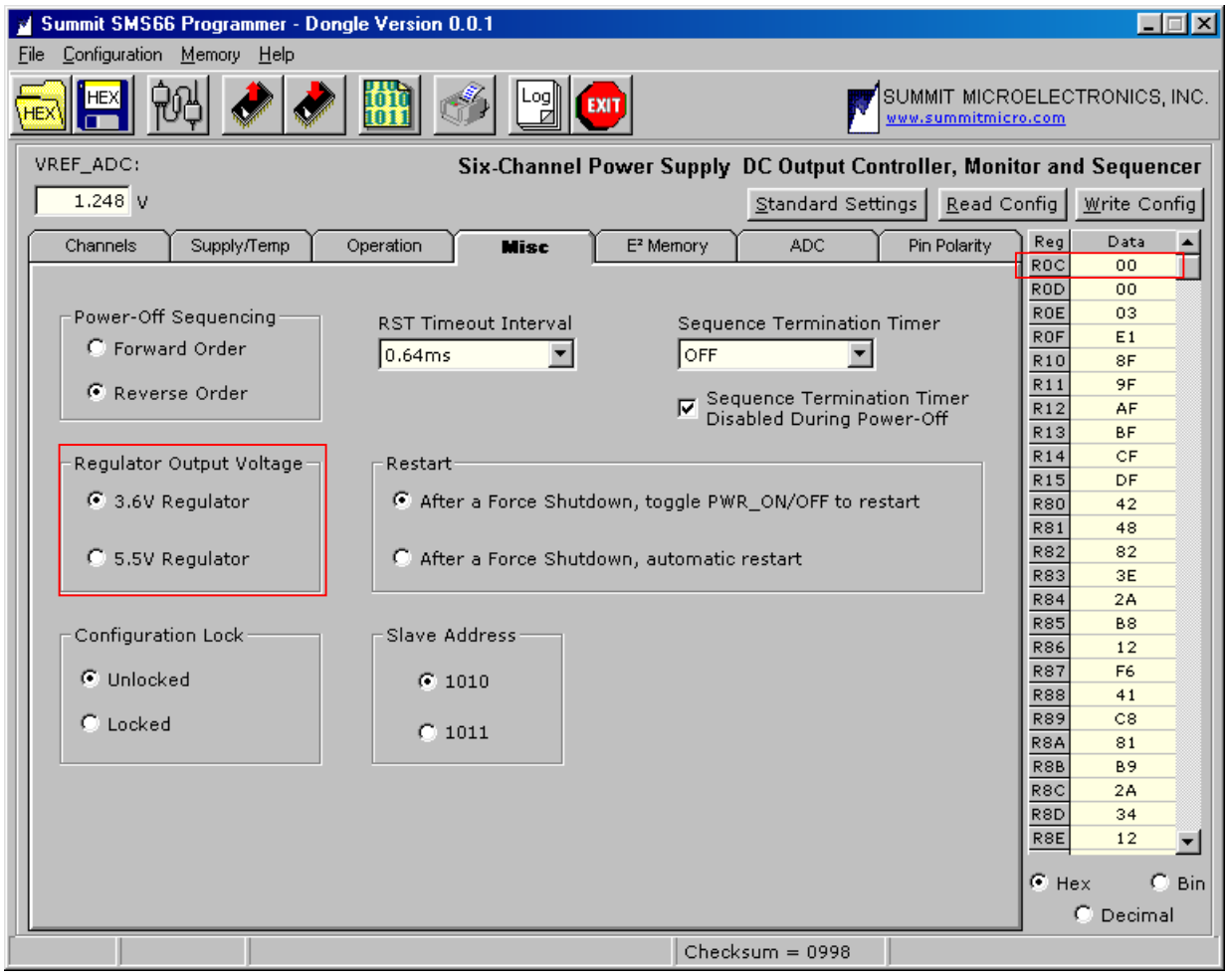

Figure 6 - Register R0C MISC Windows GUI Tab

Register R0D – Configuration Register Lock, Preconditions for Power-On

Bit D[7] of this register allows the configuration registers to be locked. Locking the configuration registers is irreversible and therefore this option cannot be selected using the GUI. Bit D[6] is used to check the Internal Temp Sensor prior to powering on. The remaining bits are unused and must default to '0'.

Register R0D								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	Configuration registers locked (writes disabled)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	Configuration registers unlocked (writes enabled)
X	**1**	**0**	**0**	**0**	**0**	**0**	**0**	Wait for Internal Temp Sensor within limits before power on allowed
X	**0**	**0**	**0**	**0**	**0**	**0**	**0**	Don't wait for Internal Temp Sensor within limits before power on allowed

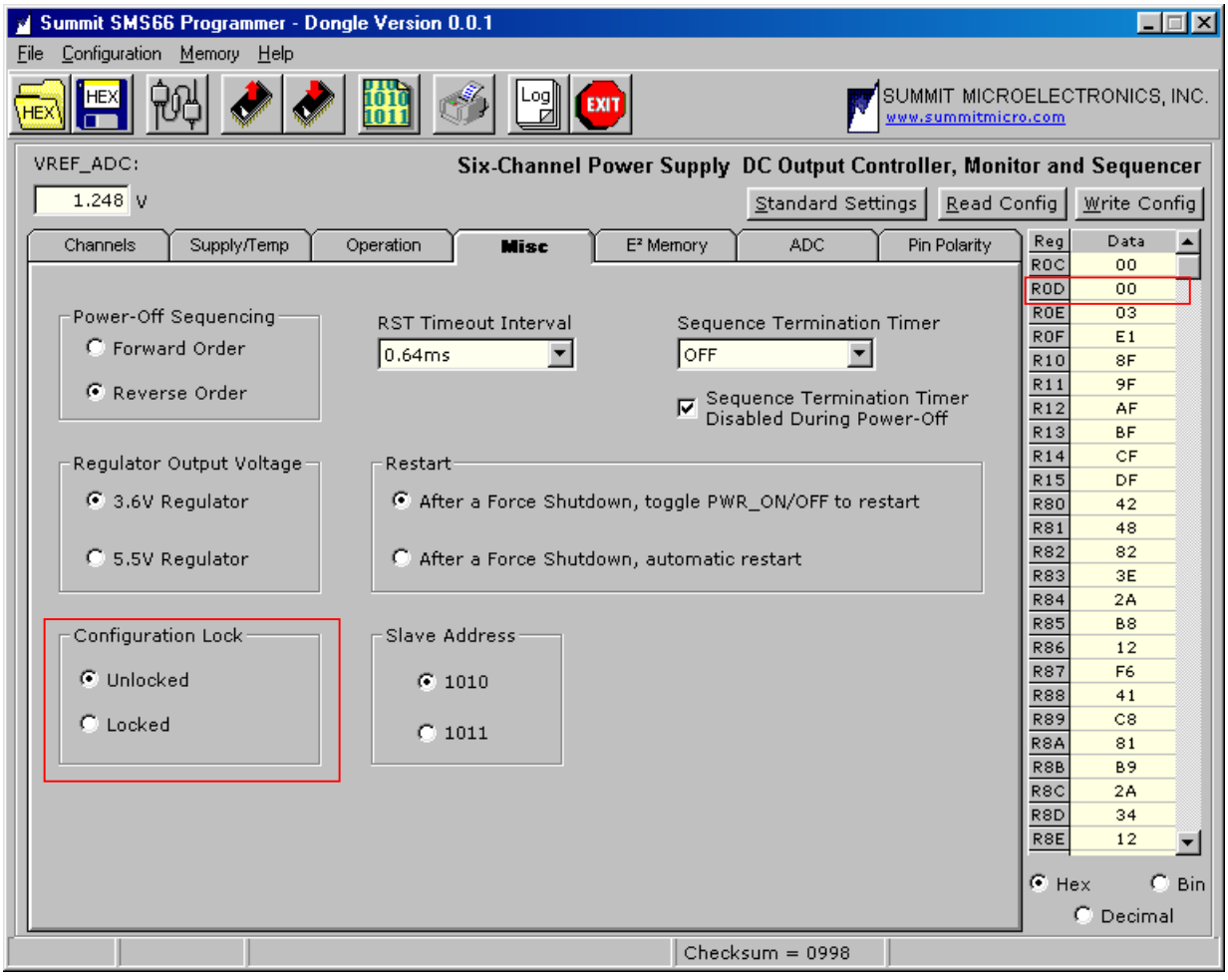

Figure 7 - Register R0D Misc Windows GUI Tab

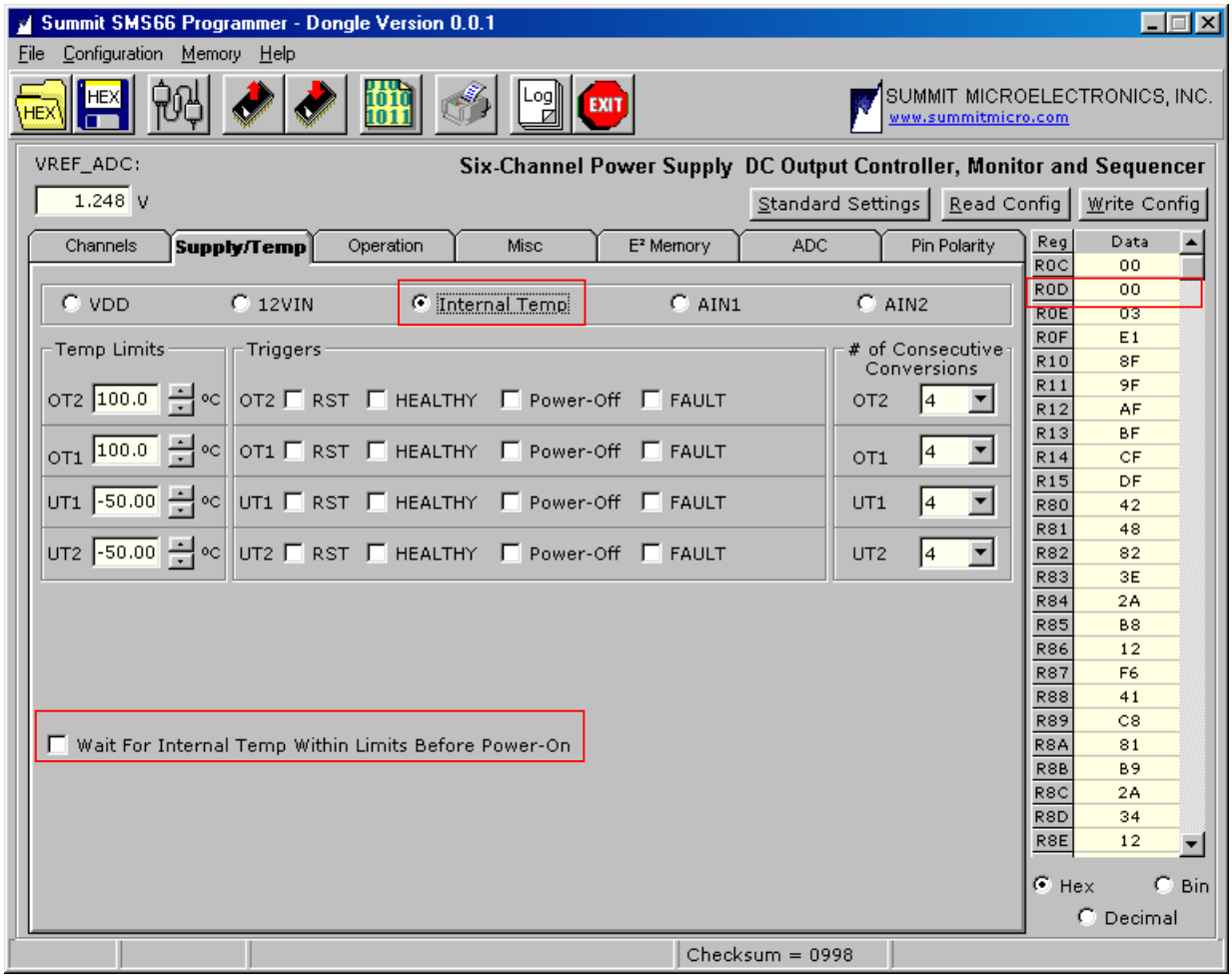

Figure 7A - Register R0D Supply/Temp Windows GUI Tab

Register R0E – Sequence Termination Timer, Reset Timeout, Slave Address, Bus Address Bits

Bits D[7:6] of this register set the Sequence Termination Timer which shuts down the PUP outputs if the timeout is exceeded. The register also sets the Reset Timeout Period with bits D[5:4]. The bus address [A2 A1 A0] of the SMS66 is set by bits D[2:0] of this register.

Register R0E								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	1	X	X	X	X	X	X	Sequence Termination Timeout = 400ms
1	0	X	X	X	X	X	X	Sequence Termination Timeout = 200ms
0	1	X	X	X	X	X	X	Sequence Termination Timeout = 100ms
0	0	X	X	X	X	X	X	Sequence Termination Timer OFF
X	X	1	1	X	X	X	X	Reset Timeout = 200ms
X	X	1	0	X	X	X	X	Reset Timeout = 100ms
X	X	0	1	X	X	X	X	Reset Timeout = 25ms
X	X	0	0	X	X	X	X	Reset Timeout = 0.64ms
X	X	X	X	1	X	X	X	Slave Address = 1011BIN
X	X	X	X	0	X	X	X	Slave Address = 1010BIN
X	X	X	X	X	1	X	X	Bus Address Bit A2 = A2 Pin
X	X	X	X	X	0	X	X	Bus Address Bit A2 = 0
X	X	X	X	X	X	1	X	Bus Address Bit A1 = 1
X	X	X	X	X	X	0	X	Bus Address Bit A1 = 0
X	X	X	X	X	X	X	1	Bus Address Bit A0 = 1
X	X	X	X	X	X	X	0	Bus Address Bit A0 = 0

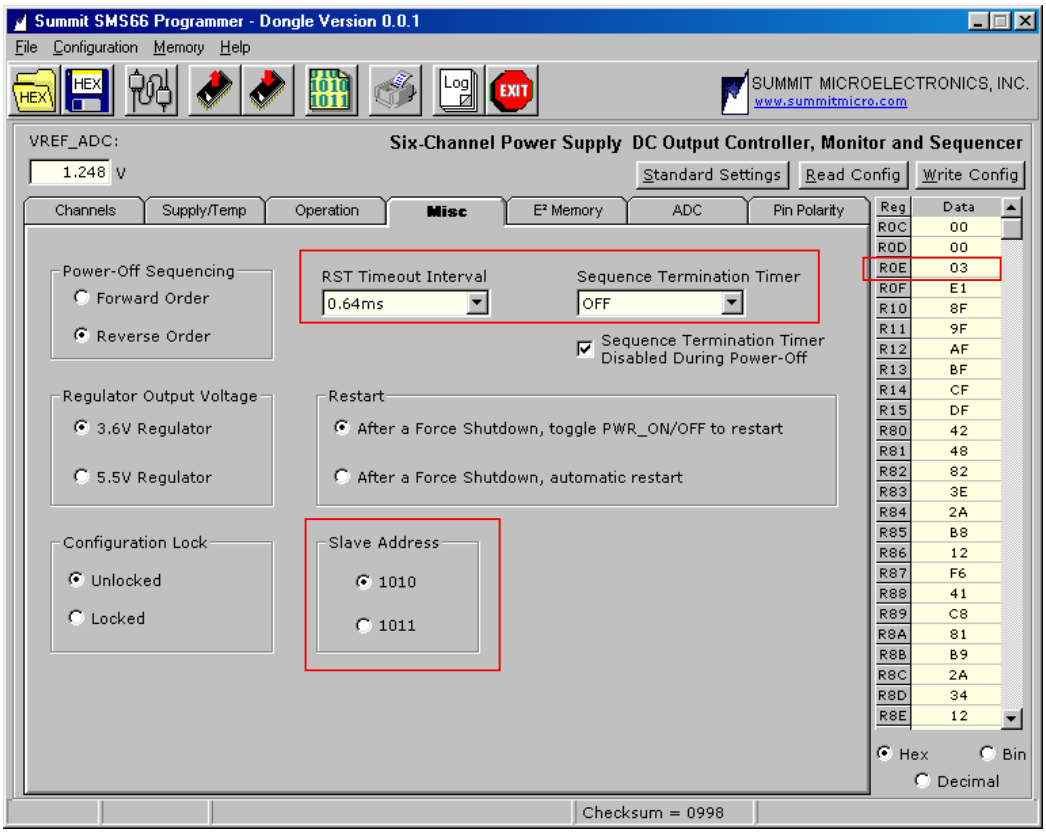

Figure 8 - Register R0E MISC Windows GUI Tab

Register R0F –Power-Off Order, Force Shutdown Restart, Power-Off Sequence Termination, Preconditions for Power-On

Bits D[7:5] of this register are unused and must default to a '1'. The Power-Off order is selected with bit D[4]. The action taken to restart the SMS66 after a Force Shutdown is selected with bit D[3]. Bit D[2] will disable the Sequence Termination Timer during a Power-Off sequence. Bits D[1:0] enable precursors to the Power-On operation.

Register R0F								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	1	1	1	X	X	X	X	Power-Off Sequence using Power-On order
1	1	1	0	X	X	X	X	Power-Off Sequence using reverse Power-On order
1	1	1	X	1	X	X	X	After a Force Shutdown, automatic restart
1	1	1	X	0	X	X	X	After a Force Shutdown, toggle PWR_ON/OFF to restart
1	1	1	X	X	1	X	X	Sequence Termination allowed during Power-Off
1	1	1	X	X	0	X	X	Sequence Termination not allowed during Power-Off
1	1	1	X	X	X	1	X	Wait for 12VIN within limits before Power-On allowed
1	1	1	X	X	X	0	X	Don't wait for 12VIN within limits before Power-On allowed
1	1	1	X	X	X	X	1	Wait for VDD within limits before Power-On allowed
1	1	1	X	X	X	X	0	Don't wait for VDD within limits before Power-On allowed

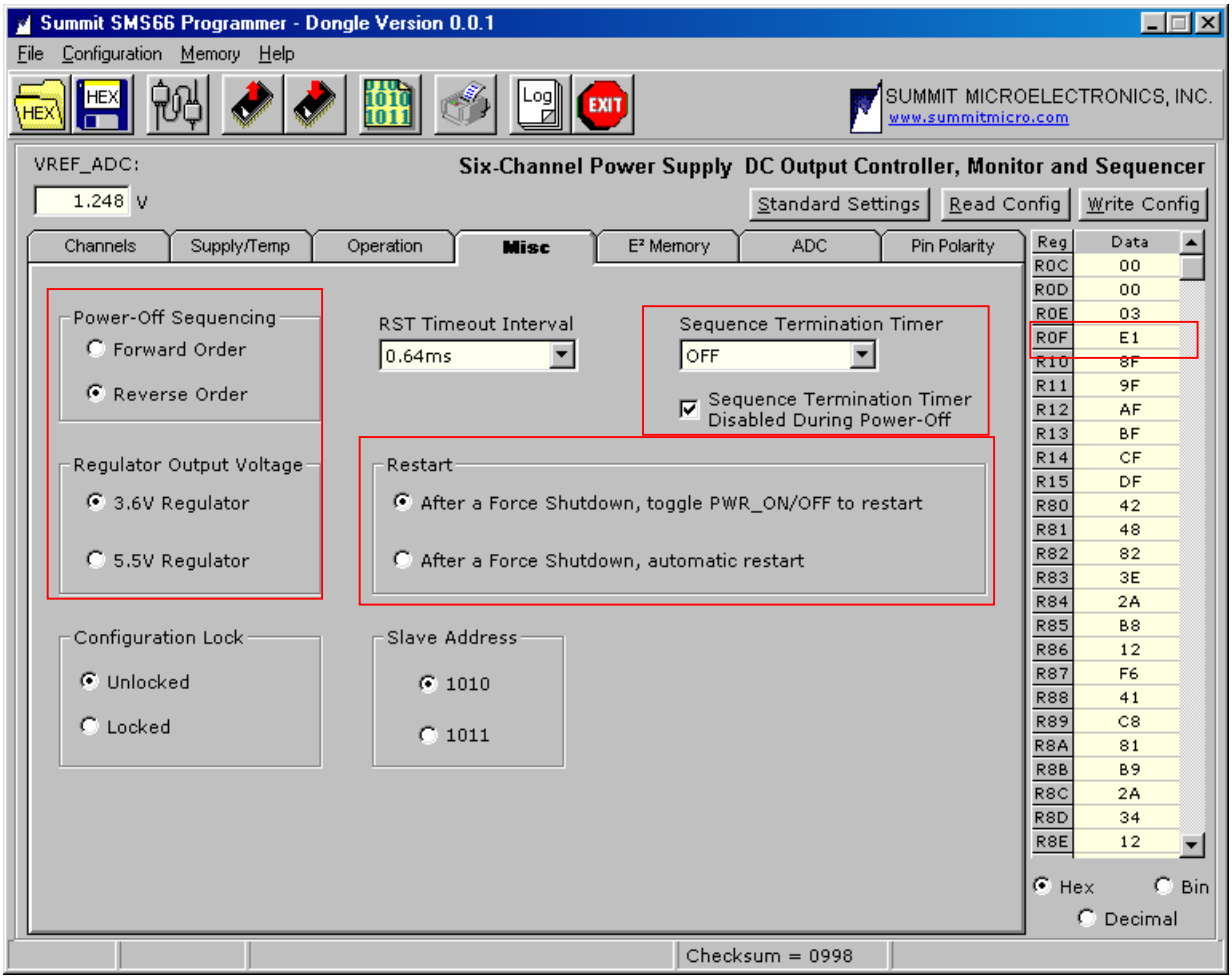

Figure 9 - Register R0F Misc Windows GUI Tab

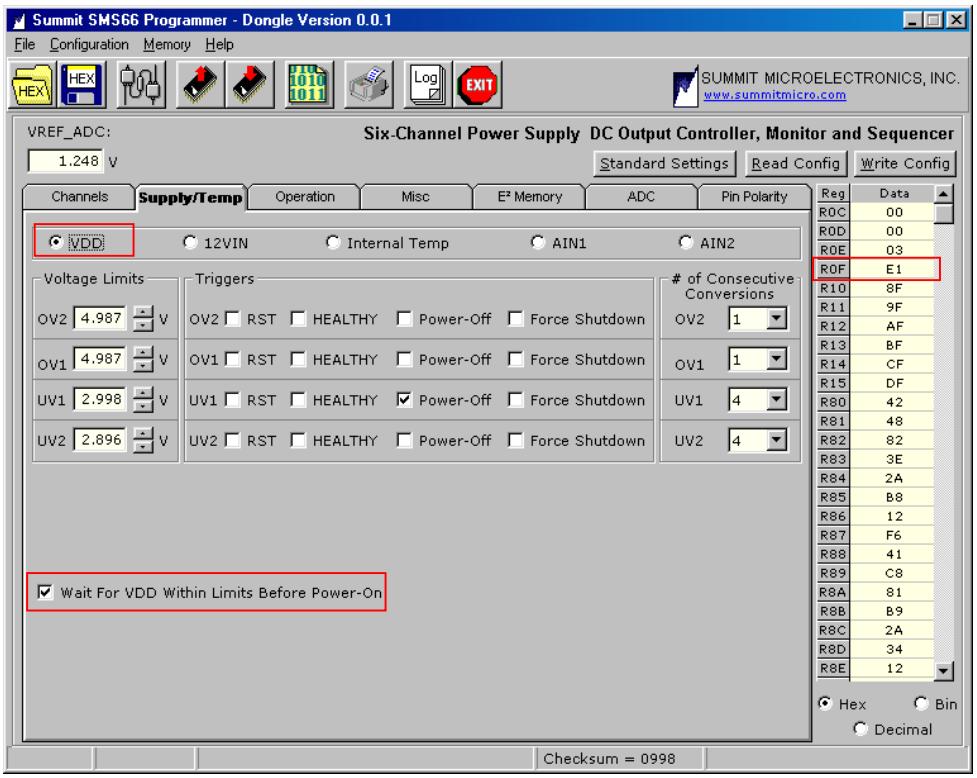

Figure 10 - Register R0F Supply Windows GUI Tab

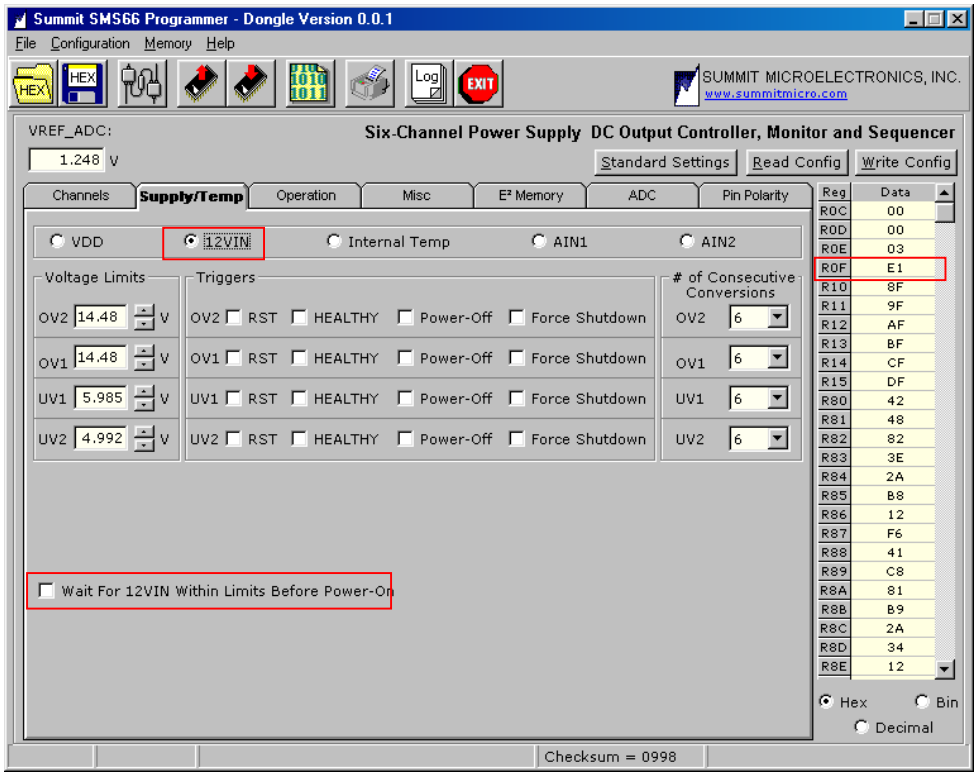

Figure 11 - Register R0F Supply Windows GUI Tab

Register R10, R11, R12, R13, R14, R15 – Sequence Position, Power-On and Power-Off Delays

Bit D[7] of these registers enable the channel to participate in sequencing. Bits D[6:4] set the Sequence Position of the channel. Note: Channels that do not participate in sequencing should have these bits set to 111_{BIN}. The Power-On delays are set by bits D[3:2] and the Power-Off delays are set by bits D[1:0].

Register R10, R11, R12, R13, R14, R15								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	X	X	X	X	X	X	X	Channel X used in Sequencing
0	X	X	X	X	X	X	X	Channel X not used in Sequencing
X	1	1	1	X	X	X	X	Channel X not used in Sequencing
X	1	0	1	X	X	X	X	Channel X Sequence Position = $5(101_{BIN})$ (Last sequence)
X	0	0	0	X	X	X	X	Channel X Sequence Position = $0(000_{BIN})$ (First sequence)
X	X	X	X	1	1	X	X	Channel X Power-On Delay = 50ms
X	X	X	X	1	0	X	X	Channel X Power-On Delay = 25ms
X	X	X	X	0	1	X	X	Channel X Power-On Delay = 12.5ms
X	X	X	X	0	0	X	X	Channel X Power-On Delay = 0.64ms
X	X	X	X	X	X	1	1	Channel X Power-Off Delay = 50ms
X	X	X	X	X	X	1	0	Channel X Power-Off Delay = 25ms
X	X	X	X	X	X	0	1	Channel X Power-Off Delay = 12.5ms
X	X	X	X	X	X	0	0	Channel X Power-Off Delay = 0.64ms

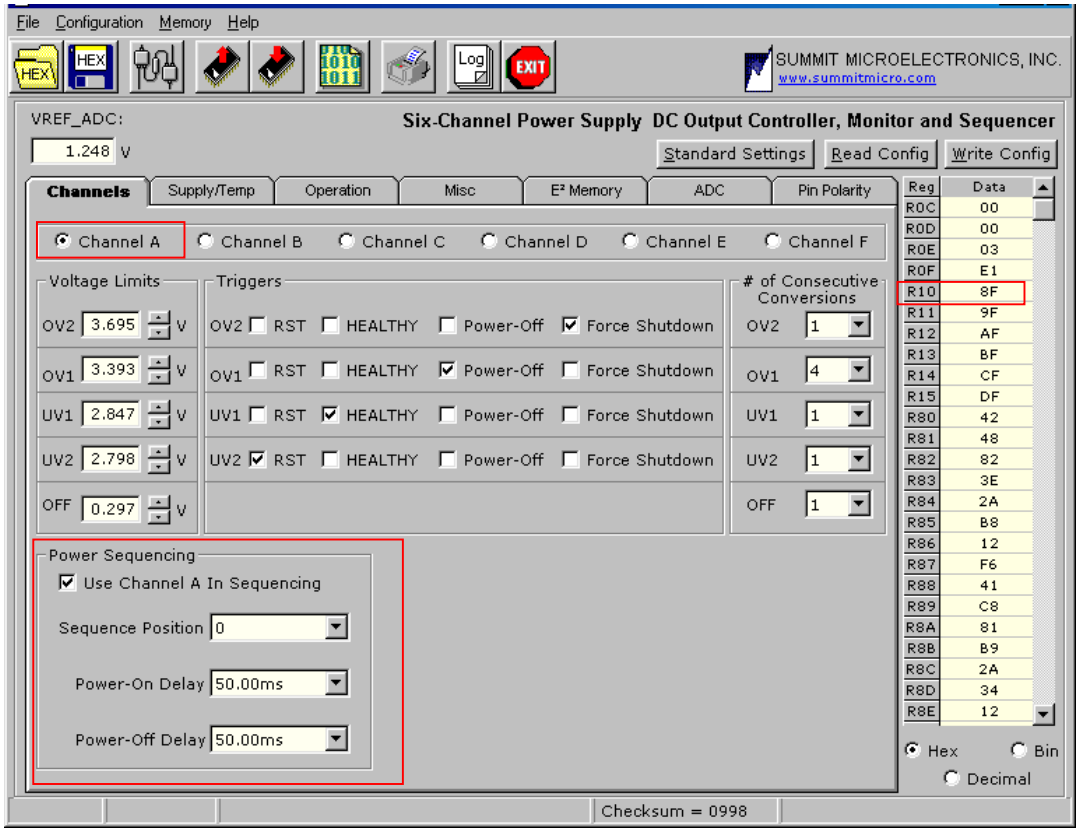

Figure 12 - Register R10 Channels Windows GUI Tab

Register R80, R82, R84, R86, R88, R8A, R8C, R8E, R90, R92, R94, R96, R98, R9A, R9C, R9E, RA0, RA2, RA4, RA6, RA8, RAA, RAC, RAE, RB0, RB2, RB4, RB6, RB8, RBA, RBC, RBE – Triggers, Filter, and Voltage Limits for Channels A, B, C, D, E and F, VDD and 12VIN

These registers are combined with the following set of registers to set the over-voltage (OV1 and OV2) and under-voltage (UV1 and UV2) limits. Each limit also has associated triggers and filters.

Register R80, R82, R84, R86, R88, R8A, R8C, R8E, R90, R92, R94, R96, R98, R9A, R9C, R9E, RA0, RA2, RA4, RA6, RA8, RAA, RAC, RAE, RB0, RB2, RB4, RB6, RB8, RBA, RBC, RBE								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	X	X	X	X	X	X	X	Triggers RST
0	X	X	X	X	X	X	X	Does not trigger RST
X	1	X	X	X	X	X	X	Triggers HEALTHY
X	0	X	X	X	X	X	X	Does not trigger HEALTHY
X	X	1	X	X	X	X	X	Triggers Power-Off
X	X	0	X	X	X	X	X	Does not trigger Power-Off
X	X	X	1	X	X	X	X	Triggers Force Shutdown
X	X	X	0	X	X	X	X	Does not trigger Force Shutdown
X	X	X	X	1	1	X	X	Fault on 6 Consecutive Conversions
X	X	X	X	1	0	X	X	Fault on 4 Consecutive Conversions
X	X	X	X	0	1	X	X	Fault on 2 Consecutive Conversions
X	X	X	X	0	0	X	X	Fault on 1 Conversion
X	X	X	X	X	X	C9	C8	Bits [9:8] of 10-bit Limit Setting

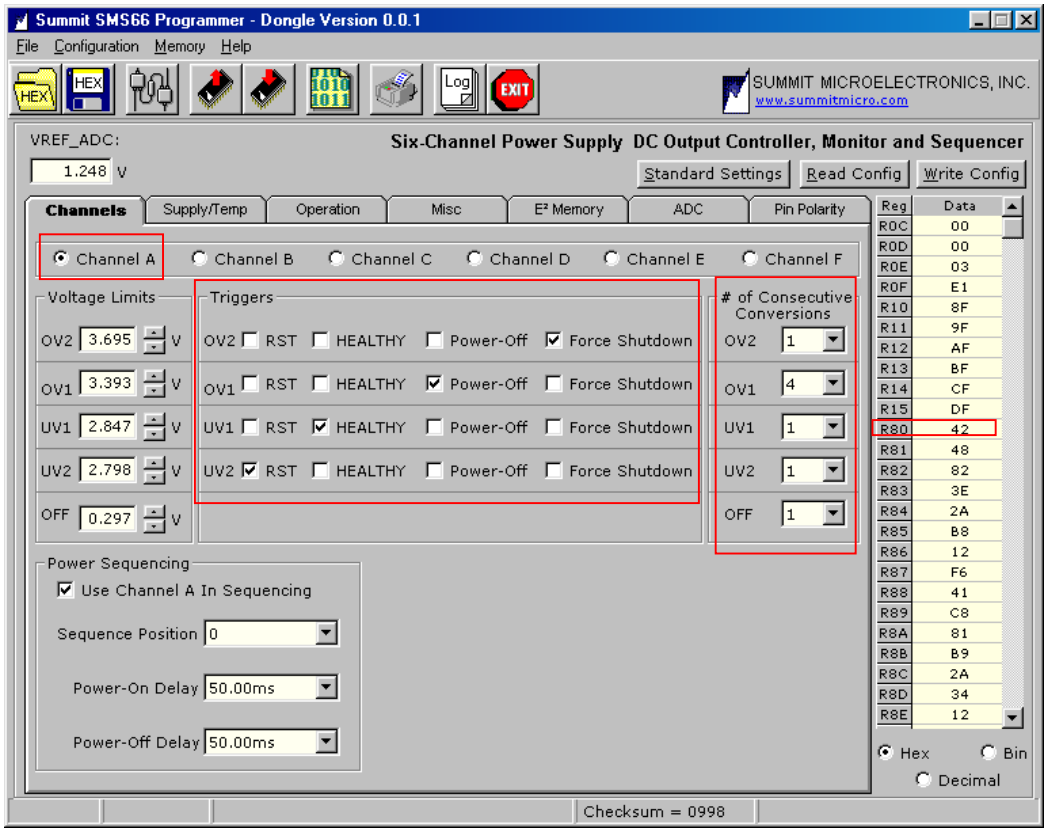

Figure 13 - Register R80 Channels Windows GUI Tab

Register R81, R83, R85, R87, R89, R8B, R8D, R8F, R91, R93, R95, R97, R99, R9B, R9D, R9F, RA1, RA3, RA5, RA7, RA9, RAB, RAD, RAF, RB1, RB3, RB5, RB7, RB9, RBB, RBD, RBF - Voltage Limits for Channels A, B, C, D, E and F, VDD and 12VIN

These registers are combined with the previous set of registers to set the over-voltage (OV1 and OV2) and under-voltage (UV1 and UV2) limits.

Register R81, R83, R85, R87, R89, R8B, R8D, R8F, R91, R93, R95, R97, R99, R9B, R9D, R9F, RA1, RA3, RA5, RA7, RA9, RAB, RAD, RAF, RB1, RB3, RB5, RB7, RB9, RBB, RBD, RBF								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	C6	C5	C4	C3	C2	C1	C0	Bits [7:0] of 10-bit Limit Setting

The Limit Setting bits (C[9:0]) are set using the following table:

If Channel =:	Then = C[9:0]:
A, B, C, D, E, F or VDD	1024 * Limit(V)/(4 * VREF_ADC)
12VIN	1024 * Limit(V)/(12 * VREF_ADC)

The following table lists the registers with their corresponding Channel and Limit:

Registers	Ch. - Limit	Registers	Ch. – Limit	Registers	Ch. – Limit	Registers	Ch. - Limit
R80:R81	Ch A – UV1	R90:R91	Ch C – UV1	RA0:RA1	Ch E – UV1	RB0:RB1	VDD – UV1
R82:R83	Ch A – UV2	R92:R93	Ch C – UV2	RA2:RA3	Ch E – UV2	RB2:RB3	VDD – UV2
R84:R85	Ch A – OV1	R94:R95	Ch C – OV1	RA4:RA5	Ch E – OV1	RB4:RB5	VDD – OV1
R86:R87	Ch A – OV2	R96:R97	Ch C – OV2	RA6:RA7	Ch E – OV2	RB6:RB7	VDD – OV2
R88:R89	Ch B – UV1	R98:R99	Ch D – UV1	RA8:RA9	Ch F – UV1	RB8:RB9	12VIN – UV1
R8A:R8B	Ch B – UV2	R9A:R9B	Ch D – UV2	RAA:RAB	Ch F – UV2	RBA:RBB	12VIN – UV2
R8C:R8D	Ch B – OV1	R9C:R9D	Ch D – OV1	RAC:RAD	Ch F – OV1	RBC:RBD	12VIN – OV1
R8E:R8F	Ch B – OV2	R9E:R9F	Ch D – OV2	RAE:RAF	Ch F – OV2	RBE:RBF	12VIN– OV2

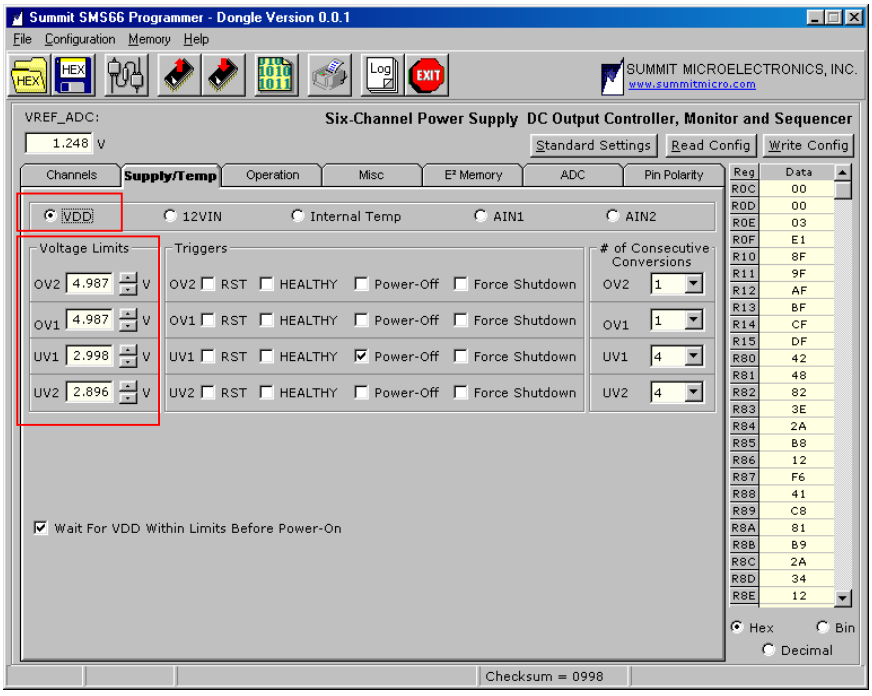

Figure 14 - R81 Windows Supply/Temp GUI Tab

Register RC0, RC2, RC4, RC6, RC8, RCA, RCC, RCE, RD0, RD2, RD4, RD6 – Triggers, Filter, and Limits for AIN1, AIN2 and the Internal Temperature Sensor

These registers are combined with the following set of registers to set the over-voltage (OV1 and OV2) and under-voltage (UV1 and UV2) limits and the over-temperature (OT1 and OT2) and under-temperature (UT1 and UT2) limits. Each limit also has associated triggers and filters.

Register RC0, RC2, RC4, RC6, RC8, RCA, RCC, RCE, RD0, RD2, RD4, RD6								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	**X**	**X**	**X**	**X**	**X**	**X**	**X**	Triggers RST
0	**X**	**X**	**X**	**X**	**X**	**X**	**X**	Does not trigger RST
X	**1**	**X**	**X**	**X**	**X**	**X**	**X**	Triggers HEALTHY
X	**0**	**X**	**X**	**X**	**X**	**X**	**X**	Does not trigger HEALTHY
X	**X**	**1**	**X**	**X**	**X**	**X**	**X**	Triggers Power-Off
X	**X**	**0**	**X**	**X**	**X**	**X**	**X**	Does not trigger Power-Off
X	**X**	**X**	**1**	**X**	**X**	**X**	**X**	Triggers FAULT
X	**X**	**X**	**0**	**X**	**X**	**X**	**X**	Does not trigger FAULT
X	**X**	**X**	**X**	**1**	**1**	**X**	**X**	Fault on 6 Consecutive Conversions
X	**X**	**X**	**X**	**1**	**0**	**X**	**X**	Fault on 4 Consecutive Conversions
X	**X**	**X**	**X**	**0**	**1**	**X**	**X**	Fault on 2 Consecutive Conversions
X	**X**	**X**	**X**	**0**	**0**	**X**	**X**	Fault on 1 Conversion
X	**X**	**X**	**X**	**X**	**X**	**C9**	**C8**	Bits [9:8] of 10-bit Limit Setting

Register RC1, RC3, RC5, RC7, RC9, RCB, RCD, RCF, RD1, RD3, RD5, RD7 - Limits for AIN1, AIN2 and the Internal Temperature Sensor

These registers are combined with the previous set of registers to set the over-voltage (OV1 and OV2) and under-voltage (UV1 and UV2) limits and the over-temperature (OT1 and OT2) and under-temperature (UT1 and UT2) limits.

Register RC1, RC3, RC5, RC7, RC9, RCB, RCD, RCF, RD1, RD3, RD5, RD7								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Bits [7:0] of 10-bit Limit Setting

The Limit Setting bits (C[9:0]) are set using the following table:

If Channel =:	**Then = C[9:0]:**
AIN1 or AIN2	1024 * Limit(V)/(2 * VREF_ADC)
Internal Temperature Sensor	4 * Limit(C) + 512

The following table lists the registers with their corresponding Channel and Limit:

Registers	**Ch. - Limit**	**Registers**	**Ch. – Limit**
RC0:RC1	Int. Temp. Sense – UT1	RD0:RD1	AIN2 – UV1
RC2:RC3	Int. Temp. Sense – UT2	RD2:RD3	AIN2 – UV2
RC4:RC5	Int. Temp. Sense – OT1	RD4:RD5	AIN2 – OV1
RC6:RC7	Int. Temp. Sense – OT2	RD6:RD7	AIN2 – OV2
RC8:RC9	AIN1 – UV1		
RCA:RCB	AIN1 – UV2		
RCC:RCD	AIN1 – OV1		
RCE:RCF	AIN1 – OV2		

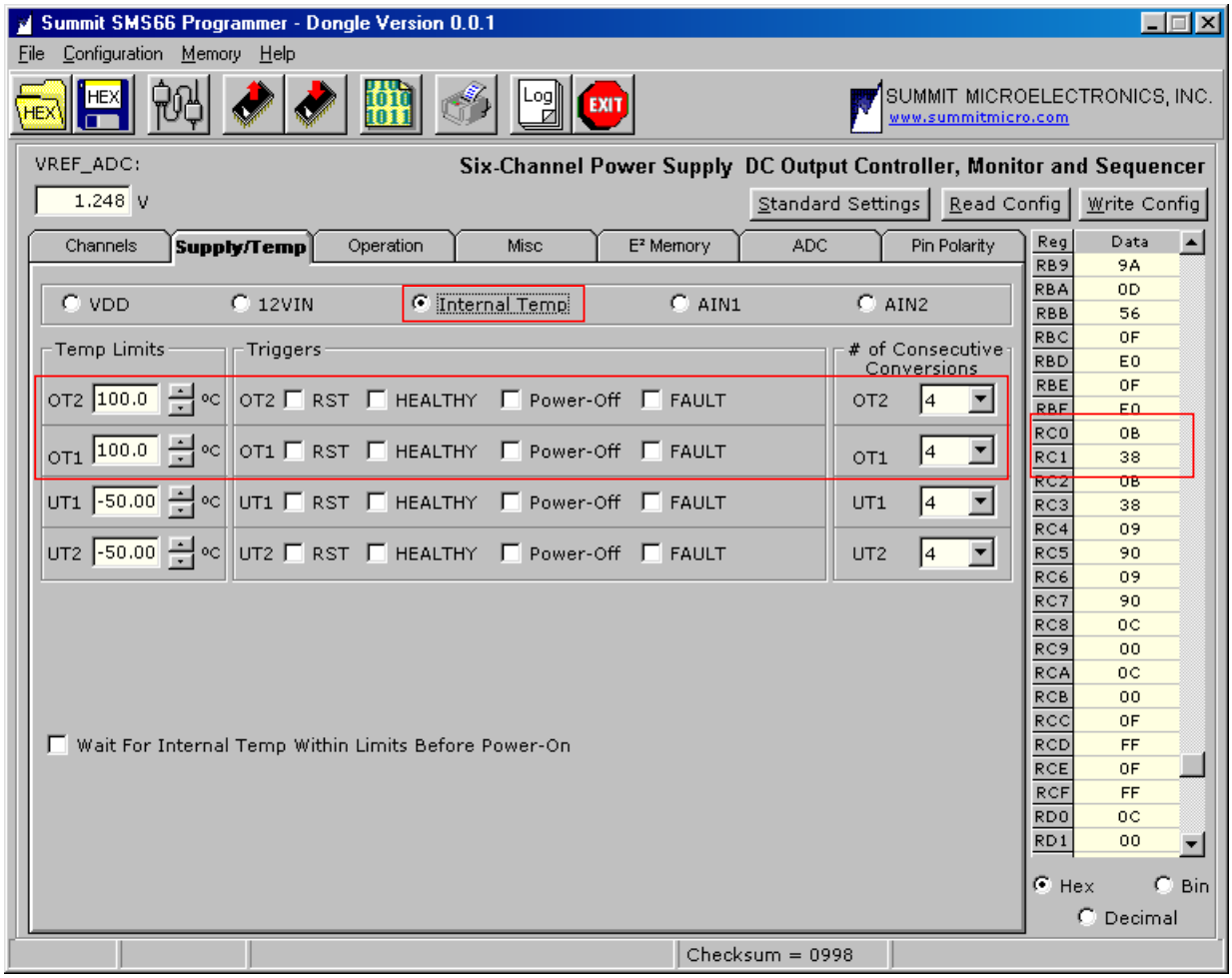

Figure 15 - Register RC0, RC1 Windows Supply/Temp GUI Tab

Register RE0, RE2, RE4, RE6, RE8, REA - Filter and Off Limit for Channels A, B, C, D, E and F

These registers are combined with the following set of registers to set the OFF limit used for Power-Off sequencing and Force Shutdown operations.

Register RE0, RE2, RE4, RE6, RE8, REA								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**0**	**0**	**X**	**X**	**X**	**X**	These bits must be set to 0
X	**X**	**X**	**X**	**1**	**1**	**X**	**X**	OFF on 6 Consecutive Conversions
X	**X**	**X**	**X**	**1**	**0**	**X**	**X**	OFF on 4 Consecutive Conversions
X	**X**	**X**	**X**	**0**	**1**	**X**	**X**	OFF on 2 Consecutive Conversions
X	**X**	**X**	**X**	**0**	**0**	**X**	**X**	OFF on 1 Conversion
X	**X**	**X**	**X**	**X**	**X**	**C9**	**C8**	Bits [9:8] of 10-bit Limit Setting

Register RE1, RE3, RE5, RE7, RE9, REB - Off Limit for Channels A, B, C, D, E and F

These registers are combined with the previous set of registers to set the OFF limit used for Power-Off sequencing and Force Shutdown operations.

Register RE1, RE3, RE5, RE7, RE9, REB								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	Bits [7:0] of 10-bit Limit Setting

The Limit Setting bits (C[9:0]) are set using the following table:

If Channel =:	**Then = C[9:0]:**
A, B, C, D, E or F	1024 * Limit(V)/(4 * VREF_ADC)

The following table lists the registers with their corresponding Channel and Limit:

Registers	**Ch. – Limit**
RE0:RE1	Ch A – OFF
RE2:RE3	Ch B – OFF
RE4:RE5	Ch C – OFF
RE6:RE7	Ch D – OFF
RE8:RE9	Ch E – OFF
REA:REB	Ch F – OFF

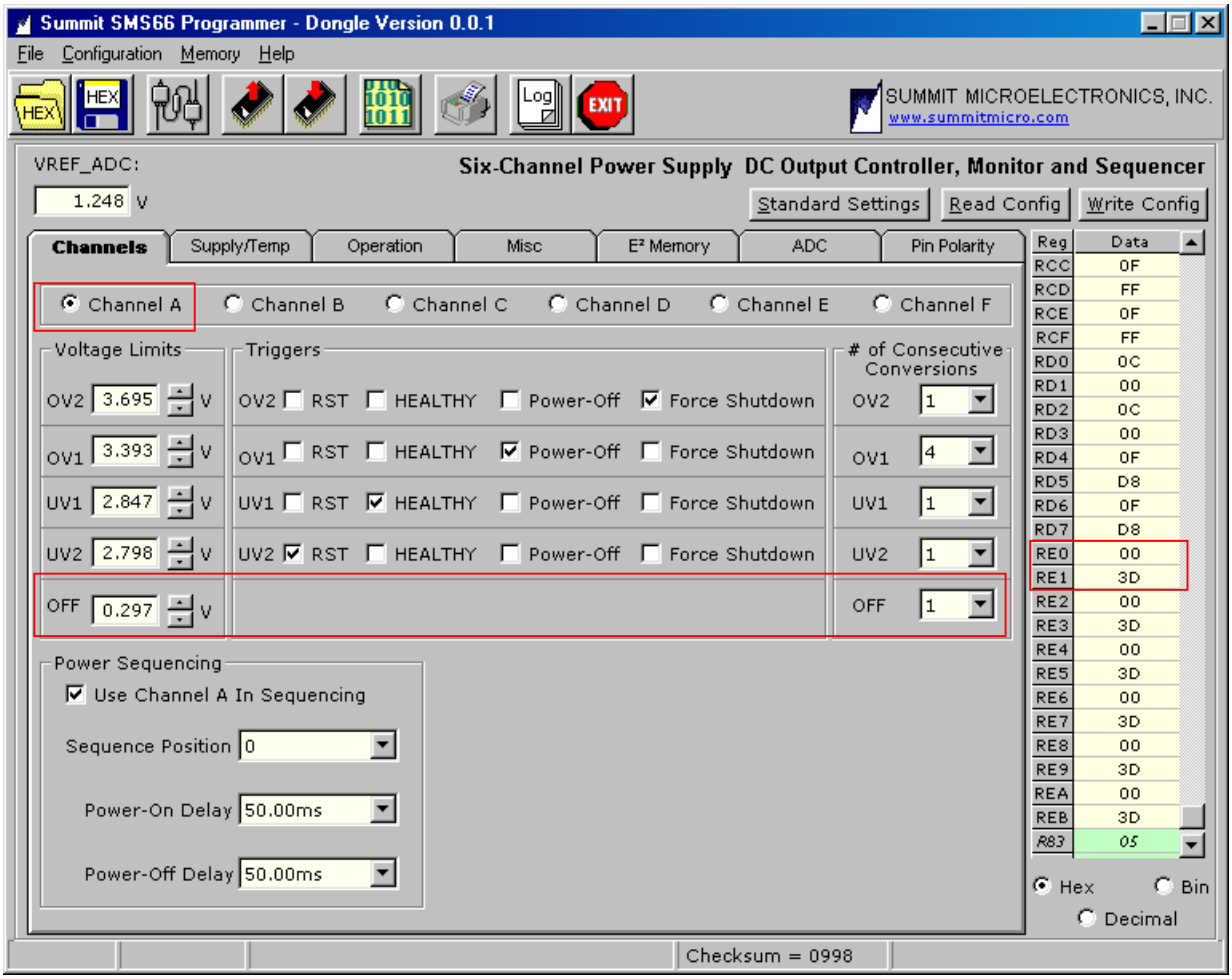

Figure 16 - Register RE0, RE1 Windows Channel GUI Tab

The following registers are located at slave address 1001_{BIN}, bus address A2 A1 A0 where A2 is either the A2 pin bias or 0 depending on the programmed selection and A1 A0 are depend on the programmed combination. See register R0E in the above section.

Register R80 – Command and Status Register (Volatile)

This volatile register allows I2C control of the Power-On, Power-Off and Force Shutdown commands. It also contains to status bits which are set when all the sequenced channels are on and when all the sequenced channels are off.

Register R80								
D7	D6	D5	D4	D3	D2	D1	D0	Action
1	0	0	X	X	X	X	X	Power-On Command
0	1	0	X	X	X	X	X	Power-Off Command
0	0	1	X	X	X	X	X	Force Shutdown Command
X	X	X	X	1	X	X	X	All Sequenced Channels ON (Read-Only)
X	X	X	X	0	X	X	X	All Sequenced Channels not ON (Read-Only)
X	X	X	X	X	1	X	X	All Sequenced Channels OFF (Read-Only)
X	X	X	X	X	0	X	X	All Sequenced Channels not OFF (Read-Only)

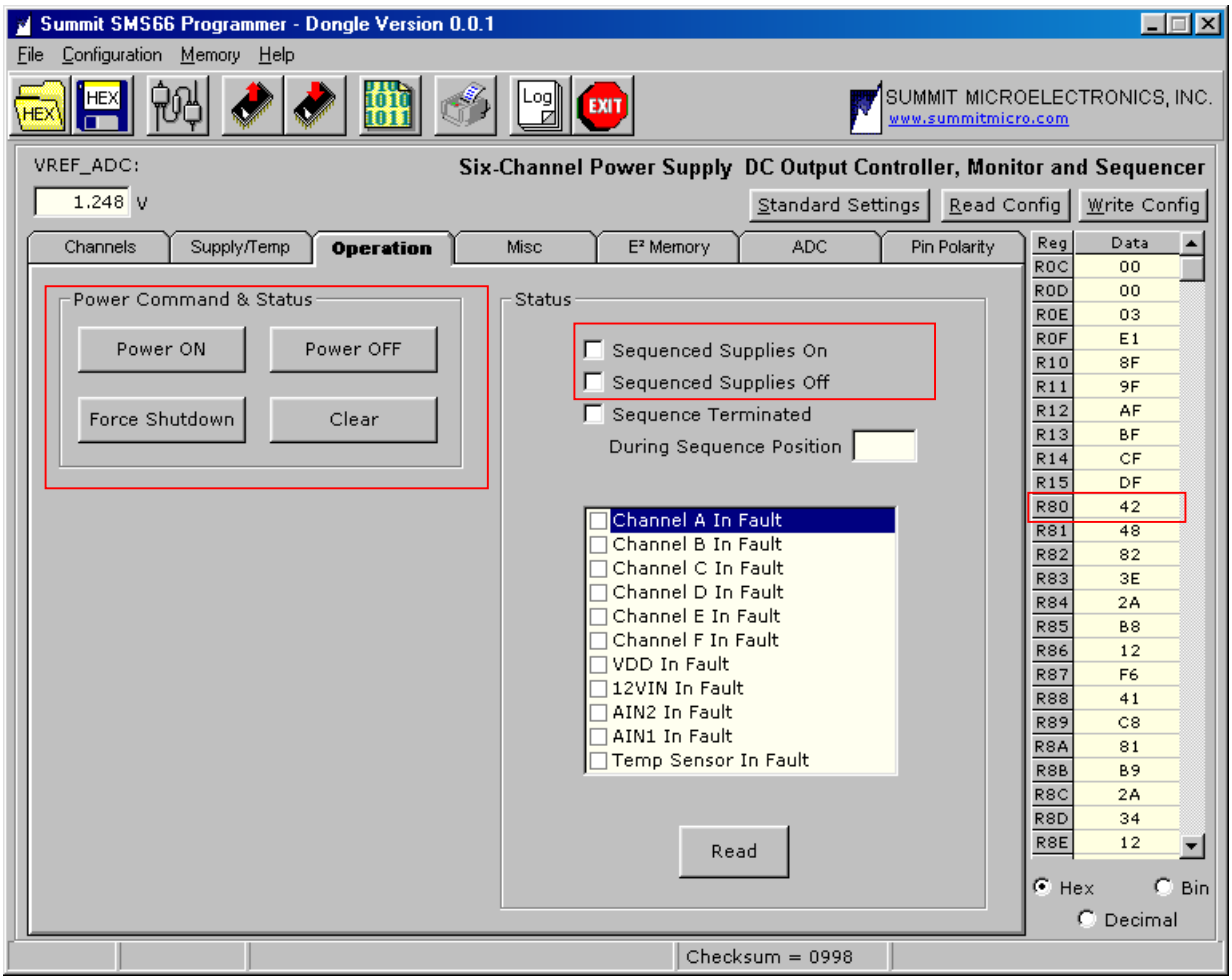

Figure 17 - Register R80 Windows Operations GUI Tab

Register R81 – Status Register (Volatile, Read-Only)

This volatile, read-only register shows the status of AIN1, AIN2 and the Internal Temperature. Bits D[7:4] of the register store information regarding a Sequence Termination.

Register R81								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	**X**	**X**	**X**	**X**	**X**	**X**	**X**	Last Sequence Terminated
0	**X**	**X**	**X**	**X**	**X**	**X**	**X**	Last Sequence not Terminated
1	**1**	**0**	**1**	**X**	**X**	**X**	**X**	Last Sequence Terminated in Position 5
1	**0**	**0**	**0**	**X**	**X**	**X**	**X**	Last Sequence Terminated in Position 0
X	**X**	**X**	**X**	**X**	**1**	**X**	**X**	Fault on AIN2
X	**X**	**X**	**X**	**X**	**0**	**X**	**X**	No Fault on AIN2
X	**X**	**X**	**X**	**X**	**X**	**1**	**X**	Fault on AIN1
X	**X**	**X**	**X**	**X**	**X**	**0**	**X**	No Fault on AIN1
X	**X**	**X**	**X**	**X**	**X**	**X**	**1**	Fault on Internal Temperature Sensor
X	**X**	**X**	**X**	**X**	**X**	**X**	**0**	No Fault on Internal Temperature Sensor

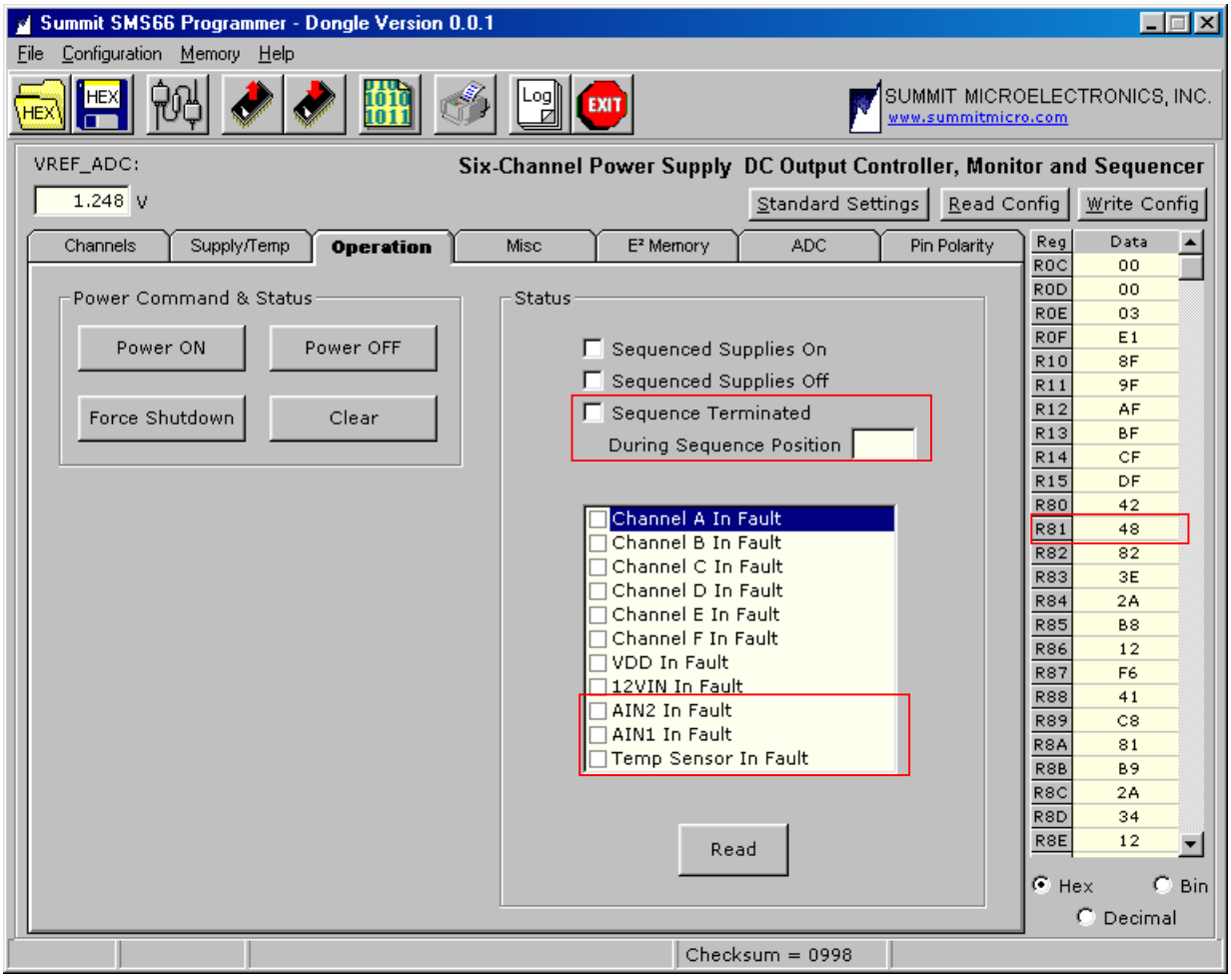

Figure 18 - Register R81 Windows Operation GUI Tab

Register R82 – Status Register (Volatile, Read-Only)

This volatile, read-only register shows the status of Channels A, B, C, D, E and F and the VDD and 12VIN inputs.

Register R82								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
1	X	X	X	X	X	X	X	Fault on Channel 12VIN
0	X	X	X	X	X	X	X	No Fault on Channel 12VIN
X	1	X	X	X	X	X	X	Fault on Channel VDD
X	0	X	X	X	X	X	X	No Fault on VDD
X	X	1	X	X	X	X	X	Fault on Channel F
X	X	0	X	X	X	X	X	No Fault on Channel F
X	X	X	1	X	X	X	X	Fault on Channel E
X	X	X	0	X	X	X	X	No Fault on Channel E
X	X	X	X	1	X	X	X	Fault on Channel D
X	X	X	X	0	X	X	X	No Fault on Channel D
X	X	X	X	X	1	X	X	Fault on Channel C
X	X	X	X	X	0	X	X	No Fault on Channel C
X	X	X	X	X	X	1	X	Fault on Channel B
X	X	X	X	X	X	0	X	No Fault on Channel B
X	X	X	X	X	X	X	1	Fault on Channel A
X	X	X	X	X	X	X	0	No Fault on Channel A

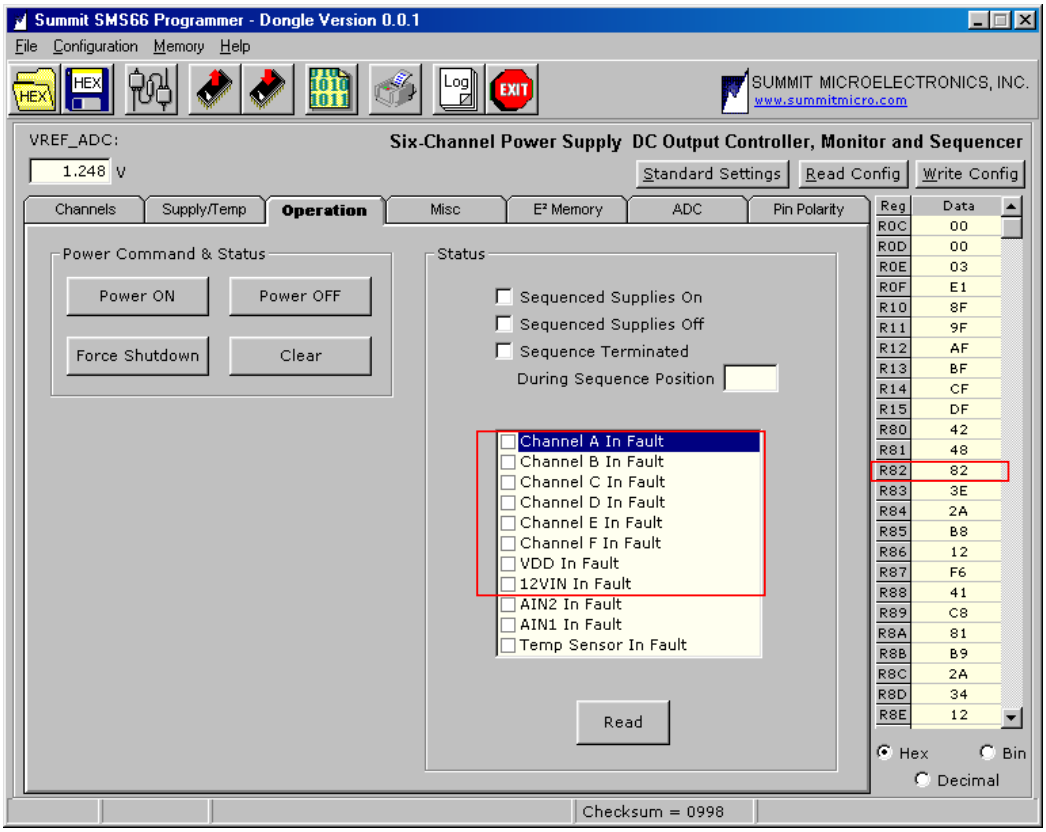

Figure 19 - Register R82 Windows Operation GUI Tab

Register R83 – Input and Output Pin Polarities

This register sets the polarity of the HEALTHY, FAULT and RST outputs and the MR, PWR_ON/OFF and FS inputs.

Register R83								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	0	X	X	X	X	X	X	Set these bits to 0's
0	0	1	X	X	X	X	X	HEALTHY Active High
0	0	0	X	X	X	X	X	HEALTHY Active Low
0	0	X	1	X	X	X	X	FAULT Active High
0	0	X	0	X	0	X	X	FAULT Active Low
0	0	X	X	1	X	X	X	RST Active High
0	0	X	X	0	X	X	X	RST Active Low
0	0	X	X	X	1	X	X	MR Active High
0	0	X	X	X	0	X	X	MR Active Low
0	0	X	X	X	X	1	X	PWR_ON/OFF Active High
0	0	X	X	X	X	0	X	PWR_ON/OFF Active Low
0	0	X	X	X	X	X	1	FS Active High
0	0	X	X	X	X	X	0	FS Active Low

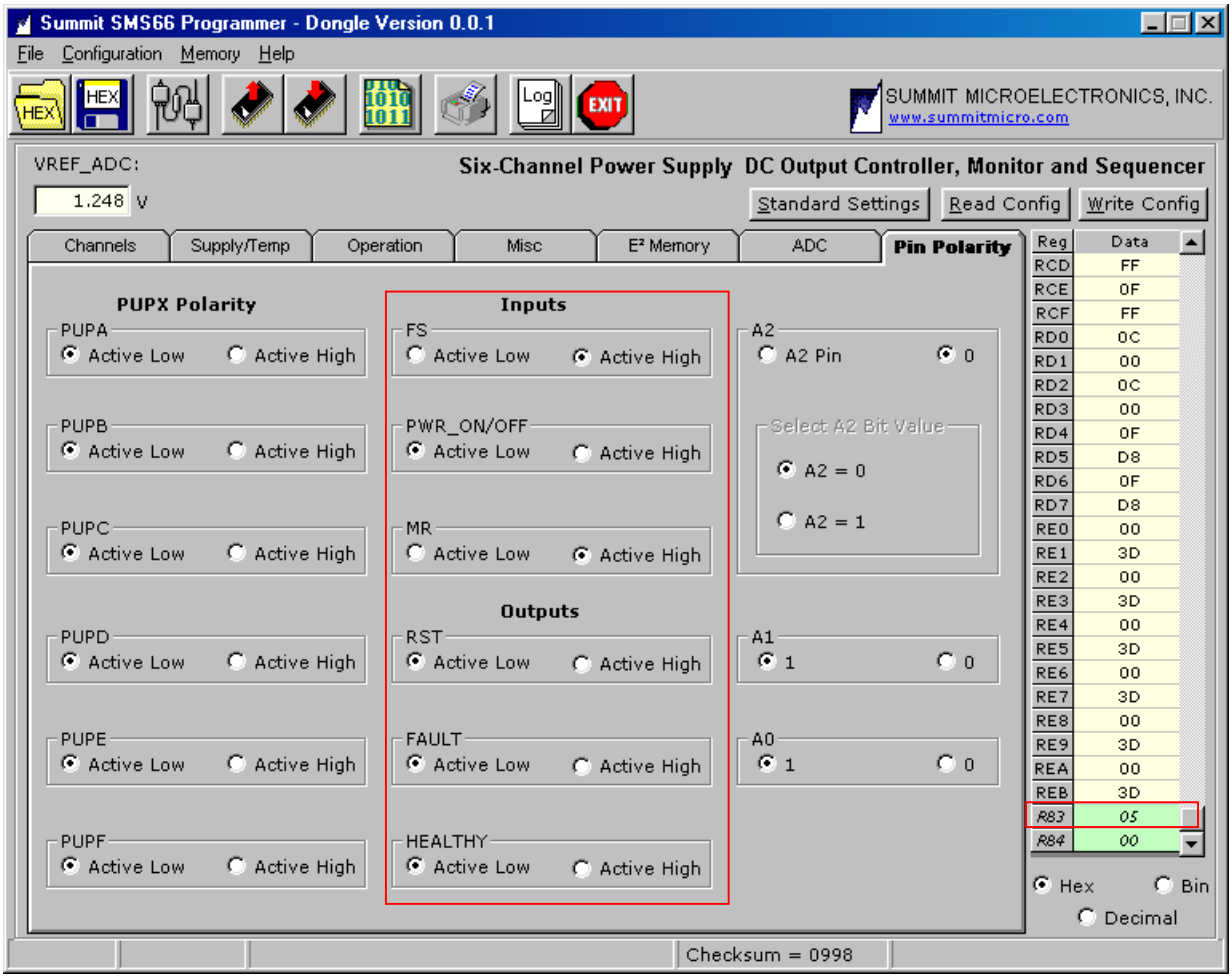

Figure 20 - Register R83 Windows Pin Polarity GUI Tab

Register R84 - PUPX Pin Polarities

This register sets the polarity of the PUP outputs.

Register R84								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**0**	**X**	**X**	**X**	**X**	**X**	**X**	Set these bits to 0's
X	**X**	**1**	**X**	**X**	**X**	**X**	**X**	PUPF Active High
X	**X**	**0**	**X**	**X**	**X**	**X**	**X**	PUPF Active Low
X	**X**	**X**	**1**	**X**	**X**	**X**	**X**	PUPE Active High
X	**X**	**X**	**0**	**X**	**0**	**X**	**X**	PUPE Active Low
X	**X**	**X**	**X**	**1**	**X**	**X**	**X**	PUPD Active High
X	**X**	**X**	**X**	**0**	**X**	**X**	**X**	PUPD Active Low
X	**X**	**X**	**X**	**X**	**1**	**X**	**X**	PUPC Active High
X	**X**	**X**	**X**	**X**	**0**	**X**	**X**	PUPC Active Low
X	**X**	**X**	**X**	**X**	**X**	**1**	**X**	PUPB Active High
X	**X**	**X**	**X**	**X**	**X**	**0**	**X**	PUPB Active Low
X	**X**	**X**	**X**	**X**	**X**	**X**	**1**	PUPA Active High
X	**X**	**X**	**X**	**X**	**X**	**X**	**0**	PUPA Active Low

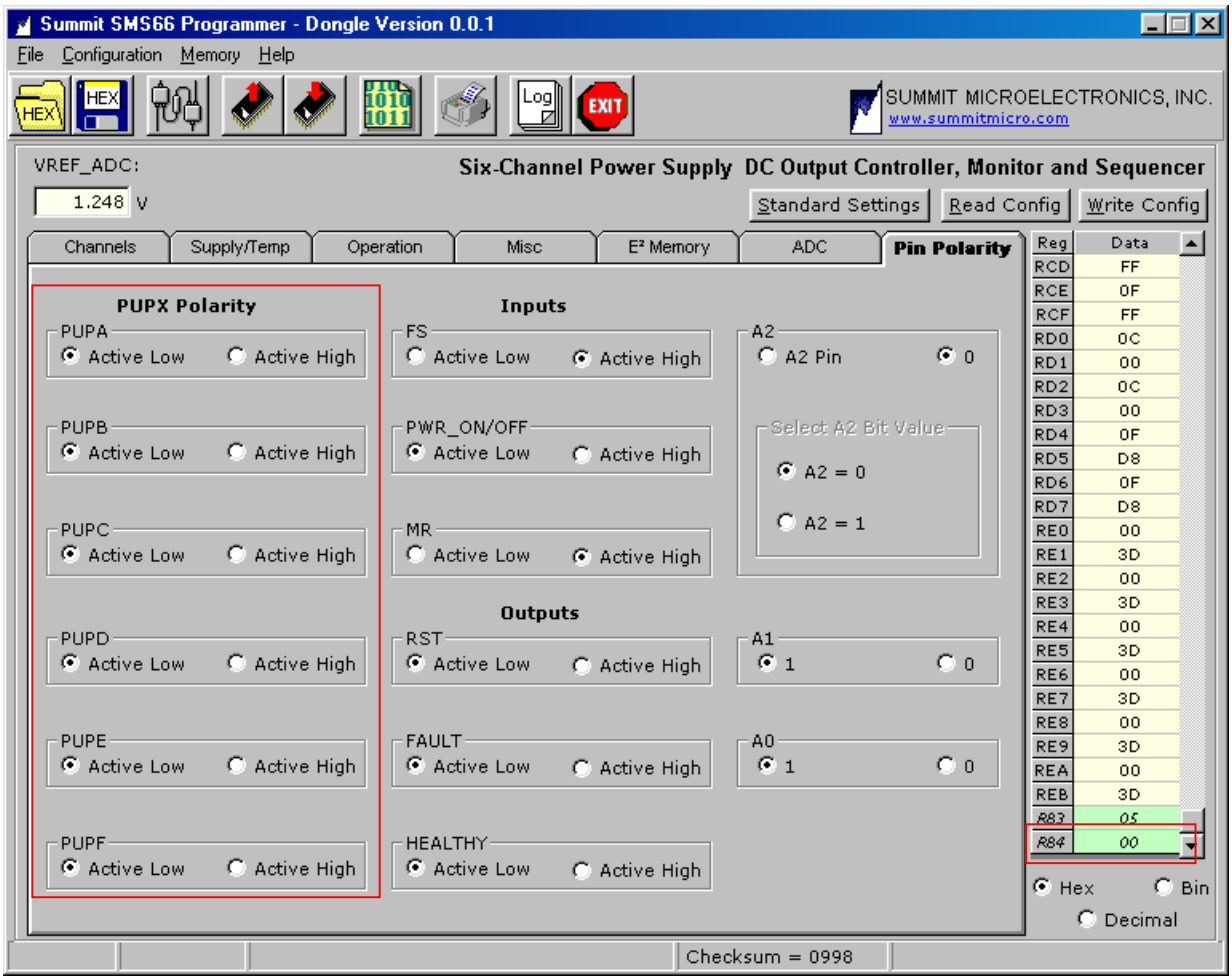

Figure 21 - Register R84 Windows GUI Pin Polarity Tab

Register R87 - Write Protection Register (Write-Only)

This volatile, write-only register disables write protection to the memory and configuration registers. This register powers up into a write protected state. Before a write operation is allowed, the code 0101_{BIN} must be written to this registers memory or configuration bits. The register must then be written with other data (----BIN) to write protect the memory or configuration. This feature is not available on the GUI.

Register R87								
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Action**
0	**1**	**0**	**1**					Memory Write Protection Disabled
X	**X**	**X**	**X**					Memory Write Protection Enabled
				0	**1**	**0**	**1**	Configuration Write Protection Disabled
				X	**X**	**X**	**X**	Configuration Write Protection Enabled

4k Nonvolatile General Purpose Memory Array

The memory array can be updated by writing data directly into the memory location. To write into a specific location, go to the Hex column location in the Tabular view and press the 'Backspace' key. Type in the new data and then press the 'Enter' key.

A graphic view of the memory can also be displayed for test purposes to check that the entire memory contents has changed or by writing pages or bytes, etc. using the buttons in the Graphic View Memory window.

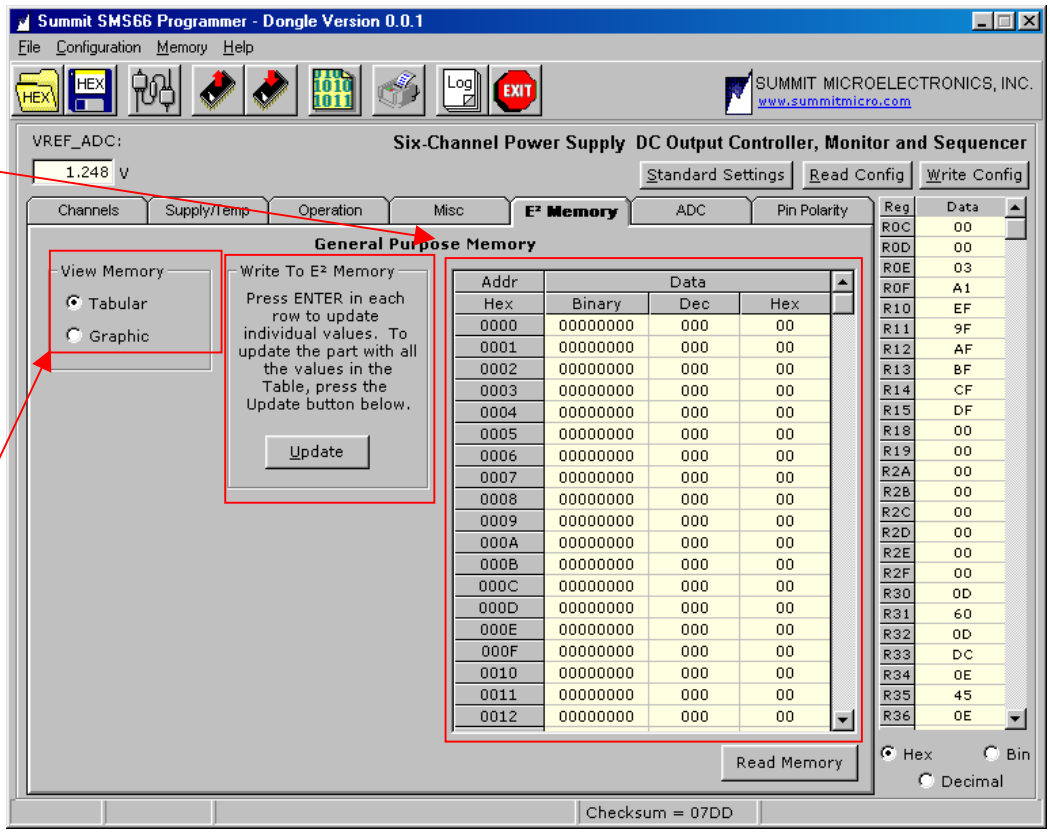

Figure 22 – E^2 Memory Windows GUI Tab

SMS66 Register Map

The following registers are accessed using slave address 101 SA0 A2 1 1 (SA0 = R0E[3])

R00 – R0B	Unused
R0C	[7] Regulator Output Voltage [6] Unused [5] Unused [4] Unused [3] Unused [2] Unused [1] Unused [0] Unused

R0D	[7] Configuration Lock [6] Wait For Internal Temp Before Power On [5] Unused [4] Unused [3] Unused [2] Unused [1] Unused [0] Unused
R0E	[7:6] Sequence Termination Timeout Period [5:4] Reset Timeout Period [3] Slave Address Select [2] A2 Address Bit [1] A1 Address Bit [0] A0 Address Bit
R0F	[7] Unused [6] Unused [5] Unused [4] Power-Off Sequencing Order [3] Restart (After a Force Shutdown) [2] Seq. Termination Timer During Power-Off [1] Wait For 12VIN Within Limits Before Power On [0] Wait For VDD Within Limits Before Power On
R10	[7] Use Channel A In Sequencing [6:4] Channel A Sequence Position [3:2] Channel A Power-On Delay [1:0] Channel A Power-Off Delay
R11	[7] Use Channel B In Sequencing [6:4] Channel B Sequence Position [3:2] Channel B Power-On Delay [1:0] Channel B Power-Off Delay
R12	[7] Use Channel C In Sequencing [6:4] Channel C Sequence Position [3:2] Channel C Power-On Delay [1:0] Channel C Power-Off Delay

R13	[7] Use Channel D In Sequencing [6:4] Channel D Sequence Position [3:2] Channel D Power-On Delay [1:0] Channel D Power-Off Delay
R14	[7] Use Channel E In Sequencing [6:4] Channel E Sequence Position [3:2] Channel E Power-On Delay [1:0] Channel E Power-Off Delay
R15	[7] Use Channel F In Sequencing [6:4] Channel F Sequence Position [3:2] Channel F Power-On Delay [1:0] Channel F Power-Off Delay
R16 – R7F	Unused

R80	[7] Channel A UV1 Triggers RST [6] Channel A UV1 Triggers HEALTHY [5] Channel A UV1 Triggers Power Off [4] Channel A UV1 Triggers Force Shutdown [3:2] Channel A UV1 Consecutive Conversions [1:0] UV1 - Channel A Low Limit 1 Bits [9:8]
R81	[7:0] Channel A Low Limit 1 Bits [7:0]
R82	[7] Channel A UV2 Triggers RST [6] Channel A UV2 Triggers HEALTHY [5] Channel A UV2 Triggers Power Off [4] Channel A UV2 Triggers Force Shutdown [3:2] Channel A UV2 Consecutive Conversions [1:0] UV1 - Channel A Low Limit 2 Bits [9:8]
R83	[7:0] Channel A Low Limit 2 Bits [7:0]
R84	[7] Channel A OV1 Triggers RST [6] Channel A OV1 Triggers HEALTHY [5] Channel A OV1 Triggers Power Off [4] Channel A OV1 Triggers Force Shutdown [3:2] Channel A OV1 Consecutive Conversions [1:0] UV1 - Channel A High Limit 1 Bits [9:8]
R85	[7:0] Channel A High Limit 1 Bits [7:0]
R86	[7] Channel A OV2 Triggers RST [6] Channel A OV2 Triggers HEALTHY [5] Channel A OV2 Triggers Power Off [4] Channel A OV2 Triggers Force Shutdown [3:2] Channel A OV2 Consecutive Conversions [1:0] UV1 - Channel A High Limit 2 Bits [9:8]
R87	[7:0] Channel A High Limit 2 Bits [7:0]
R88	[7] Channel B UV1 Triggers RST [6] Channel B UV1 Triggers HEALTHY [5] Channel B UV1 Triggers Power Off [4] Channel B UV1 Triggers Force Shutdown [3:2] Channel B UV1 Consecutive Conversions [1:0] UV1 - Channel B Low Limit 1 Bits [9:8]
R89	[7:0] Channel B Low Limit 1 Bits [7:0]
R8A	[7] Channel B UV2 Triggers RST [6] Channel B UV2 Triggers HEALTHY [5] Channel B UV2 Triggers Power Off [4] Channel B UV2 Triggers Force Shutdown [3:2] Channel B UV2 Consecutive Conversions [1:0] UV1 - Channel B Low Limit 2 Bits [9:8]
R8B	[7:0] Channel B Low Limit 2 Bits [7:0]
R8C	[7] Channel B OV1 Triggers RST [6] Channel B OV1 Triggers HEALTHY [5] Channel B OV1 Triggers Power Off [4] Channel B OV1 Triggers Force Shutdown [3:2] Channel B OV1 Consecutive Conversions [1:0] UV1 - Channel B High Limit 1 Bits [9:8]
R8D	[7:0] Channel B High Limit 1 Bits [7:0]
R8E	[7] Channel B OV2 Triggers RST [5] Channel B OV2 Triggers Power Off [6] Channel B OV2 Triggers HEALTHY [4] Channel B OV2 Triggers Force Shutdown [3:2] Channel B OV2 Consecutive Conversions [1:0] UV1 - Channel B High Limit 2 Bits [9:8]
R8F	[7:0] Channel B High Limit 2 Bits [7:0]
R90	[7] Channel C UV1 Triggers RST [6] Channel C UV1 Triggers HEALTHY [5] Channel C UV1 Triggers Power Off [4] Channel C UV1 Triggers Force Shutdown [3:2] Channel C UV1 Consecutive Conversions [1:0] UV1 - Channel C Low Limit 1 Bits [9:8]
R91	[7:0] Channel C Low Limit 1 Bits [7:0]
R92	[7] Channel C UV2 Triggers RST [6] Channel C UV2 Triggers HEALTHY [5] Channel C UV2 Triggers Power Off [4] Channel C UV2 Triggers Force Shutdown [3:2] Channel C UV2 Consecutive Conversions [1:0] UV1 - Channel C Low Limit 2 Bits [9:8]
R93	[7:0] Channel C Low Limit 2 Bits [7:0]
R94	[7] Channel C OV1 Triggers RST [6] Channel C OV1 Triggers HEALTHY [5] Channel C OV1 Triggers Power Off [4] Channel C OV1 Triggers Force Shutdown [3:2] Channel C OV1 Consecutive Conversions [1:0] UV1 - Channel C High Limit 1 Bits [9:8]
R95	[7:0] Channel C High Limit 1 Bits [7:0]
R96	[7] Channel C OV2 Triggers RST [6] Channel C OV2 Triggers HEALTHY [5] Channel C OV2 Triggers Power Off [4] Channel C OV2 Triggers Force Shutdown [3:2] Channel C OV2 Consecutive Conversions [1:0] UV1 - Channel C High Limit 2 Bits [9:8]
R97	[7:0] Channel C High Limit 2 Bits [7:0]

R98	[7] Channel D UV1 Triggers RST [6] Channel D UV1 Triggers HEALTHY [5] Channel D UV1 Triggers Power Off [4] Channel D UV1 Triggers Force Shutdown [3:2] Channel D UV1 Consecutive Conversions [1:0] UV1 - Channel D Low Limit 1 Bits [9:8]
R99	[7:0] Channel D Low Limit 1 Bits [7:0]
R9A	[7] Channel D UV2 Triggers RST [6] Channel D UV2 Triggers HEALTHY [5] Channel D UV2 Triggers Power Off [4] Channel D UV2 Triggers Force Shutdown [3:2] Channel D UV2 Consecutive Conversions [1:0] UV1 - Channel D Low Limit 2 Bits [9:8]
R9B	[7:0] Channel D Low Limit 2 Bits [7:0]
R9C	[7] Channel D OV1 Triggers RST [6] Channel D OV1 Triggers HEALTHY [5] Channel D OV1 Triggers Power Off [4] Channel D OV1 Triggers Force Shutdown [3:2] Channel D OV1 Consecutive Conversions [1:0] UV1 - Channel D High Limit 1 Bits [9:8]
R9D	[7:0] Channel D High Limit 1 Bits [7:0]
R9E	[7] Channel D OV2 Triggers RST [6] Channel D OV2 Triggers HEALTHY [5] Channel D OV2 Triggers Power Off [4] Channel D OV2 Triggers Force Shutdown [3:2] Channel D OV2 Consecutive Conversions [1:0] UV1 - Channel D High Limit 2 Bits [9:8]
R9F	[7:0] Channel D High Limit 2 Bits [7:0]
RA0	[7] Channel E UV1 Triggers RST [6] Channel E UV1 Triggers HEALTHY [5] Channel E UV1 Triggers Power Off [4] Channel E UV1 Triggers Force Shutdown [3:2] Channel E UV1 Consecutive Conversions [1:0] UV1 - Channel E Low Limit 1 Bits [9:8]
RA1	[7:0] Channel E Low Limit 1 Bits [7:0]
RA2	[7] Channel E UV2 Triggers RST [6] Channel E UV2 Triggers HEALTHY [5] Channel E UV2 Triggers Power Off [4] Channel E UV2 Triggers Force Shutdown [3:2] Channel E UV2 Consecutive Conversions [1:0] UV1 - Channel E Low Limit 2 Bits [9:8]
RA3	[7:0] Channel E Low Limit 2 Bits [7:0]

RA4	[7] Channel E OV1 Triggers RST [6] Channel E OV1 Triggers HEALTHY [5] Channel E OV1 Triggers Power Off [4] Channel E OV1 Triggers Force Shutdown [3:2] Channel E OV1 Consecutive Conversions [1:0] UV1 - Channel E High Limit 1 Bits [9:8]
RA5	[7:0] Channel E High Limit 1 Bits [7:0]
RA6	[7] Channel E OV2 Triggers RST [6] Channel E OV2 Triggers HEALTHY [5] Channel E OV2 Triggers Power Off [4] Channel E OV2 Triggers Force Shutdown [3:2] Channel E OV2 Consecutive Conversions [1:0] UV1 - Channel E High Limit 2 Bits [9:8]
RA7	[7:0] Channel E High Limit 2 Bits [7:0]
RA8	[7] Channel F UV1 Triggers RST [6] Channel F UV1 Triggers HEALTHY [5] Channel F UV1 Triggers Power Off [4] Channel F UV1 Triggers Force Shutdown [3:2] Channel F UV1 Consecutive Conversions [1:0] UV1 - Channel F Low Limit 1 Bits [9:8]
RA9	[7:0] Channel F Low Limit 1 Bits [7:0]
RAA	[7] Channel F UV2 Triggers RST [6] Channel F UV2 Triggers HEALTHY [5] Channel F UV2 Triggers Power Off [4] Channel F UV2 Triggers Force Shutdown [3:2] Channel F UV2 Consecutive Conversions [1:0] UV1 - Channel F Low Limit 2 Bits [9:8]
RAB	[7:0] Channel F Low Limit 2 Bits [7:0]
RAC	[7] Channel F OV1 Triggers RST [6] Channel F OV1 Triggers HEALTHY [5] Channel F OV1 Triggers Power Off [4] Channel F OV1 Triggers Force Shutdown [3:2] Channel F OV1 Consecutive Conversions [1:0] UV1 - Channel F High Limit 1 Bits [9:8]
RAD	[7:0] Channel F High Limit 1 Bits [7:0]
RAE	[7] Channel F OV2 Triggers RST [6] Channel F OV2 Triggers HEALTHY [5] Channel F OV2 Triggers Power Off [4] Channel F OV2 Triggers Force Shutdown [3:2] Channel F OV2 Consecutive Conversions [1:0] UV1 - Channel F High Limit 2 Bits [9:8]
RAF	[7:0] Channel F High Limit 2 Bits [7:0]

RB0	[7] VDD UV1 Triggers RST [6] VDD UV1 Triggers HEALTHY [5] VDD UV1 Triggers Power Off [4] VDD UV1 Triggers Force Shutdown [3:2] VDD UV1 Consecutive Conversions [1:0] UV1 - VDD Low Limit 1 Bits [9:8]
RB1	[7:0] VDD Low Limit 1 Bits [7:0]
RB2	[7] VDD UV2 Triggers RST [6] VDD UV2 Triggers HEALTHY [5] VDD UV2 Triggers Power Off [4] VDD UV2 Triggers Force Shutdown [3:2] VDD UV2 Consecutive Conversions [1:0] UV1 - VDD Low Limit 2 Bits [9:8]
RB3	[7:0] VDD Low Limit 2 Bits [7:0]
RB4	[7] VDD OV1 Triggers RST [6] VDD OV1 Triggers HEALTHY [5] VDD OV1 Triggers Power Off [4] VDD OV1 Triggers Force Shutdown [3:2] VDD OV1 Consecutive Conversions [1:0] UV1 - VDD High Limit 1 Bits [9:8]
RB5	[7:0] VDD High Limit 1 Bits [7:0]
RB6	[7] VDD OV2 Triggers RST [6] VDD OV2 Triggers HEALTHY [5] VDD OV2 Triggers Power Off [4] VDD OV2 Triggers Force Shutdown [3:2] VDD UV2 Consecutive Conversions [1:0] UV1 - VDD High Limit 2 Bits [9:8]
RB7	[7:0] Channel VDD High Limit 2 Bits [7:0]
RB8	[7] 12VIN UV1 Triggers RST [6] 12VIN UV1 Triggers HEALTHY [5] 12VIN UV1 Triggers Power Off [4] 12VIN UV1 Triggers Force Shutdown [3:2] 12VIN UV1 Consecutive Conversions [1:0] UV1 – 12VIN Low Limit 1 Bits [9:8]
RB9	[7:0] 12VIN Low Limit 1 Bits [7:0]
RBA	[7] 12VIN UV2 Triggers RST [6] 12VIN UV2 Triggers HEALTHY [5] 12VIN UV2 Triggers Power Off [4] 12VIN UV2 Triggers Force Shutdown [3:2] 12VIN UV2 Consecutive Conversions [1:0] UV1 – 12VIN Low Limit 2 Bits [9:8]
RBB	[7:0] Channel 12VIN Low Limit 2 Bits [7:0]

RBC	[7] 12VIN OV1 Triggers RST [6] 12VIN OV1 Triggers HEALTHY [5] 12VIN OV1 Triggers Power Off [4] 12VIN OV1 Triggers Force Shutdown [3:2] 12VIN OV1 Consecutive Conversions [1:0] UV1 – 12VIN High Limit 1 Bits [9:8]
RBD	[7:0] 12VIN High Limit 1 Bits [7:0]
RBE	[7] 12VIN OV2 Triggers RST [6] 12VIN OV2 Triggers HEALTHY [5] 12VIN OV2 Triggers Power Off [4] 12VIN OV2 Triggers Force Shutdown [3:2] 12VIN OV2 Consecutive Conversions [1:0] UV1 – 12VIN High Limit 2 Bits [9:8]
RBF	[7:0] Channel 12VIN High Limit 2 Bits [7:0]
RC0	[7] Internal Temp Sense UT1 Triggers RST [6] Internal Temp Sense UT1 Triggers HEALTHY [5] Internal Temp Sense UT1 Triggers Power Off [4] Internal Temp Sense UT1 Triggers Force Shutdown [3:2] Internal Temp Sense UT1 Consecutive Conversions [0:1] UV1 - Internal Temp Sense UT1 Bits [9:8]
RC1	[0:7] Internal Temp Sense UT1 Bits [7:0]
RC2	[7] Internal Temp Sense UT2 Triggers RST [6] Internal Temp Sense UT2 Triggers HEALTHY [5] Internal Temp Sense UT2 Triggers Power Off [4] Internal Temp Sense UT2 Triggers Force Shutdown [3:2] Internal Temp Sense UT2 Consecutive Conversions [0:1] Internal Temp Sense UT2 Bits [9:8]
RC3	[0:7] Internal Temp Sense UT2 Bits [7:0]
RC4	[7] Internal Temp Sense OT1 Triggers RST [6] Internal Temp Sense OT1 Triggers HEALTHY [5] Internal Temp Sense OT1 Triggers Power Off [4] Internal Temp Sense OT1 Triggers Force Shutdown [3:2] Internal Temp Sense OT1 Consecutive Conversions [0:1] Internal Temp Sense OT1 Bits [9:8]

RC5	[0:7] Internal Temp Sense OV1 Bits [7:0]
RC6	[7] Internal Temp Sense OT2 Triggers RST [6] Internal Temp Sense OT2 Triggers HEALTHY [5] Internal Temp Sense OT2 Triggers Power Off [4] Internal Temp Sense OT2 Triggers Force Shutdown [3:2] Internal Temp Sense OT2 Consecutive Conversions [0:1] Internal Temp Sense OT2 Bits [9:8]
RC7	[0:7] Internal Temp Sense OT2 Bits [7:0]
RC8	[7] AIN1 UV1 Triggers RST [6] AIN1 UV1 Triggers HEALTHY [5] AIN1 UV1 Triggers Power Off [4] AIN1 UV1 Triggers Force Shutdown [3:2] AIN1 UV1 Consecutive Conversions [0:1] AIN1 UV1 Bits [9:8]
RC9	[0:7] AIN1 UV1 Bits [7:0]
RCA	[7] AIN1 UV2 Triggers RST [6] AIN1 UV2 Triggers HEALTHY [5] AIN1 UV2 Triggers Power Off [4] AIN1 UV2 Triggers Force Shutdown [3:2] AIN1 UV2 Consecutive Conversions [0:1] AIN1 UV2 Bits [9:8]
RCB	[0:7] AIN1 UV2 Bits [7:0]
RCC	[7] AIN1 OV1 Triggers RST [6] AIN1 OV1 Triggers HEALTHY [5] AIN1 OV1 Triggers Power Off [4] AIN1 OV1 Triggers Force Shutdown [3:2] AIN1 OV1 Consecutive Conversions [0:1] AIN1 OV1 Bits [9:8]
RCD	[0:7] AIN1 OV1 Bits [7:0]
RCE	[7] AIN1 OV2 Triggers RST [6] AIN1 OV2 Triggers HEALTHY [5] AIN1 OV2 Triggers Power Off [4] AIN1 OV2 Triggers Force Shutdown [3:2] AIN1 OV2 Consecutive Conversions [0:1] AIN1 OV2 Bits [9:8]
RCF	[0:7] AIN1 OV2 Bits [7:0]
RD0	[7] AIN2 UV1 Triggers RST [6] AIN2 UV1 Triggers HEALTHY [5] AIN2 UV1 Triggers Power Off [4] AIN2 UV1 Triggers Force Shutdown [3:2] AIN2 UV1 Consecutive Conversions [0:1] AIN2 UV1 Bits [9:8]
RD1	[0:7] AIN2 UV1 Bits [7:0]
RD2	[7] AIN2 UV2 Triggers RST [6] AIN2 UV2 Triggers HEALTHY [5] AIN2 UV2 Triggers Power Off [4] AIN2 UV2 Triggers Force Shutdown [3:2] AIN2 UV2 Consecutive Conversions [0:1] AIN2 UV2 Bits [9:8]
RD3	[0:7] AIN2 UV2 Bits [7:0]
RD4	[7] AIN2 OV1 Triggers RST [6] AIN2 OV1 Triggers HEALTHY [5] AIN2 OV1 Triggers Power Off [4] AIN2 OV1 Triggers Force Shutdown [3:2] AIN2 OV1 Consecutive Conversions [0:1] AIN2 OV1 Bits [9:8]
RD5	[0:7] AIN2 OV1 Bits [7:0]
RD6	[7] AIN2 OV2 Triggers RST [6] AIN2 OV2 Triggers HEALTHY [5] AIN2 OV2 Triggers Power Off [4] AIN2 OV2 Triggers Force Shutdown [3:2] AIN2 OV2 Consecutive Conversions [0:1] AIN2 OV2 Bits [9:8]
RD7	[0:7] AIN2 OV2 Bits [7:0]
RD8 TO RDF	Unused
RE0	[7] Channel A OFF Limit Triggers RST [6] Channel A OFF Limit Triggers HEALTHY [5] Channel A OFF Limit Triggers Power Off [4] Channel A OFF Limit Triggers Force Shutdown [3:2] Channel A OFF Limit Consecutive Conversions [0:1] Channel A OFF Limit Bits [9:8]
RE1	[7:0] Channel A OFF Limit Bits [7:0]

RE2	[7] Channel B OFF Limit Triggers RST [6] Channel B OFF Limit Triggers HEALTHY [5] Channel B OFF Limit Triggers Power Off [4] Channel B OFF Limit Triggers Force Shutdown [3:2] Channel B OFF Limit Consecutive Conversions [0:1] Channel B OFF Limit Bits [9:8]
RE3	[7:0] Channel B OFF Limit Bits [7:0]
RE4	[7] Channel C OFF Limit Triggers RST [6] Channel C OFF Limit Triggers HEALTHY [5] Channel C OFF Limit Triggers Power Off [4] Channel C OFF Limit Triggers Force Shutdown [3:2] Channel C OFF Limit Consecutive Conversions [0:1] Channel C OFF Limit Bits [9:8]
RE5	[7:0] Channel C OFF Limit Bits [7:0]
RE6	[7] Channel D OFF Limit Triggers RST [6] Channel D OFF Limit Triggers HEALTHY [5] Channel D OFF Limit Triggers Power Off [4] Channel D OFF Limit Triggers Force Shutdown [3:2] Channel D OFF Limit Consecutive Conversions [0:1] Channel D OFF Limit Bits [9:8]
RE7	[7:0] Channel D OFF Limit Bits [7:0]
RE8	[7] Channel E OFF Limit Triggers RST [6] Channel E OFF Limit Triggers HEALTHY [5] Channel E OFF Limit Triggers Power Off [4] Channel E OFF Limit Triggers Force Shutdown [3:2] Channel E OFF Limit Consecutive Conversions [0:1] Channel E OFF Limit Bits [9:8]
RE9	[7:0] Channel E OFF Limit Bits [7:0]
REA	[7] Channel F OFF Limit Triggers RST [6] Channel F OFF Limit Triggers HEALTHY [5] Channel F OFF Limit Triggers Power Off [4] Channel F OFF Limit Triggers Force Shutdown [3:2] Channel F OFF Limit Consecutive Conversions [0:1] Channel F OFF Limit Bits [9:8]
REB	[7:0] Channel F OFF Limit Bits [7:0]

The following registers are accessed using slave address 1001 A2 A1 A0

R00	[7:3] = [00000]ADC channel for Channel A [2] = 0 [1:0] Bits [9:8] of ADC data for Channel A
R01	[7:0] Bits [7:0] of ADC data for Channel A
R02 to R07	Unused
R08	[7:3] = [00001]ADC channel for Channel B [2] = 0 [1:0] Bits [9:8] of ADC data for Channel B
R09	[7:0] Bits [7:0] of ADC data for Channel B
R1A to R1F	Unused
R10	[7:3] = [00010]ADC channel for Channel C [2] = 0 [1:0] Bits [9:8] of ADC data for Channel C
R11	[7:0] Bits [7:0] of ADC data for Channel C
R12 to R17	Unused
R18	[7:3] = [00011]ADC channel for Channel D [2] = 0 [1:0] Bits [9:8] of ADC data for Channel D
R19	[7:0] Bits [7:0] of ADC data for Channel D
R1A to R1F	Unused
R20	[7:3] = [00100]ADC channel for Channel E [2] = 0 [1:0] Bits [9:8] of ADC data for Channel E
R21	[7:0] Bits [7:0] of ADC data for Channel E
R22 to R27	Unused
R28	[7:3] = [00101]ADC channel for Channel F [2] = 0 [1:0] Bits [9:8] of ADC data for Channel F
R29	[7:0] Bits [7:0] of ADC data for Channel F
R2A to R2F	Unused
R30	[7:3] = [00110]ADC channel for Channel VDD [2] = 0 [1:0] Bits [9:8] of ADC data for Channel VDD
R31	[7:0] Bits [7:0] of ADC data for Channel VDD
R32 to R37	Unused
R38	[7:3] = [00111]ADC channel for Channel 12VIN [2] = 0 [1:0] Bits [9:8] of ADC data for Channel 12VIN
R39	[7:0] Bits [7:0] of ADC data for Channel 12VIN
R3A to R3F	Unused
R40	[7:3] = [01000]ADC channel for Channel INT_TEMP [2] = 0 [1:0] Bits [9:8] of ADC data for Channel INT_TEMP
R41	[7:0] Bits [7:0] of ADC data for Channel INT_TEMP
R42 to R47	Unused
R48	[7:3] = [01001]ADC channel for Channel AIN1 [2] = 0 [1:0] Bits [9:8] of ADC data for Channel AIN1
R49	[7:0] Bits [7:0] of ADC data for Channel AIN1
R4A to R4F	Unused
R50	[7:3] = [01010]ADC channel for Channel AIN2 [2] = 0 [1:0] Bits [9:8] of ADC data for Channel AIN2
R51	[7:0] Bits [7:0] of ADC data for Channel AIN2

R52 to R7F	Unused
R80	[7:5] I²C Commands: 000X XXXX Does nothing 100X XXXX I²C Power-On 010X XXXX I²C Power-Off 001X XXXX I²C Force Shutdown [4] Unused [3] Sequenced channels out of fault (read only) [2] Sequenced channels below off limit (read only) [1:0] Unused
R81	[7] Sequence Aborted [6:4] Sequence position when aborted [3] Unused [2] AIN2 Fault [1] AIN1 Fault [0] Int Temp Fault
R82	[7] 12VIN Fault [6] VDD Fault [5] Channel F Fault [4] Channel E Fault [3] Channel D Fault [2] Channel C Fault [1] Channel B Fault [0] Channel A Fault
R83	[7:6] Unused [5] HEALTHY pad polarity [4] FAULT pad polarity [3] RST pad polarity [2] MR polarity [1] PWR_ON polarity [0] FS Polarity
R84	[7:6] Unused [5] PUP F Polarity [4] PUP E Polarity [3] PUP D Polarity [2] PUP C Polarity [1] PUP B Polarity [0] PUP A Polarity
R85, R86	Unused
R87	[7:4] Write Protect Memory [3:0] Write Protect Config
R88	Revision