Application Note 42

Obtaining Optimum Performance with Summit's ADOC[TM]/Marginer Family

INTRODUCTION

Systems are migrating from distributed power architectures to Point-of-Load (POL) design to gain better regulation and control at the load. Providing power at the load gives superior regulation transient response and avoids voltage drops across PCB traces and planes. This is necessary as voltage levels decrease and allowable supply variations around these levels also decrease. These tighter voltage limits demand accurate control especially under full load conditions to maintain performance.

Summit's family of Active DC Output Controllers (ADOC[TM]) was designed to accurately control the voltage accuracy and margining of DC-DC converters. The SMM105 is targeted for POL (Point Of Load) applications requiring extremely accurate control of the converter's voltage while the SMM205/605/665 for centralized applications where multiple voltages are used. The information in this App Note is intended to focus on obtaining the highest possible performance from Summit's Marginers and to avoid creating unnecessary problems by presenting a more detailed functional description of these devices.

Why Margin?

Voltage margining is performed in systems to test components at their worst case operating voltage extremes in order to find weak or marginal devices and replace them to improve overall reliability. For example, a 3.3V supply may be margined to a logic family's high operating voltage of 3.465V (+5%) and to its low operating voltage of 3.135V (-5%). Summit's marginers provide an additional measure of safety to voltage margining by accurately setting the target supply to its nominal voltage prior to margining. This practice greatly enhances the usefulness of voltage margining by improving the inherent ±2% to ±4% nominal stated accuracy of the DC-DC converter to ±0.2% to ensure the target margin voltage does not under or over-stress the components in question when the margin voltage is added (or subtracted) with an inaccurate nominal supply voltage.

Make certain that when choosing an existing marginer solution, the overall accuracy is well understand and is not hidden in some obscure specification not readily found in the manufacturer's data sheet. For example, one vendor advertises a margin accuracy of <0.4% but upon further examination of the vendor's data sheet and after performing numerous calculations it is found the advertised accuracy is only attainable when the vendor's device and the external components contain no inaccuracies. Summit's marginers require little or no calculations due too the active feedback adjustment of the output level. The only sources of margin inaccuracies are the marginer itself and the external reference, if used. Summit's advertised accuracy is easily attained without component tuning or selection.

Accuracy

Of the marginer family, the SMM665 contains two functional blocks both of which are designed for high accuracy. The ADOC block is that portion of the device that controls the DC-DC converter output voltage and the ADC block is the portion that monitors the converter voltages and is also available to the user as digital data.

Obtaining ADOC Accuracy

The base accuracy of the marginer ADOC function is ±0.1% over temperature plus the accuracy of the reference used. To obtain ±0.2% accuracy an inexpensive ±0.1% external reference is commonly used. When the internal reference is used the ADOC accuracy is ±0.5% across temperature. To ensure this accuracy is achieved, locate the external voltage reference near the marginer; making a direct PCB trace connection from the low side of the voltage reference to the marginer's GND pin (Fig. 1) and from the reference output pin to the marginer VREF_CNTL pin (Fig. 1).

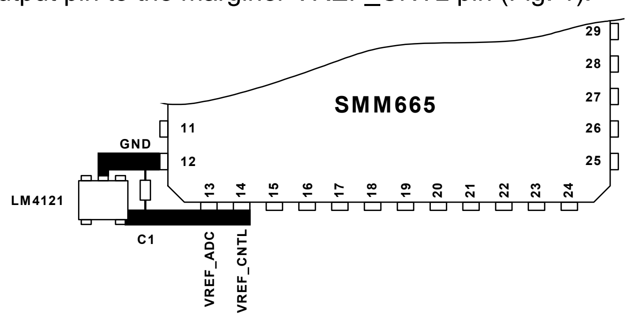

Figure 1. VREF to SMM665 PCB Connection

Although it may be convenient to make the GND connections to an inner layer using a copper via, the method shown in Figure 1 is preferred because it is unaffected by other currents returning to the GND pin. Make certain to use a bypass capacitor (C1) from the reference output to GND as recommended by the manufacturer. If using the marginer's internal reference bypass the VREF_CNTL pin directly to the GND pin with a 0.1µF ceramic capacitor.

Choosing the Reference Voltage

All of Summit's marginers contain an internal voltage reference of 1.25V nominal resulting in an overall accuracy of ±0.5%. Higher accuracies may be achieved by using an external reference with an accuracy of at ≤±0.2%. Further, the reference voltage is internally scaled by 4 times limiting the upper voltage that may be monitored or controlled to 5V for a 1.25V reference.

When using an external reference, a 1.25V nominal voltage results in the best overall accuracy using the factory default hex file program settings. Other popular voltage reference values may be used and are most accurate when factory trimmed for the exact value. When ordering samples, specify the nearest reference voltage being used (Table 1) to obtain the best possible accuracy. In production, the reference value is determined by the HEX file contents generated from the Windows GUI.

Table 1: Voltage Reference Selection Guide

1. 1.024V	2. 1.250V
3. 2.048V	4. 2.500V
5. 3.000V	6. 3.300V

Although the voltage chosen for a certain application may not be present in Table 1, the breakpoints are chosen so that no degradation in accuracy is experienced when using unlisted values. Be certain to specify the voltage closest to the actual reference used.

Choosing the Internal Voltage Regulator Setting

With +12V Supply

The internal voltage regulator powers the marginer's logic and other functional blocks including the I^2C communication bus. Select the internal voltage regulator (3.6V or 5.5V) so that the highest input voltage to be margined is less than or equal that chosen. For example, in a system margining a 5V supply, the internal regulator must be set to 5.5V. If the system uses a lower voltage (e.g., 3.3V) for the I^2C communications a level shifter must be placed between the I^2C master and the marginer clock and data lines to boost the voltage swing to 5V. If a 5V I^2C bus is used the level shifter is not required.

Without +12V Supply

When a 12V supply is unavailable the marginer is powered from the VDD pin and the internal regulator is selected so the highest margined voltage is less than the internal regulator. For example, if the system's highest monitored/margined voltage is 5V, this supply is connected to both the VDD pin and to one of the VMX pins. Again the internal regulator is set either 5.5V because the 5V is being margined and is the highest voltage. If it were not being margined, it is permissible to set the internal regulator to 3.6V if the I^2C bus is operating at this voltage, thereby preventing the need for a level shifter between the I^2C master and the margining device.

$TRIM\_CAP_X$: Selection and Proper Placement

The $TRIM\_CAP_X$ serves as the storage element for the ADOC operation and as such requires attention be paid to its maximum leakage and placement with respect to the margining device.

The maximum allowable leakage from the $TRIM\_CAP_X$ pin is:

Eq: 1: $$I_{L(TRIM\_CAP_X\_Node)} \le \left(\frac{5\mu S \cdot 30\mu A}{0.0017S}\right) \le 87nA$$

Allowing for PCB and other leakage sources use 50nA as the maximum leakage allowed from the $TRIM\_CAP_X$ node capacitor. For a circuit having an average voltage of 5V on the $TRIM\_CAP_X$ capacitor, the maximum allowable leakage (IR) resistance of the capacitor is:

Eq 2: $$R_{L(TRIM\_CAP_X)} \ge \left(\frac{5V}{50nA}\right) \ge 100M\Omega$$

Many vendors offer an X7R type ceramic capacitor with adequate IR (insulation resistance) to be suitable for the ADOC $TRIM\_CAP_X$ (see list below) for the 1µF value suggested. Be certain the ceramic capacitor chosen also meets or exceeds the IR requirements at elevated temperatures. A general rule to follow for this application is to use a capacitor with R-C product of 500 MΩ-µF or higher.

Film capacitors do offer much higher IR ratings but at both a cost and space premium. These may be used as an alternative but are generally not required.

$TRIM\_CAP_X$: Recommended Suppliers:

Kemet: C0805C105K9RAC, 1µF, 0805, +-10%, 6.3V
http://www.kemet.com
AVX: 08056C105KAT4A, 1µF, 0805, +-10%, 6.3V
http://www.avxcorp.com
TDK p/n: C2012X7R1C105K, 1µF, 2012, +-10%, 16V
http://www.component.tdk.com
NIC Components Corporation: p/n
NMC0805X7R105K16TRP, 1µF, 0805, +-10%, 16V
http://www.niccomp.com

Figure 2 illustrates the use of a 'star-ground' to connect all the TRIM_CAP$_X$ capacitors together directly to the marginer's GND pin. If the space under the device is unavailable the use of via's from the capacitors to a ground plane or layer is acceptable providing no other currents are flowing in that area of the plane or that they are minimized.

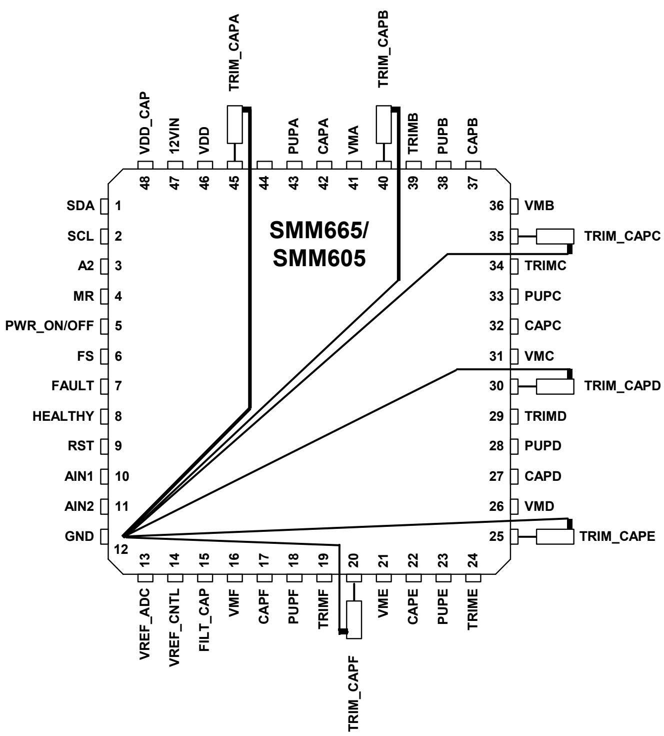

Figure 2. 'Star-Ground' made to all TRIM_CAP$_X$'s

FILT_CAP : Selection and Proper Placement

The function of the FILT_CAP is to filter the converter's noise for the ADOC measurement. Each VM$_X$ input is internally multiplexed to the FILT_CAP pin through a 1k series resistor each time a channel is sampled. This pin must have a 1nF-22nF capacitor to filter the converter noise within each channel's ADOC sample time interval. An ordinary ceramic capacitor is suitable for this function. Place this component nearby the device making the pin and GND connections as short as possible avoiding any ground loops or noise pickup from high current paths.

VM$_X$ and GND : The measurement inputs.

The ADOC measurement is performed between the VM$_X$ and the GND pins. When using the SMM105 make a connection from the measurement of interest (the load) directly to the device's GND pin and the VM$_X$ input (Figure 3).

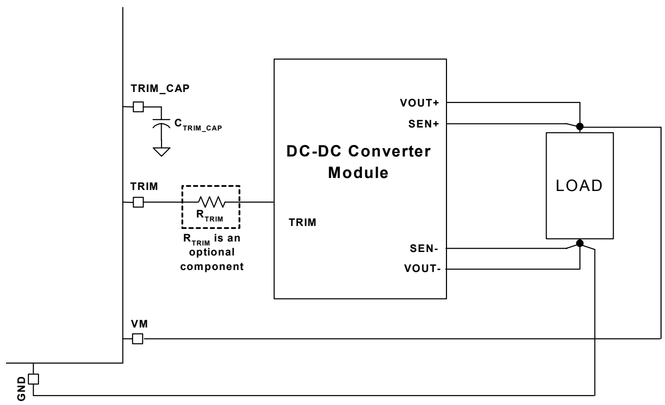

Figure 3. VM$_X$/GND correct PCB connections

Figure 4 displays a layout using the SMM105 and the connections made between the device and the correct sensing points with respect to the supply and the load.

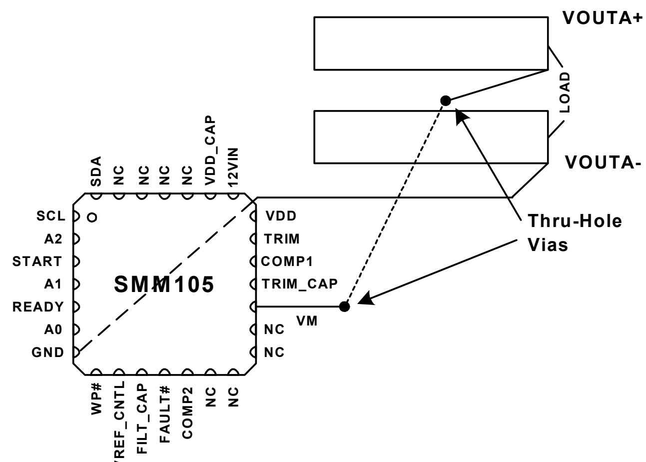

Figure 4. VM/GND Connection to Single Load

When multiple channel devices are used employ the same trace connection to the VM$_X$ pins while making the GND connection to the return of the supply requiring the most accurate monitoring at the point of load. This is most often the lowest system supply voltage. Figure 5 displays a PCB layout using the SMM205 and 2 DC-DC converters. Note the GND connection is made midway between the common ground plane between the returns of the 2 converters.

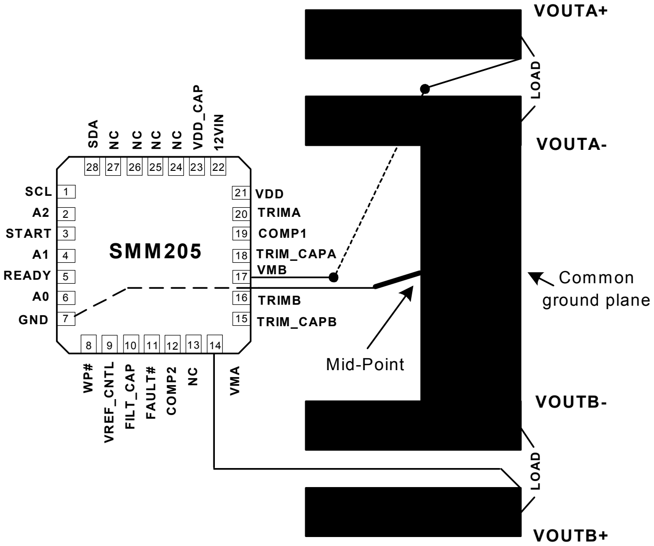

Figure 5. VM_X/GND Connections to 2 Loads
The PUP outputs: Pullup resistor selection

Excessive currents flowing into the PUP outputs can contribute to measurement errors. Minimize these currents to less than 3mA total by using the largest possible resistor value that will ensure a high noise margin to avoid false turn-on of the DC-DC converters. If the PUP currents are unavoidably excessive, use a buffer between the PUP outputs and the converter's ENABLE pin (Figure 6).

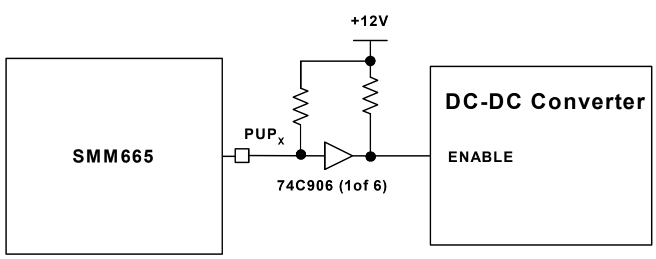

Figure 6. Use a buffer to reduce/eliminate PUP currents

ADC Accuracy

The ADC is a separate functional block than the ADOC and is used for monitoring and reading channel supply voltages. As it is a separate block, certain external components are required to optimize its accuracy and separate it from the ADOC function.

CAP_X : Selection and Proper Placement

This component is used to filter switching noise on each VM_X input prior to inputting into the ADC. The capacitor forms a low-pass filter with the marginer's internal resistive divider (Figure 7).

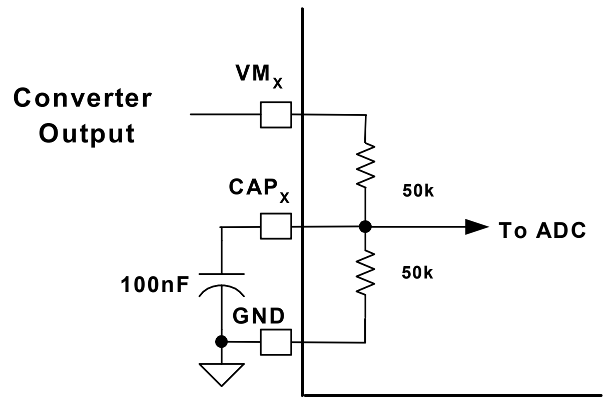

Figure 7. CAP_X and VM_X Filter Action

The minimum recommended value for CAP_X is 80nF placing the -3dB filter point at 80Hz; well below the ripple and noise voltage caused by the converter's switching frequency.

The value of CAP_X is also important for eliminating last sequence position overshoot. Overshoot during sequence on of the power supplies can occur on the last sequence position if ADOC is enabled on the channel(s) and if the UV1 setting of that channel(s) is less than 80% of the channel's nominal voltage. This is due to the TRIM_CAP_X capacitor not reaching the nominal value of the converter's TRIM pin voltage before the UV1 setting is reached by the converter's output.

The charging current available from the TRIM_CAP_X node during sequencing is 1mA and assuming a final TRIM voltage of 1.25V the time to fully charge a 1µF TRIMCAP$_X$ capacitor is:

$$\text{Eq 3: } t_{TRIM\_CAPx} = \frac{1.25\times 1\times 10^{-6}}{0.001} = 1.25mS$$

To prevent overshoot choose the RC time constant consisting of the internal R = 25k and the CAP_X capacitor so the input to the ADC lags the converter output by 2ms. This allows the TRIM_CAPX node to be fully charged before the device enables ADOC thus preventing overshoot (See Figures 9-12). For TRIM_CAP_X capacitors larger than 1µF the 2ms time constant should be multiplied by:

$$\text{Eq 4: } t_{TRIM\_CAPx}t = 2mS \times \frac{TRIM\_CAPx}{1\mu F}$$

Overshoot can also occur on the devices using a START pin (SMM105, SMM205 & SMM605) to begin the ADOC event. Make certain this pin is de-asserted for a short delay time (2-5mS) after powering the marginer to ensure the TRIM_CAP$_X$ is fully charged before the ADOC is started.

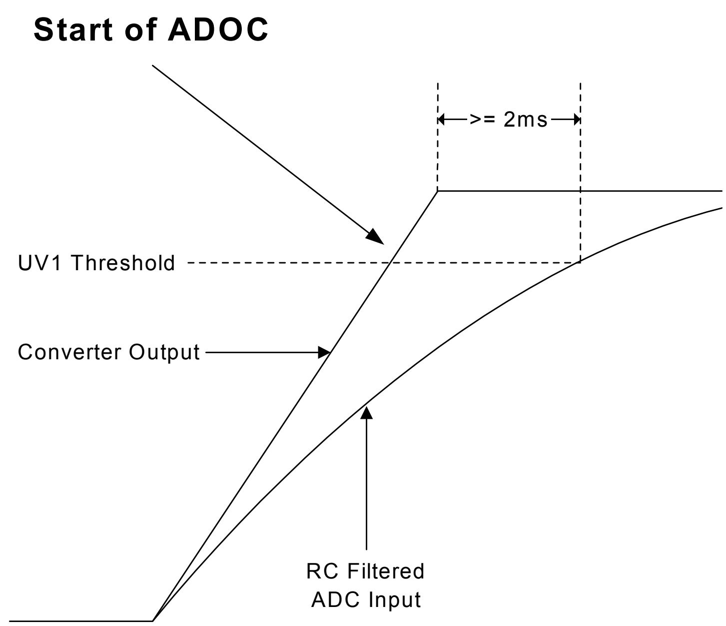

Figure 8: The input to the device's ADC lags the converter according to the time constant of the internal 25kΩ and the CAP$_X$ value. Choosing a time constant of 2mS per µF of TRIMCAP$_X$ guarantees the device to be ready (TRIMCAPX fully charged) before ADOC is engaged.

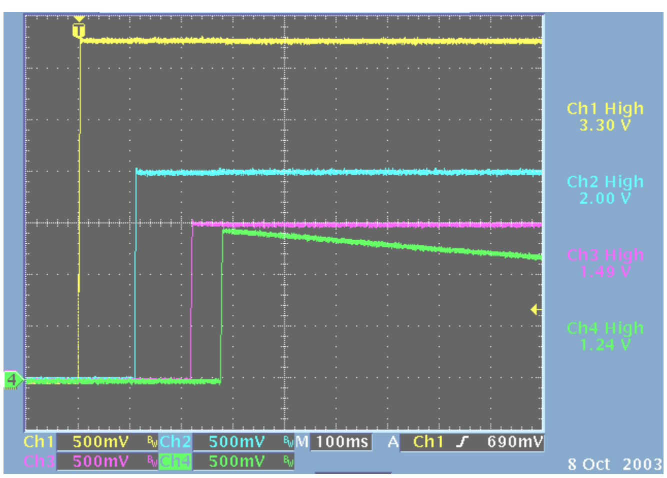

Figure 9: Last Sequence Position Overshoot: UV1 = 0.6V, CAP$_F$=0.01µF

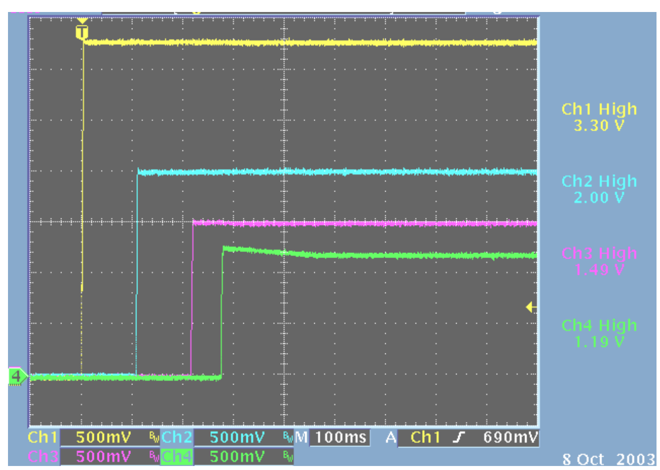

Figure 10: Last Sequence Position Overshoot: UV1 = 1.15V, CAP$_F$ = 0.01µF

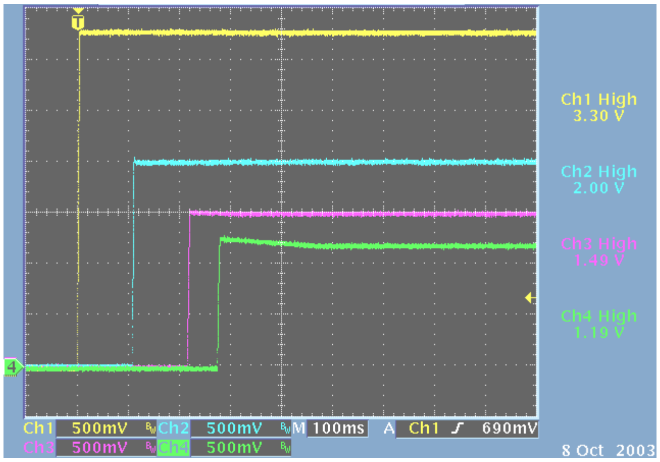

Figure 11: Last Sequence Position Overshoot: UV1 = 0.6V, CAP_F = 0.1µF

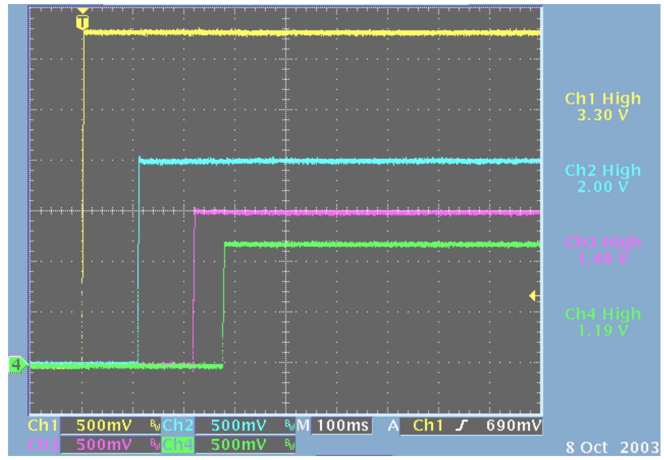

Figure 12: Last Sequence Position Overshoot: UV1 = 1.15V, CAP_F = 0.1µF

ADOC Accuracy and Transient Response

The ADOC/marginer's ability to set the output voltage of a converter accurately and maintain this accuracy when exposed to transient loads is shown in Figure 13. Here a converter is being managed by the ADOC/marginer immediately at turn-on setting the converter's output voltage to the preferred nominal voltage of 3.30V. In Figure 14, the same converter is turned on with the ADOC disengaged and as can be seen the output falls to a value of 3.23V due to the loading (green channel).

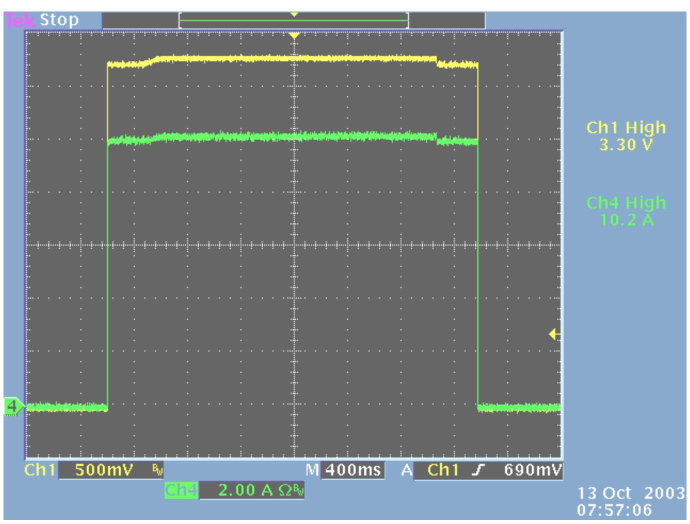

Figure 13: SMM665 controlling 10A DC/DC converter with ADOC engaged.
Vout set to 3.299V, reading 3.30V
< 0.2% accuracy error

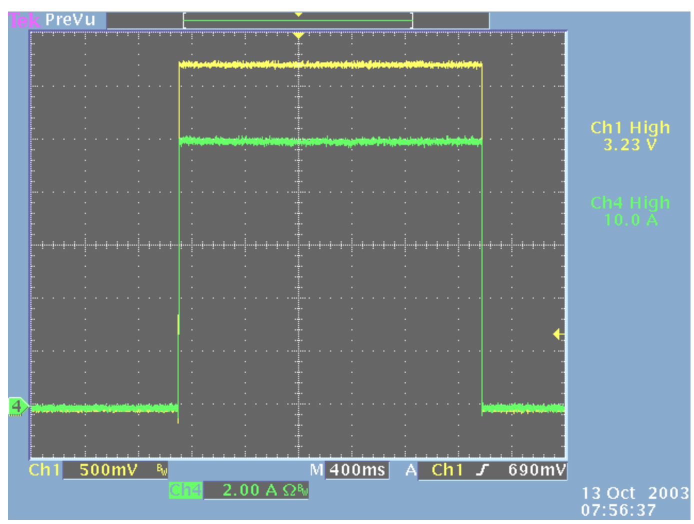

Figure 14: SMM665 controlling 10A DC/DC converter without ADOC engaged.
Vout set to 3.299V, reading 3.23V
> 2% accuracy error