

SMM605 SIX-CHANNEL SUPPLY MONITOR, CONTROLLER AND MARGINER Windows GUI Users Guide and Configuration Register Descriptions

Introduction

The information contained in Application Note 40 details the Configuration Register settings for the SMM605 six-channel supply monitor, controller and sequencer. The SMM605 Windows Graphical User Interface (GUI) is also shown with the associated register and function highlighted. For additional explanation on device functionality related to the configuration registers, refer to the SMM605 Data Sheet.

Register Formats and Functions

There are a total of 48 registers that are separated into four basic register types. The first are those that set a monitoring threshold where the binary value

written to the register is used to compute an incremental voltage. The second type enables or disables a function or selects between two specific functions. The third register type allows selection of various timing intervals or other values. These are not incremental, like the thresholds, but specific bit patterns select specific timer or other values. The fourth register type is a volatile status register that records device conditions. The device responds to two different slave addresses on the I²C bus. The general-purpose memory responds to slave address 1010_{BIN} or 1011_{BIN}; the configuration and software registers respond to slave address 1010_{BIN} or 1011_{BIN}.

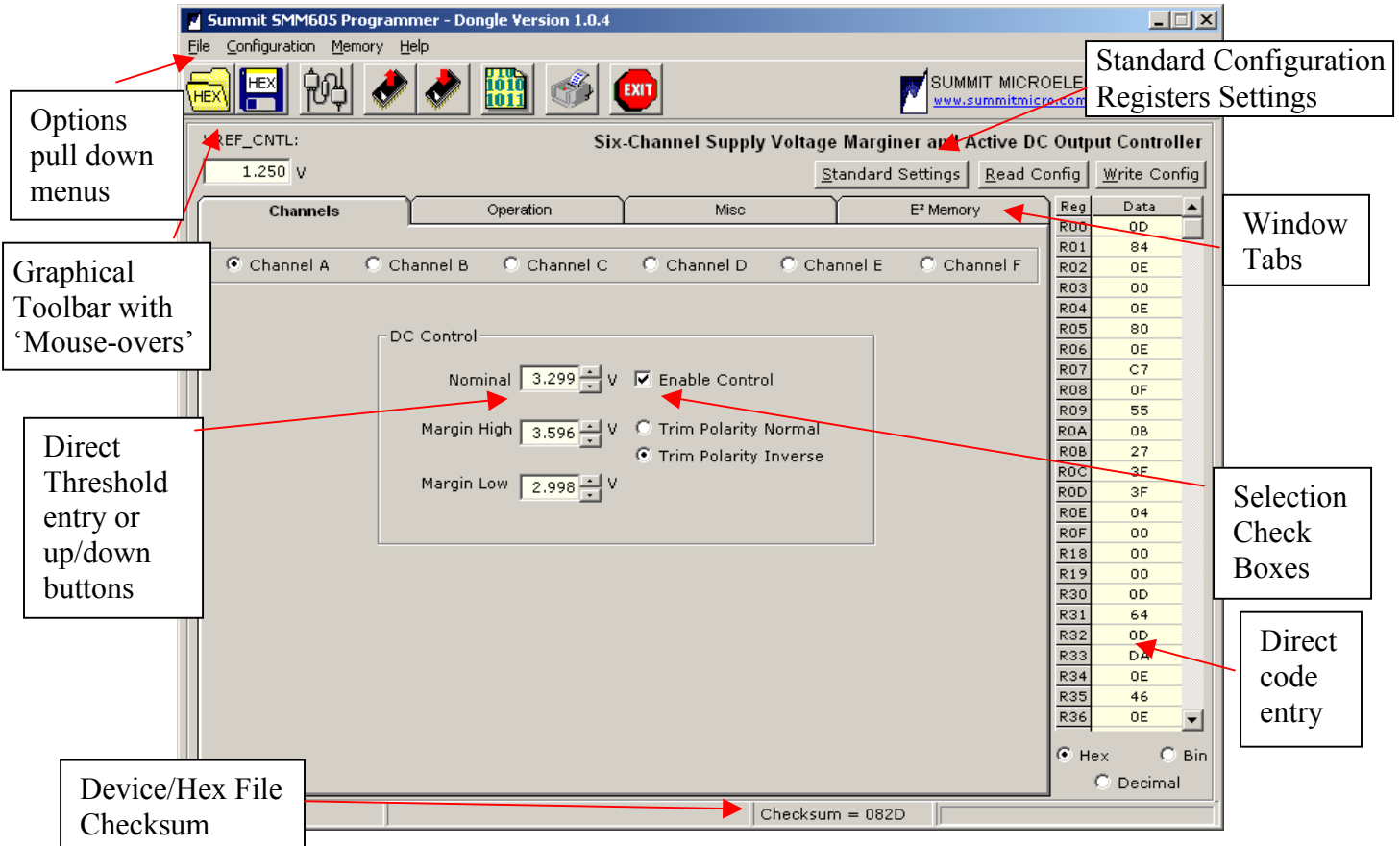


Figure 1 - SMM605 Windows GUI Features

SMM605 Windows Graphical User Interface

The SMM605 Windows GUI (Figure 1) is used with the SMX3200 programming 'Dongle'. It is an easy to use Graphical Interface that is compatible with Windows 95, 98, NT, 2000 and XP operating systems. The GUI consists of pull-down menus, check boxes,

up/down buttons, etc.. There are "mouse-overs" that define every function and an expert mode for directly entering data into the configuration registers. The GUI generates a checksum that can compare the programmed device configuration register values versus the hex contents.



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Help Menu

The Help menu can be used to view the SMM605 Datasheet or this app note while prototyping with the Windows GUI. The 'About' selection will show the GUI version number. Please always go to the Summit web site (www.summitmicro.com) to check for the most current data sheet and GUI software. There are also options if applicable, to View GUI change notices or to check the web site directly for the most current GUI version (Check Programmer Version).

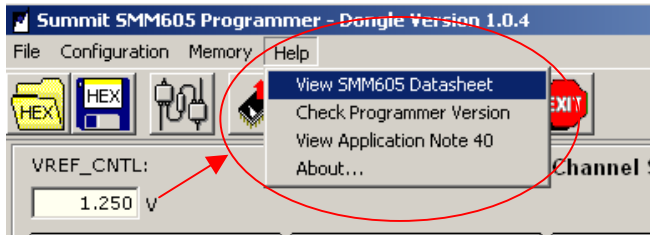


Figure 2 - Help Menu

Configuration Pull Down Menu

This menu (Figure 3A) has an option that will check for communications between the device and the PC. This selection should be tried first before changing any options. If the test passes, then all other options can be left in the default condition. If it doesn't pass, check all SMX3200 cable connections to the board and PC. If correct, then slow the I²C clock frequency as described in the Setup Options paragraph below.

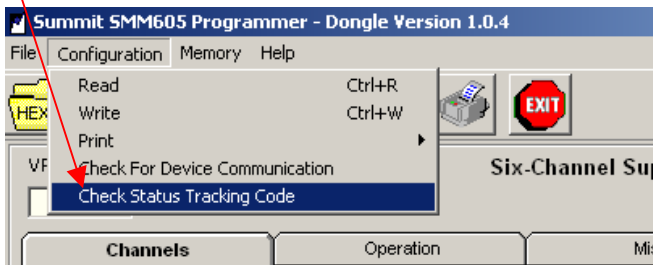


Figure 3A - Configuration Window

Setup Options

In the "File" pull-down menu (Figure 3B), there are options to set the I²C clock frequency and delays before I²C Read and Write operations. The default settings work with most PCs, so these settings are only for circumstances where the PC cannot communicate successfully with the SMX3200 programming 'Dongle'. The "Auto-Read Configuration/Memory After Write" check box enables a checksum test which compares the GUI hex settings or file to the programmed device at the end of a Write sequence. It does this by performing a Read immediately following a Write. Figure 4 shows the Settings Options Window which includes an additional control for the value of A2 in Configuration register R0E (see pages 7 and 9). There is also an option to keep the 'Dongle' supply active.

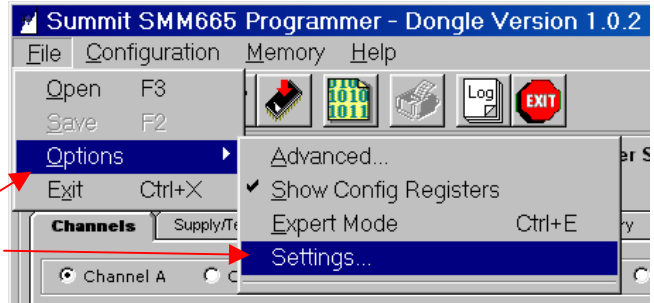


Figure 3B - Settings Window

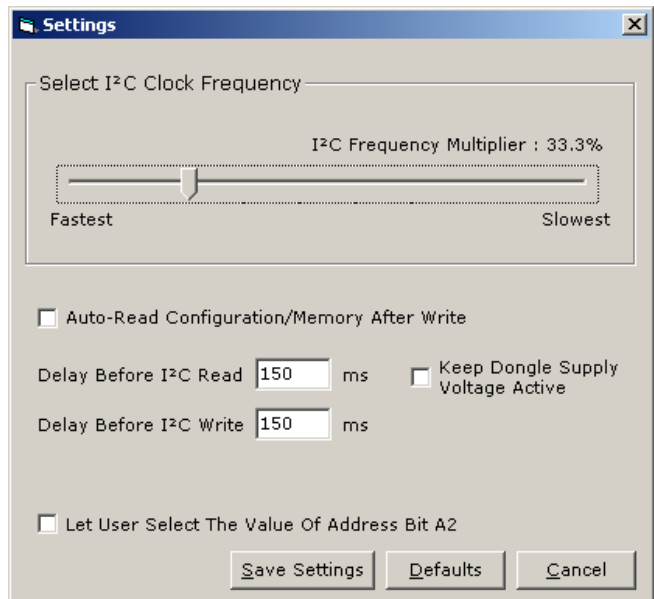


Figure 4 - Settings Options Window

Interfacing Options

The parallel Port Interfacing Window sets different options for programming the device. The 'Parallel Port Interfacing' should always be set to 'Dongle'. The 'Parallel Port Driver' can be changed for laptops if a problem is encountered in Win9X systems.

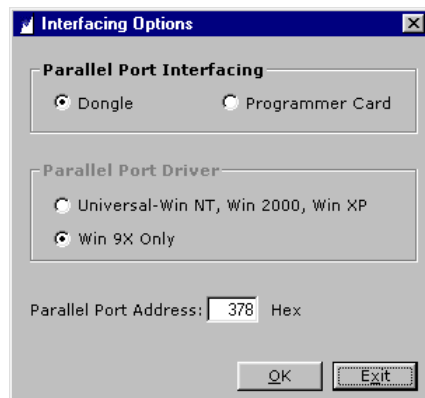


Figure 5 - Interfacing Options Window



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The following registers are located at slave address 101SA0_{BIN} SA0=R0E[3], bus address A2 11_{BIN} (A2 = 1_{BIN}) where A2 is either the A2 pin bias or 0 depending on the programmed selection. See register R0E, Fig 11.

Register R00, R02, R04, R06, R08, R0A, R30, R32, R34, R36, R38, R3A, R40, R42, R44, R46, R48, R4A - DC Control Nominal, Margin High and Margin Low Voltage Settings

These registers (R00 through R4A) are combined with registers R01 through R4B to set the 10-bit DC Control voltage. An explanation that shows the formula for setting the DC Control voltage follows the register descriptions.

Register R00, R02, R04, R06, R08, R0A, R30, R32, R34, R36, R38, R3A, R40, R42, R44, R46, R48, R4A								Action
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	1	1	X	X	DC Control Reference Voltage = VREF_CNTL voltage
X	X	X	X	1	0	X	X	DC Control Reference Voltage = 0.75*VREF_CNTL voltage
X	X	X	X	0	1	X	X	DC Control Reference Voltage = 0.50*VREF_CNTL voltage
X	X	X	X	0	0	X	X	DC Control Reference Voltage = 0.25*VREF_CNTL voltage
X	X	X	X	X	X	C9	C8	Bits [9:8] of 10-bit DC Control Setting (see table below)

Register R01, R03, R05, R07, R09, R0B, R31, R33, R35, R37, R39, R3B, R41, R43, R45, R47, R49, R4B - DC Control Nominal, Margin High and Margin Low Voltage Settings

These registers are combined with the previous set of registers to set the DC Control voltage.

Register R01, R03, R05, R07, R09, R0B, R31, R33, R35, R37, R39, R3B, R41, R43, R45, R47, R49, R4B								Action
D7	D6	D5	D4	D3	D2	D1	D0	
C7	C6	C5	C4	C3	C2	C1	C0	Bits [7:0] of 10-bit DC Control Setting

The DC Control Reference Voltage bits (D[3:2]) of registers (R00 through R4A) are set using the following table:

If:	Then = D[3:2]:
DC Control Nominal Voltage > VREF_CNTL	11
VREF_CNTL > DC Control Nominal Voltage > 0.80*VREF_CNTL	10
0.80*VREF_CNTL > DC Control Nominal Voltage > 0.55*VREF_CNTL	01
0.55*VREF_CNTL > DC Control Nominal Voltage > 0.30*VREF_CNTL	00

The DC Control Voltage setting bits (C[9:0]) are set using the following table:

If D[3:2] =:	Then C[9:0] =:
11	$1024 * VREF_CNTL / DC\ Control\ Voltage$
10	$1024 * 0.75 * VREF_CNTL / DC\ Control\ Voltage$
01	$1024 * 0.50 * VREF_CNTL / DC\ Control\ Voltage$
00	$1024 * 0.25 * VREF_CNTL / DC\ Control\ Voltage$
*For higher accuracy see registers R2A-R2F	



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The following table lists the registers with their corresponding Channel and DC Control Mode:

Registers	DC Control Setting	Registers	DC Control Setting	Registers	DC Control Setting
R00:R01	Ch A – Nominal	R30:R31	Ch A – Margin High	R40:R41	Ch A – Margin Low
R02:R03	Ch B – Nominal	R32:R33	Ch B – Margin High	R42:R43	Ch B – Margin Low
R04:R05	Ch C – Nominal	R34:R35	Ch C – Margin High	R44:R45	Ch C – Margin Low
R06:R07	Ch D – Nominal	R36:R37	Ch D – Margin High	R46:R47	Ch D – Margin Low
R08:R09	Ch E – Nominal	R38:R39	Ch E – Margin High	R48:R49	Ch E – Margin Low
R0A:R0B	Ch F – Nominal	R3A:R3B	Ch F – Margin High	R4A:R4B	Ch F – Margin Low

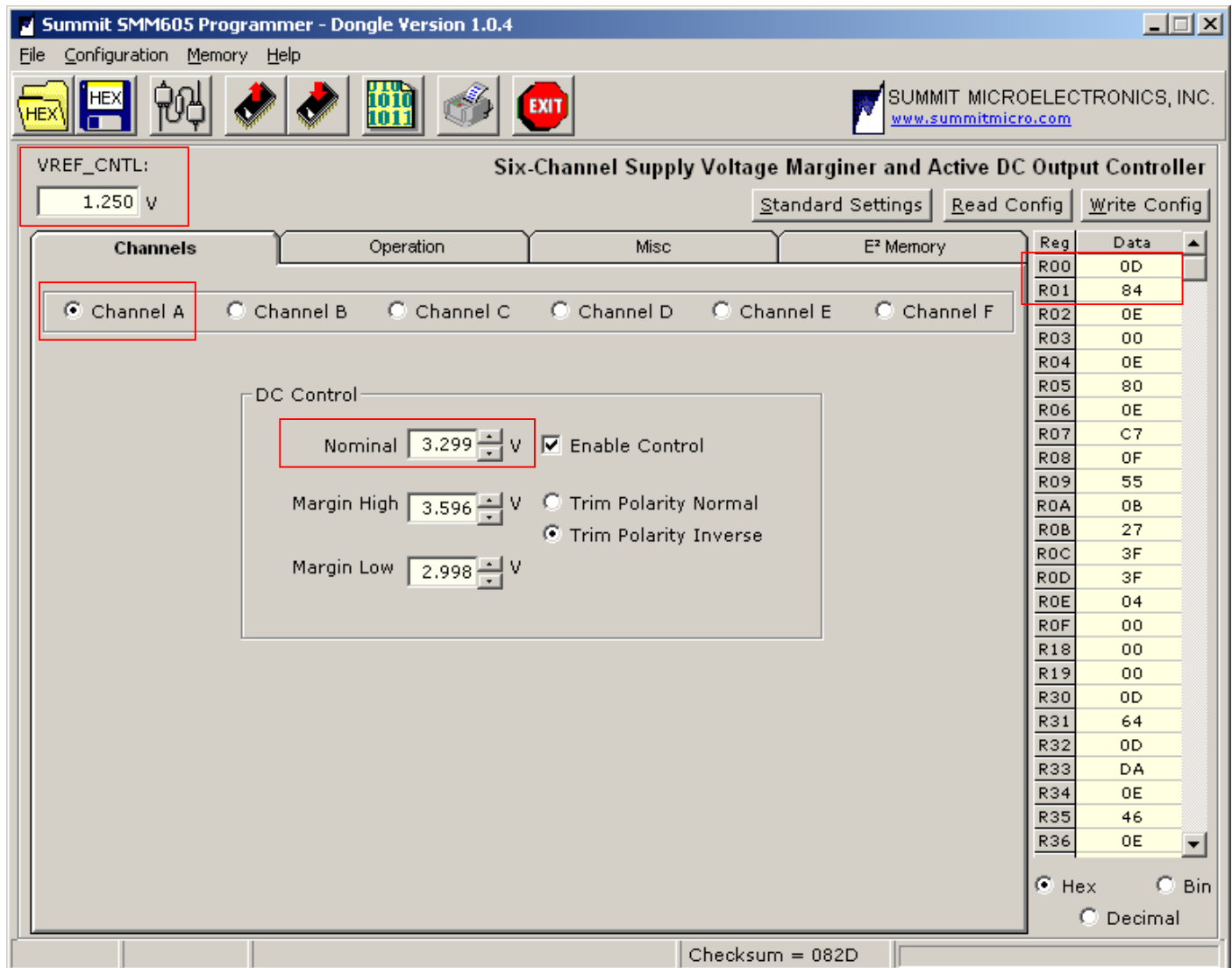


Figure 6 - Register R00, R01 Windows GUI Tab for Channel A and VREF_CNTL.



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Register R0C - Internal Regulator Output, Fast Convergence, TRIMX Pin Polarity

Bit D[7] of this register selects the output voltage of the internal regulator powered by 12VIN. This voltage will power the SMM605 if the voltage on the VDD pin is lower than this setting. Bit D[6] enables fast convergence to decrease the time it takes to change between nominal, margin high and margin low voltages. This remaining bits of this register individually selects the polarity of the TRIMX pins for use with different types of converters.

Register R0C								
D7	D6	D5	D4	D3	D2	D1	D0	Action
1	X	X	X	X	X	X	X	12VIN regulator output set to 5.5V
0	X	X	X	X	X	X	X	12VIN regulator output set to 3.6V
X	1	X	X	X	X	X	X	Enable Fast Convergence of DC Control
X	0	X	X	X	X	X	X	Disable Fast Convergence of DC Control
X	X	1	X	X	X	X	X	Channel F TRIMF pin polarity inverse
X	X	0	X	X	X	X	X	Channel F TRIMF pin polarity normal
X	X	X	1	X	X	X	X	Channel E TRIME pin polarity inverse
X	X	X	0	X	X	X	X	Channel E TRIME pin polarity normal
X	X	X	X	1	X	X	X	Channel D TRIMD pin polarity inverse
X	X	X	X	0	X	X	X	Channel D TRIMD pin polarity normal
X	X	X	X	X	1	X	X	Channel C TRIMC pin polarity inverse
X	X	X	X	X	0	X	X	Channel C TRIMC pin polarity normal
X	X	X	X	X	X	1	X	Channel B TRIMB pin polarity inverse
X	X	X	X	X	X	0	X	Channel B TRIMB pin polarity normal
X	X	X	X	X	X	X	1	Channel A TRIMA pin polarity inverse
X	X	X	X	X	X	X	0	Channel A TRIMA pin polarity normal



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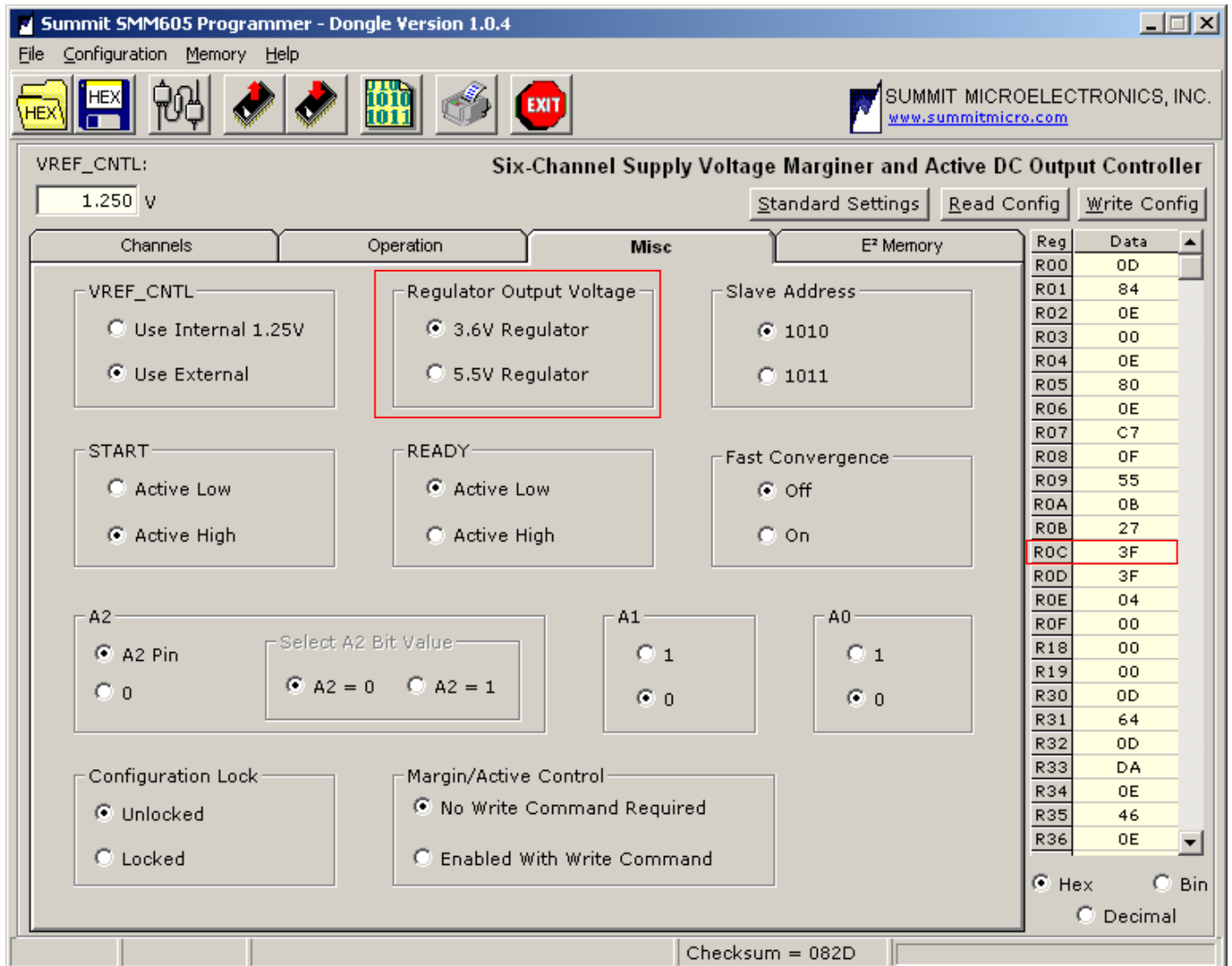


Figure 7 - Register R0C MISC Windows GUI Tab

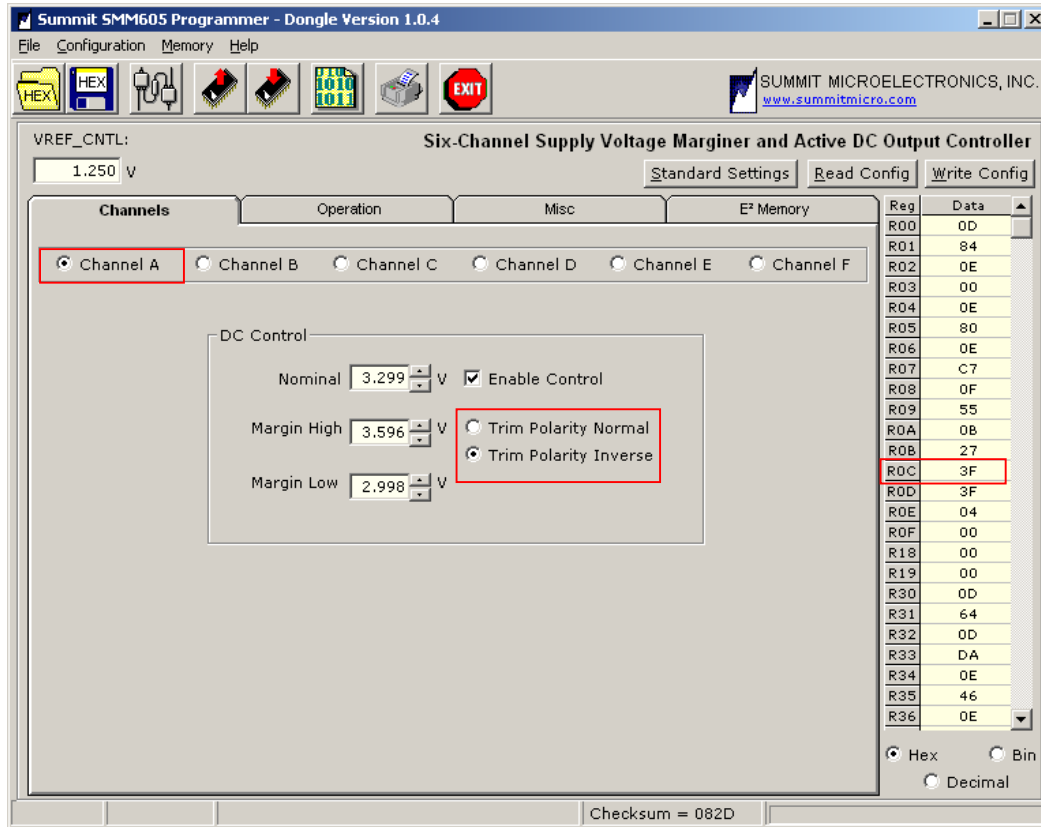


Figure 8 - Register R0C Windows GUI Tab

Register R0D – Configuration Register Lock, DC Control Enables

Bit D[7] of this register allows the configuration registers to be locked. Locking the configuration registers is irreversible and therefore this option cannot be selected using the GUI. This register also enables DC Control of each channel. The channel must be enabled for any DC Control (Nominal, Margin High, Margin Low).

Register R0D								Action
D7	D6	D5	D4	D3	D2	D1	D0	
1	X	X	X	X	X	X	X	Configuration registers locked (writes disabled)
0	X	X	X	X	X	X	X	Configuration registers unlocked (writes enabled)
X	X	1	X	X	X	X	X	Channel F DC Control enabled
X	X	0	X	X	X	X	X	Channel F DC Control disabled
X	X	X	1	X	X	X	X	Channel E DC Control enabled
X	X	X	0	X	X	X	X	Channel E DC Control disabled
X	X	X	X	1	X	X	X	Channel D DC Control enabled
X	X	X	X	0	X	X	X	Channel D DC Control disabled
X	X	X	X	X	1	X	X	Channel C DC Control enabled
X	X	X	X	X	0	X	X	Channel C DC Control disabled
X	X	X	X	X	X	1	X	Channel B DC Control enabled
X	X	X	X	X	X	0	X	Channel B DC Control disabled
X	X	X	X	X	X	X	1	Channel A DC Control enabled
X	X	X	X	X	X	X	0	Channel A DC Control disabled



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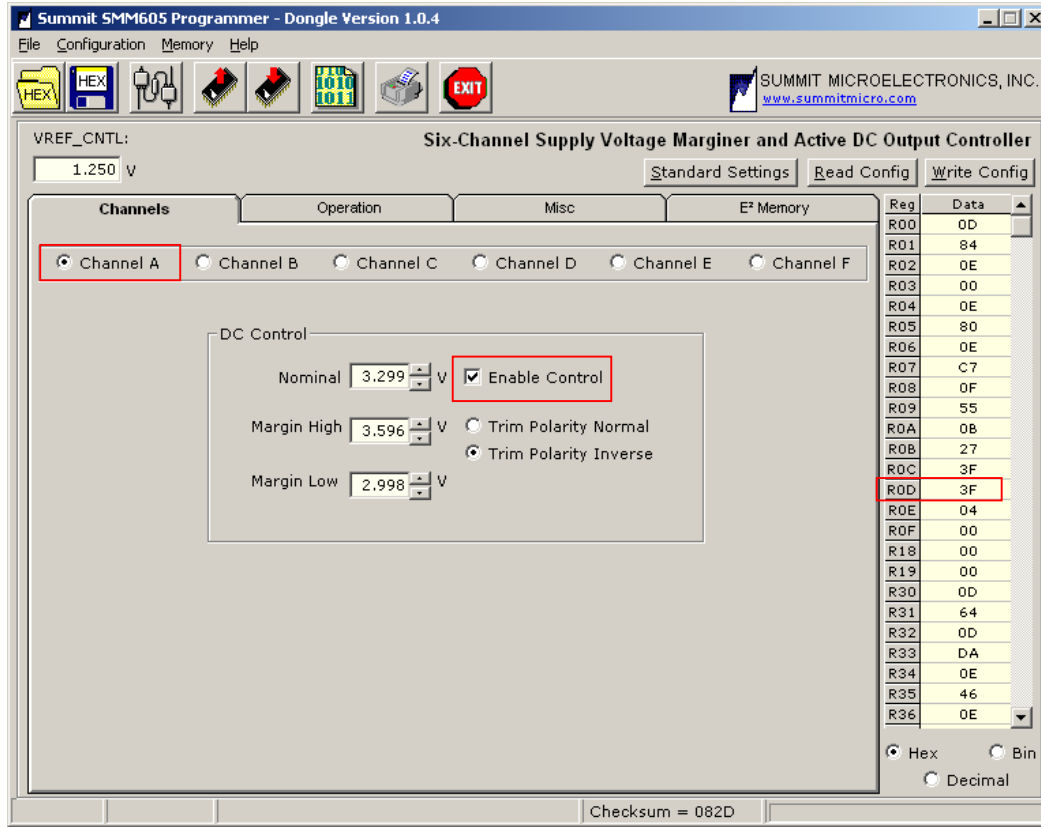


Figure 9 - Register R0D Windows GUI Tab

Register R0E –Slave Address, Bus Address Bits

The slave address [1011b and 1010b] of the SMM605 is set by bit D[3]. The bus address [A2 A1 A0] of the SMM605 is set by bits D[2:0] of this register.

Register R0E								Action
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	1	X	X	X	Slave Address = 1011BIN
X	X	X	X	0	X	X	X	Slave Address = 1010BIN
X	X	X	X	X	1	X	X	Bus Address Bit A2 = A2 Pin
X	X	X	X	X	0	X	X	Bus Address Bit A2 = 0
X	X	X	X	X	X	1	X	Bus Address Bit A1 = 1
X	X	X	X	X	X	0	X	Bus Address Bit A1 = 0
X	X	X	X	X	X	X	1	Bus Address Bit A0 = 1
X	X	X	X	X	X	X	0	Bus Address Bit A0 = 0



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The screenshot shows the Summit SMM605 Programmer software interface. The title bar reads "Summit SMM605 Programmer - Dongle Version 1.0.4". The menu bar includes "File", "Configuration", "Memory", and "Help". The toolbar contains icons for HEX files, configuration, and an EXIT button. The main window title is "Six-Channel Supply Voltage Marginer and Active DC Output Controller".

The "VREF_CNTL:" field is set to "1.250 V". The "Standard Settings", "Read Config", and "Write Config" buttons are visible. The "Misc" tab is selected, showing various configuration options:

- VREF_CNTL:** Use Internal 1.25V, Use External
- Regulator Output Voltage:** 3.6V Regulator, 5.5V Regulator
- Slave Address:** 1010, 1011
- START:** Active Low, Active High
- READY:** Active Low, Active High
- Fast Convergence:** Off, On
- A2:** A2 Pin, 0. **Select A2 Bit Value:** A2 = 0, A2 = 1
- A1:** 1, 0
- A0:** 1, 0
- Configuration Lock:** Unlocked, Locked
- Margin/Active Control:** No Write Command Required, Enabled With Write Command

The "E² Memory" table on the right shows the following data:

Reg	Data
R00	0D
R01	84
R02	0E
R03	00
R04	0E
R05	80
R06	0E
R07	C7
R08	0F
R09	55
R0A	0B
R0B	27
R0C	3F
R0D	3F
R0E	04
R0F	00
R18	00
R19	00
R30	0D
R31	64
R32	0D
R33	DA
R34	0E
R35	46
R36	0E

The "Checksum = 082D" is displayed at the bottom. The output format is set to "Hex".

Figure 10 - Register R0E MISC Windows GUI Tab



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Summit SMM605 Programmer - Dongle Version 1.0.4

File Configuration Memory Help

HEX HEX [Icons] SUMMIT MICROELECTRONICS, INC. www.summitmicro.com

VREF_CNTL: 1.250 V [Standard Settings] [Read Config] [Write Config]

Six-Channel Supply Voltage Marginer and Active DC Output Controller

Channels Operation Misc E² Memory

VREF_CNTL: Use Internal 1.25V Use External

Regulator Output Voltage: 3.6V Regulator 5.5V Regulator

Slave Address: 1010 1011

START: Active Low Active High

READY: Active Low Active High

Fast Convergence: Off On

A2: A2 Pin 0

Select A2 Bit Value: A2 = 0 A2 = 1

A1: 1 0

A0: 1 0

Configuration Lock: Unlocked Locked

Margin/Active Control: No Write Command Required Enabled With Write Command

Reg	Data
R00	0D
R01	84
R02	0E
R03	00
R04	0E
R05	80
R06	0E
R07	C7
R08	0F
R09	55
R0A	0B
R0B	27
R0C	3F
R0D	3F
R0E	04
R0F	00
R18	00
R19	00
R30	0D
R31	64
R32	0D
R33	DA
R34	0E
R35	46
R36	0E

Hex Bin Decimal

Checksum = 082D

Figure 11 - Register R0E Miscellaneous GUI Tab



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Register R0F – DC Control Reference Voltage, DC Control Command, Automonitor Actions Enable, Power-Off Order, Force Shutdown Restart, Power-Off Sequence Termination, Preconditions for Power-On

Bit D[7] of this register selects the internal or external reference for the VREF_CNTL pin. The Power-Off order is selected with bit D[4]. The action taken to restart the SMM605 after a Force Shutdown is selected with bit D[3]. Bit D[2] will disable the Sequence Termination Timer during a Power-Off sequence. Bits D[1:0] enable precursors to the Power-On operation.

Register R0F								Action
D7	D6	D5	D4	D3	D2	D1	D0	
1	X	X	X	X	X	X	X	DC Control Reference Voltage from internal 1.25V reference connected to VREF_CNTL
0	X	X	X	X	X	X	X	DC Control Reference Voltage provided externally
X	1	X	X	X	X	X	X	DC Control command required for Active Control
X	0	X	X	X	X	X	X	No DC Control command required for Active Control
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	
X	X	X	X	X	X	X	X	



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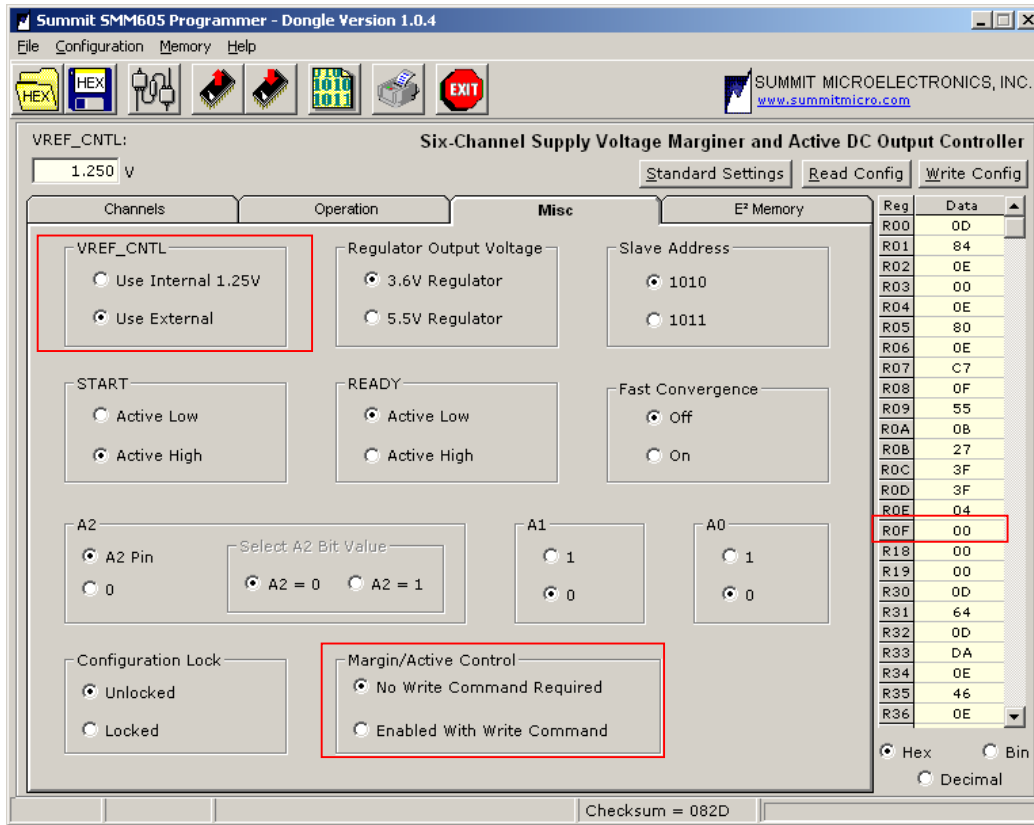


Figure 12 - Register R0F Windows GUI Tab

Register R18, R1A, R1C, R1E – DC Control Commands for Channels A, B and C

Writing to any of these registers constitutes a DC Control Command. This command initiates control of Channels A, B and C to the desired DC Control Mode voltage.

Register R18, R1A, R1C, R1E								Action
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	1	1	X	X	X	X	Channel A DC Control Margin High
X	X	1	0	X	X	X	X	Channel A DC Control Margin Low
X	X	0	X	X	X	X	X	Channel A DC Control Nominal
X	X	X	X	1	1	X	X	Channel B DC Control Margin High
X	X	X	X	1	0	X	X	Channel B DC Control Margin Low
X	X	X	X	0	X	X	X	Channel B DC Control Nominal
X	X	X	X	X	X	1	1	Channel C DC Control Margin High
X	X	X	X	X	X	1	0	Channel C DC Control Margin Low
X	X	X	X	X	X	0	X	Channel C DC Control Nominal

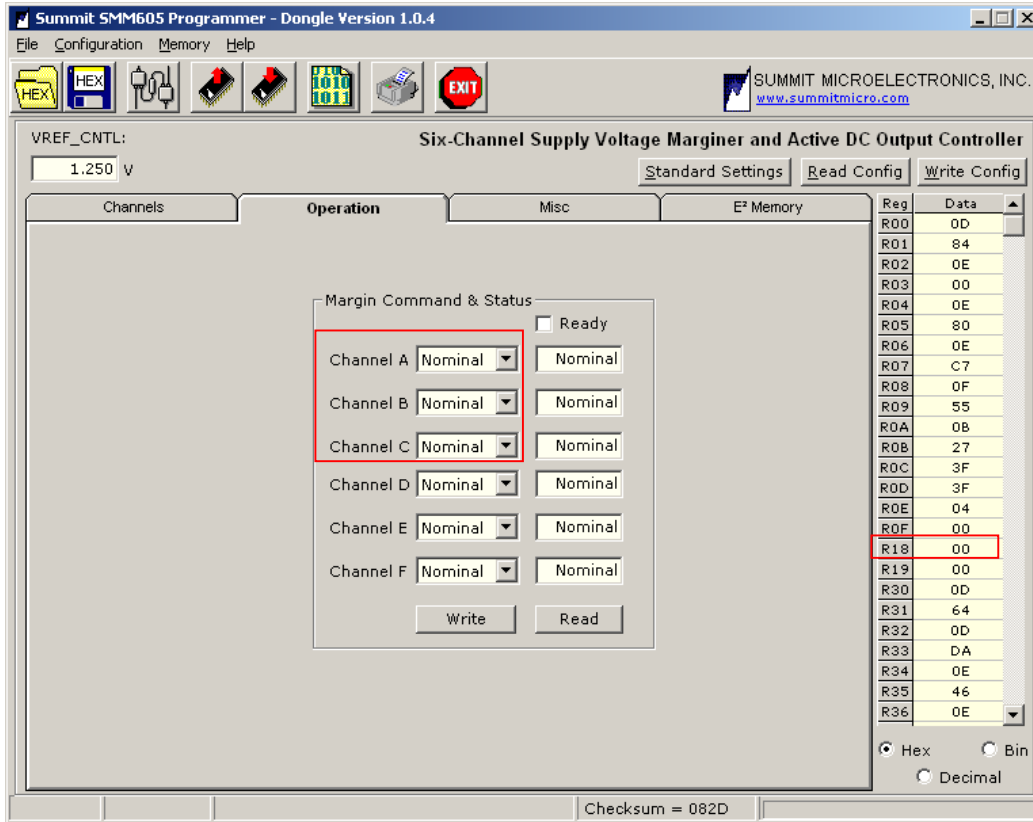


Figure 13 - Register R18 Operation Windows GUI Tab

Register R19, R1B, R1D, R1F – DC Control Commands for Channels D, E and F

Writing to any of these registers constitutes a DC Control Command. This command initiates control of Channels D, E and F to the desired DC Control Mode voltage.

Register R19, R1B, R1D, R1F								Action
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	1	1	X	X	X	X	Channel D DC Control Margin High
X	X	1	0	X	X	X	X	Channel D DC Control Margin Low
X	X	0	X	X	X	X	X	Channel D DC Control Nominal
X	X	X	X	1	1	X	X	Channel E DC Control Margin High
X	X	X	X	1	0	X	X	Channel E DC Control Margin Low
X	X	X	X	0	X	X	X	Channel E DC Control Nominal
X	X	X	X	X	X	1	1	Channel F DC Control Margin High
X	X	X	X	X	X	1	0	Channel F DC Control Margin Low
X	X	X	X	X	X	0	X	Channel F DC Control Nominal

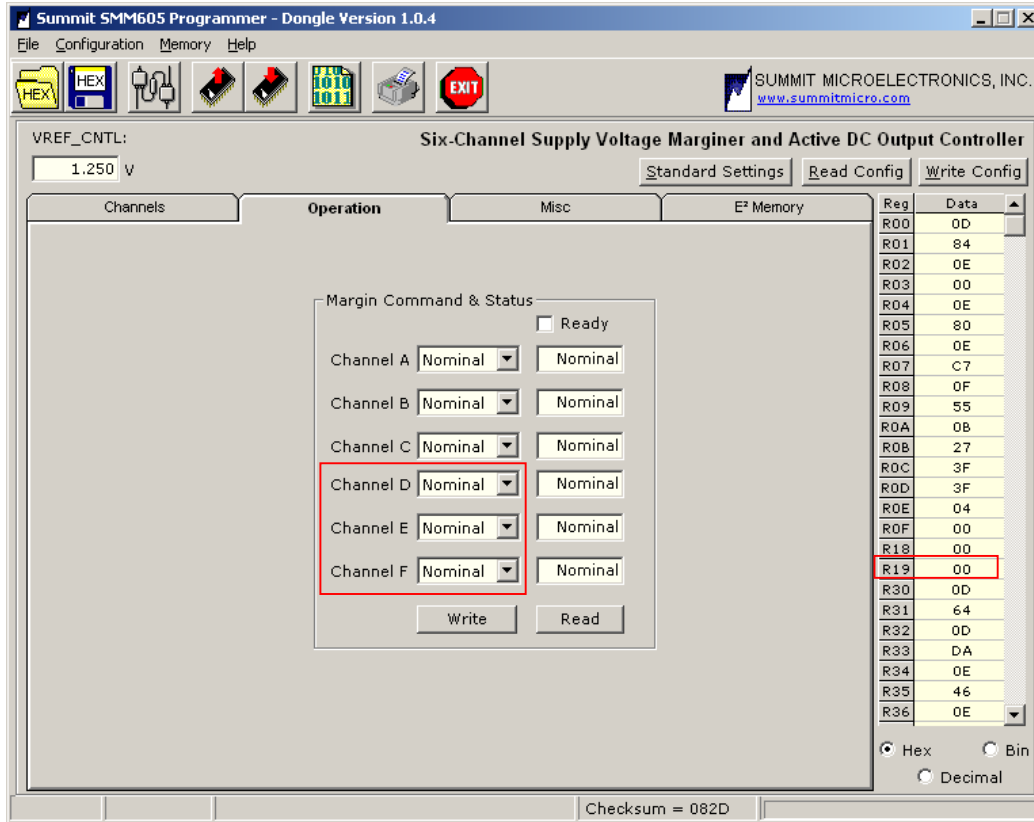


Figure 14 - Register R19 Operation Windows GUI Tab

Register R2A, R2C, R2E - Error Coefficients (READ ONLY)

These registers are combined with the next set of registers to store information used to decrease error when setting the DC Control Reference Voltage bits to 00_{BIN} , 01_{BIN} or 10_{BIN} . R2A corresponds with the DC Control Reference Voltage bits set to 10_{BIN} ; R2C corresponds with the DC Control Reference Voltage bits set to 01_{BIN} ; and R2E corresponds with the DC Control Reference Voltage bits set to 00_{BIN} .

Register R2A, R2C, R2E								Action
D7	D6	D5	D4	D3	D2	D1	D0	
1	X	X	X	X	X	X	X	Negative Error
0	X	X	X	X	X	X	X	Positive Error
X	1	1	1	X	X	X	X	Percentage Point = 7 (111_{BIN})
X	0	0	0	X	X	X	X	Percentage Point = 0 (000_{BIN})
X	X	X	X	1	0	0	1	Tenth of Percentage Point = 9 (1001_{BIN})
X	X	X	X	0	0	0	0	Tenth of Percentage Point = 0 (0000_{BIN})



Application Note 40

Register R2B, R2D, R2F - Error Coefficients (READ ONLY)

These registers are combined with the previous set of registers to store information used to decrease error when setting the DC Control Reference Voltage bits to 00_{BIN}, 01_{BIN} or 10_{BIN}. R2B corresponds with the DC Control Reference Voltage bits set to 10_{BIN}; R2D corresponds with the DC Control Reference Voltage bits set to 01_{BIN}; and R2F corresponds with the DC Control Reference Voltage bits set to 00_{BIN}.

Register R2B, R2D, R2F								Action
D7	D6	D5	D4	D3	D2	D1	D0	
1	0	0	1	X	X	X	X	Hundredth of Percentage Point = 9 (1001 _{BIN})
0	0	0	0	X	X	X	X	Hundredth of Percentage Point = 0 (0000 _{BIN})
X	X	X	X	1	0	0	1	Thousandth of Percentage Point = 9 (1001 _{BIN})
X	X	X	X	0	0	0	0	Thousandth of Percentage Point = 0 (0000 _{BIN})

Example: R2A[7:0] = 1010 0101_{BIN} and R2B[7:0] = 0001 1000_{BIN} converts to: R2A:R2B = -2.518%

The following table is used to calculate the VREF_CNTL used in registers R00-R0B, R30-R3B and R40-R4B:

If DC Control Reference Voltage bits =:	Then VREF_CNTL _{ACCURATE} =:
10	VREF_CNTL * (1 + R2A:R2B)
01	VREF_CNTL * (1 + R2C:R2D)
00	VREF_CNTL * (1 + R2E:R2F)



Application Note 40

Register R83 – Input and Output Pin Polarities (Registers 83, 85, 86, 87 are at slave address 1001 A2 A1 A0)

This register sets the polarity of the HEALTHY, FAULT and RST outputs and the MR, PWR_ON/OFF and FS inputs.

Register R83								
D7	D6	D5	D4	D3	D2	D1	D0	Action
0	0	X	X	X	X	X	X	Set these bits to 0's
X	X	1	X	X	X	X	X	READY Active High
X	X	0	X	X	X	X	X	READY Active Low
X	X	X	1	X	X	X	X	
X	X	X	0	X	0	X	X	
X	X	X	X	1	X	X	X	
X	X	X	X	0	X	X	X	
X	X	X	X	X	1	X	X	START Active High
X	X	X	X	X	0	X	X	START Active Low
X	X	X	X	X	X	1	X	
X	X	X	X	X	X	0	X	
X	X	X	X	X	X	X	1	
X	X	X	X	X	X	X	0	

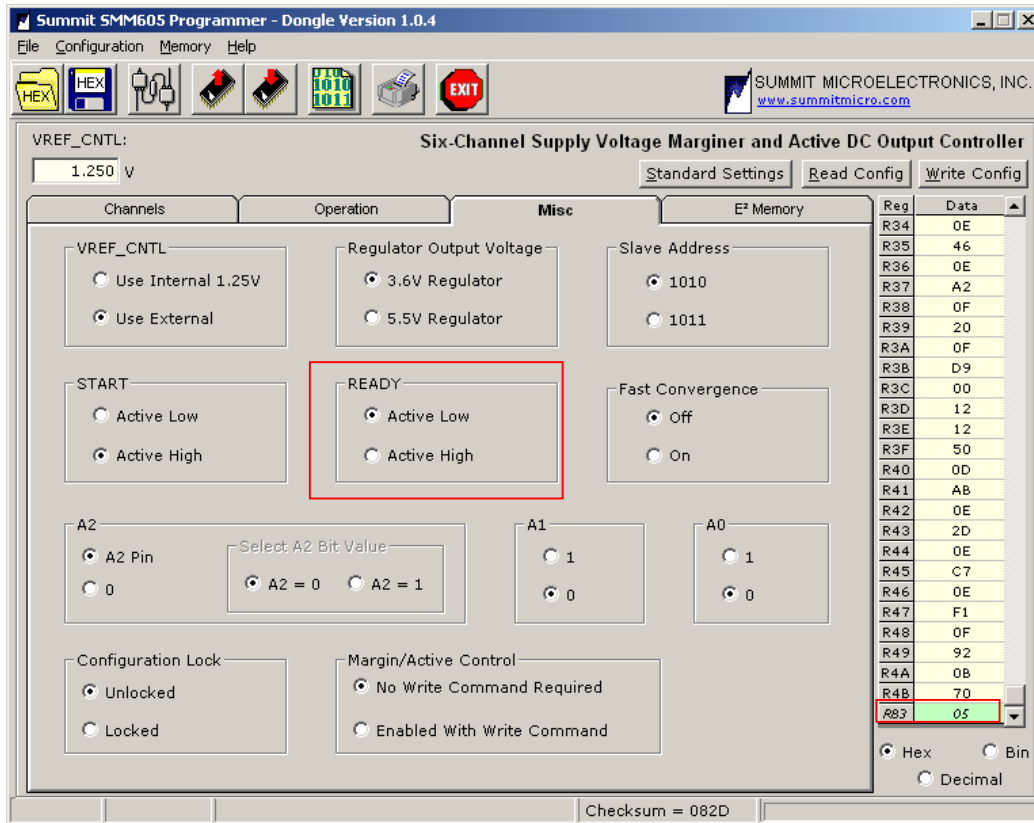


Figure 15 - Register R83 Windows GUI Tab



Application Note 40

Register R85 - DC Control Mode Status Register (Volatile, Read-Only)

This volatile, read-only register shows the mode of DC Control for Channels A, B and C. Bit D[7] of this register is set when all channels are at the desired DC Control voltage.

Register R85								
D7	D6	D5	D4	D3	D2	D1	D0	Action
1	X	X	X	X	X	X	X	DC Control is Ready (Channels at set point)
0	X	X	X	X	X	X	X	DC Control is not Ready
X	X	1	1	X	X	X	X	Channel A DC Control Mode is Margin High
X	X	1	0	X	X	X	X	Channel A DC Control Mode is Margin Low
X	X	0	X	X	X	X	X	Channel A DC Control Mode is Nominal
X	X	X	X	1	1	X	X	Channel B DC Control Mode is Margin High
X	X	X	X	1	0	X	X	Channel B DC Control Mode is Margin Low
X	X	X	X	0	X	X	X	Channel B DC Control Mode is Nominal
X	X	X	X	X	X	1	1	Channel C DC Control Mode is Margin High
X	X	X	X	X	X	1	0	Channel C DC Control Mode is Margin Low
X	X	X	X	X	X	0	X	Channel C DC Control Mode is Nominal

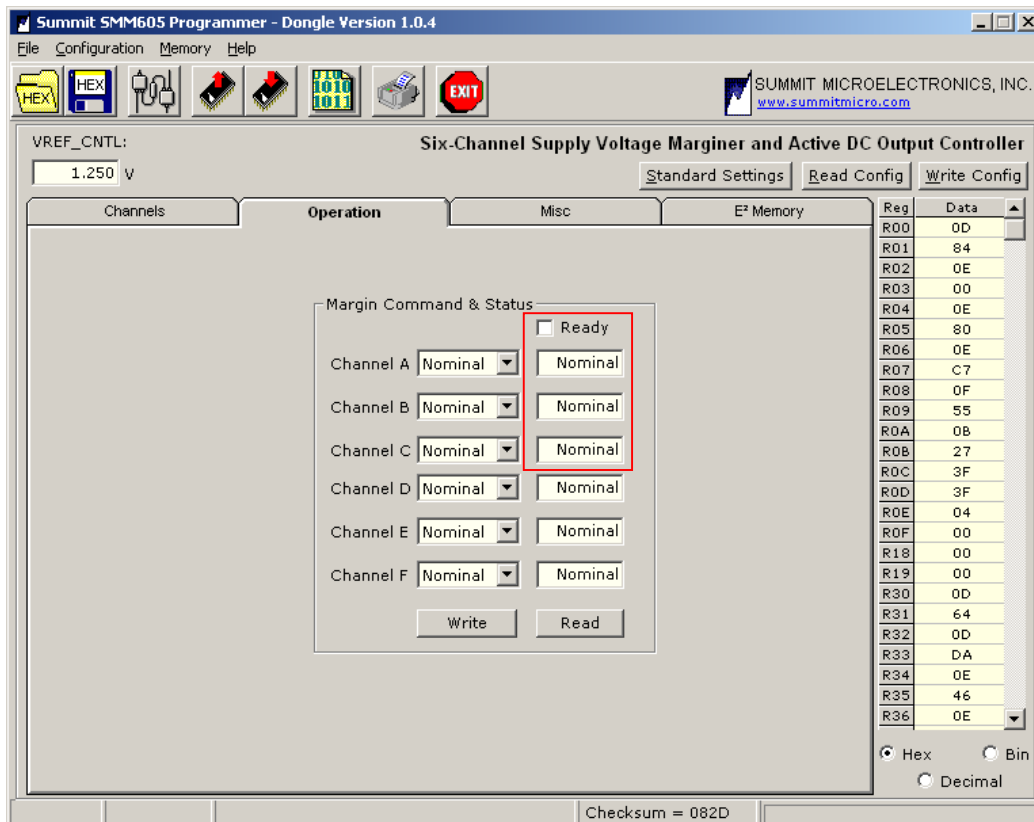


Figure 16 - Register R85 Windows GUI Tab



Application Note 40

Register R86 - DC Control Mode Status Register (Volatile, Read-Only)

This volatile, read-only register shows the mode of DC Control for Channels D, E and F. Bit D[7] of this register is set when all channels are at the desired DC Control voltage.

Register R86								Action
D7	D6	D5	D4	D3	D2	D1	D0	
1	X	X	X	X	X	X	X	DC Control is Ready (Channels at set point)
0	X	X	X	X	X	X	X	DC Control is not Ready
X	X	1	1	X	X	X	X	Channel D DC Control Mode is Margin High
X	X	1	0	X	X	X	X	Channel D DC Control Mode is Margin Low
X	X	0	X	X	X	X	X	Channel D DC Control Mode is Nominal
X	X	X	X	1	1	X	X	Channel E DC Control Mode is Margin High
X	X	X	X	1	0	X	X	Channel E DC Control Mode is Margin Low
X	X	X	X	0	X	X	X	Channel E DC Control Mode is Nominal
X	X	X	X	X	X	1	1	Channel F DC Control Mode is Margin High
X	X	X	X	X	X	1	0	Channel F DC Control Mode is Margin Low
X	X	X	X	X	X	0	X	Channel F DC Control Mode is Nominal

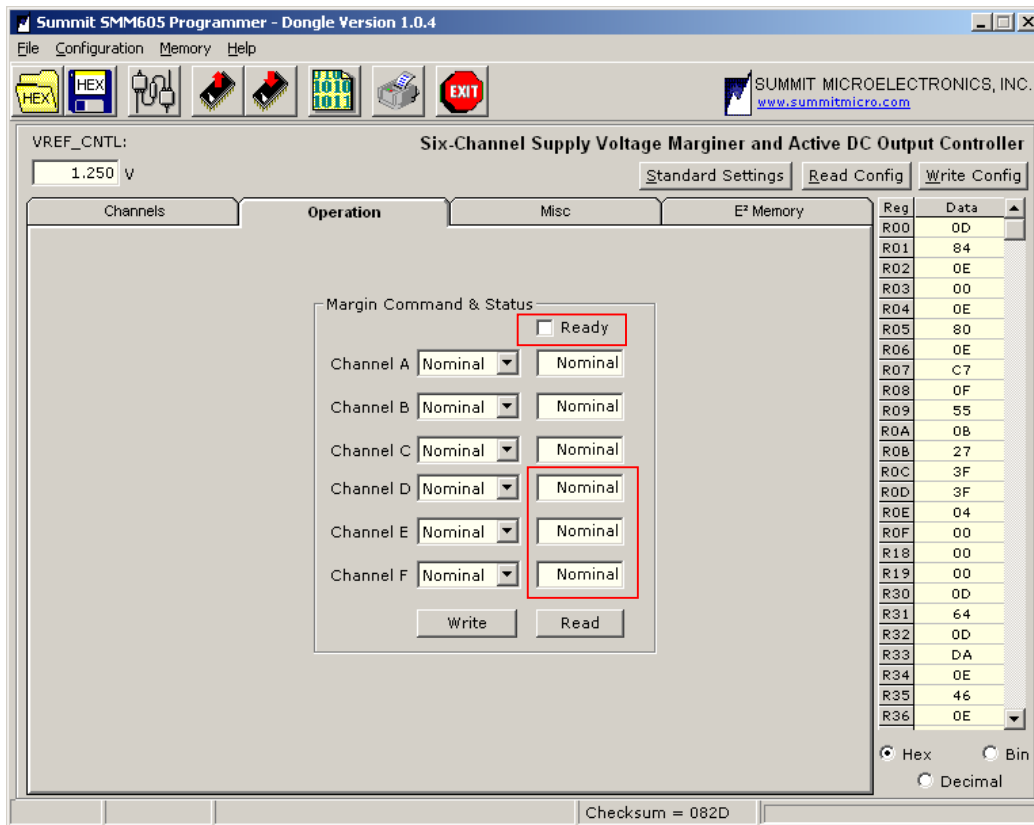


Figure 17 - Register R86 Windows GUI Tab



Application Note 40

Register R87 - Write Protection Register (Write-Only)

This volatile, write-only register disables write protection to the memory and configuration registers. This register powers up into a write protected state. Before a write operation is allowed, the code 0101_{BIN} must be written to this registers memory or configuration bits. The register must then be written with other data (----BIN) to write protect the memory or configuration.

Register R86								
D7	D6	D5	D4	D3	D2	D1	D0	Action
0	1	0	1	X	X	X	X	Memory Write Protection Disabled
-	-	-	-	X	X	X	X	Memory Write Protection Enabled
X	X	X	X	0	1	0	1	Configuration Write Protection Disabled
X	X	X	X	-	-	-	-	Configuration Write Protection Enabled

Register R88 - STATUS TRACKING CODE Identification

Register data bits D[1:0] are read-only bits that identify the “STATUS TRACKING CODE” of the SMM605. The command to do this is available in the Configuration pull down menu. The Status Tracking Code will appear in the bottom right side corner of the GUI window. The Status Code will also appear whenever a “Read Config” command is performed with an SMM605 device connected to the target PC.

Register R88								
D7	D6	D5	D4	D3	D2	D1	D0	Action
X	X	X	X	X	X	0	1	Status Tracking Code 01
X	X	X	X	X	X	1	0	Status Tracking Code 02
X	X	X	X	X	X	1	1	Status Tracking Code 03
0	0	1	0	0	1	0	1	Status Tracking Code 08

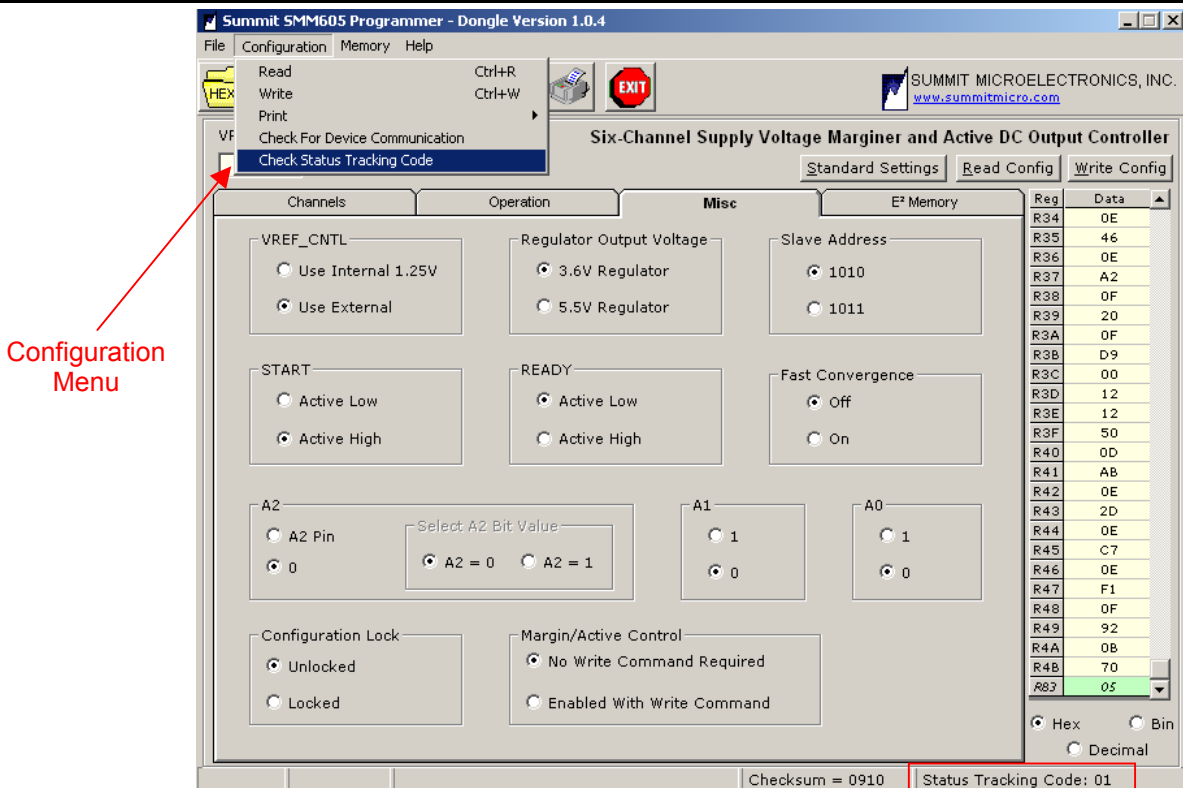


Figure 18 - Register R88 Windows GUI Tab



4k Nonvolatile Memory Array

The memory array can be updated by writing data directly into the memory location. To write into a specific location, go to the Hex column location in the Tabular view and press the 'Backspace' key. Type in the new data and then press the 'Enter' key.

A graphic view of the memory can also be displayed for test purposes to check that the entire memory contents has changed or by writing pages or bytes, etc. using the buttons in the Graphic View Memory window.

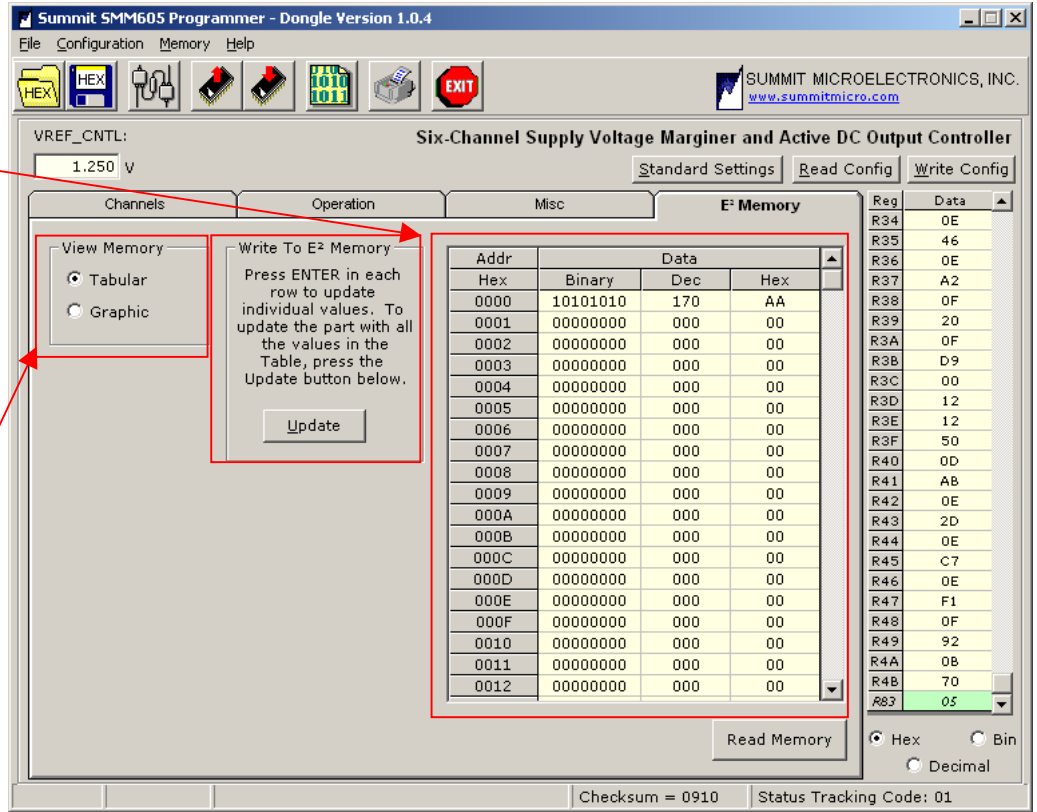


Figure 19 – E² Memory Array Windows GUI



SMM605 Register Map

The following registers are accessed using slave address 101 SA0 A2 1 1 (SA0 = R0E[3])

R00	[7:4] Unused [3:2] Channel A Margin Nominal Vref Bits [1:0] [0:1] Channel A Nominal Voltage Bits [9:8]	R0D	[7] Configuration Lock [6] Unused [5] Channel F Enable Control [4] Channel E Enable Control [3] Channel D Enable Control [2] Channel C Enable Control [1] Channel B Enable Control [0] Channel A Enable Control
R01	[0:7] Channel A Nominal Voltage Bits [7:0]	R0E	[7:6] Sequence Termination Timeout Period [5:4] Reset Timeout Period [3] Slave Address Select [2] A2 Address Bit [1] A1 Address Bit [0] A0 Address Bit
R02	[7:4] Unused [3:2] Channel B Margin Nominal Vref Bits [1:0] [0:1] Channel B Nominal Voltage Bits [9:8]	R0F	[7] VREF_CNTL [6] Write Command For Margin/Active Ctrl Enabling [5:0] Unused [5] Limit Triggers Enabled After [4] Power-Off Sequencing [3] Restart (After a Force Shutdown) [2] Seq. Termination Timer During Power-Off [1] Wait For 12VIN Within Limits Before Power On [0] Wait For VDD Within Limits Before Power On
R03	[0:7] Channel B Nominal Voltage [7:0]	R10 to R17	Unused
R04	[7:4] Unused [3:2] Channel C Margin Nominal Vref Bits [1:0] [0:1] Channel C Nominal Voltage Bits [9:8]	R18, R1A, R1C, R1E	[7:6] Unused [5:4] Channel A Margin Command Bits (Write Only) [3:2] Channel B Margin Command Bits (Write Only) [1:0] Channel C Margin Command Bits (Write Only)
R05	[0:7] Channel C Nominal Voltage [7:0]		
R06	[7:4] Unused [3:2] Channel D Margin Nominal Vref Bits [1:0] [0:1] Channel D Nominal Voltage Bits [9:8]		
R07	[0:7] Channel D Nominal Voltage [7:0]		
R08	[0:1] Channel E Nominal Voltage Bits [9:8] [3:2] Channel E Margin Nominal Vref Bits [1:0] [7:4] Unused		
R09	[0:7] Channel E Nominal Voltage [7:0]		
R0A	[7:4] Unused [3:2] Channel F Margin Nominal Vref Bits [1:0] [0:1] Channel F Nominal Voltage Bits [9:8]		
R0B	[0:7] Channel F Nominal Voltage [7:0]		
R0C	[7] Regulator Output Voltage [6] Fast Convergence [5] Channel F Trim Polarity [4] Channel E Trim Polarity [3] Channel D Trim Polarity [2] Channel C Trim Polarity [1] Channel B Trim Polarity [0] Channel A Trim Polarity		



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R19, R1B, R1D, R1F	[7:6] Unused [5:4] Channel D Margin Command Bits (Write Only) [3:2] Channel E Margin Command Bits (Write Only) [1:0] Channel F Margin Command Bits (Write Only)
R20 to R2F	Unused
R30	[7:4] Unused [3:2] Channel A Margin High Vref Bits [1:0] [0:1] Channel A Margin High Voltage Bits [9:8]
R31	[7:0] Channel A Margin High Bits [7:0]
R32	[7:4] Unused [3:2] Channel B Margin High Vref Bits [1:0] [0:1] Channel B Margin High Voltage Bits [9:8]
R33	[7:0] Channel B Margin High Bits [7:0]
R34	[7:4] Unused [3:2] Channel C Margin High Vref Bits [1:0] [0:1] Channel C Margin High Voltage Bits [9:8]
R35	[7:0] Channel C Margin High Bits [7:0]
R36	[7:4] Unused [3:2] Channel D Margin High Vref Bits [1:0] [0:1] Channel D Margin High Voltage Bits [9:8]
R37	[7:0] Channel D Margin High Bits [7:0]
R38	[7:4] Unused [3:2] Channel E Margin High Vref Bits [1:0] [0:1] Channel E Margin High Voltage Bits [9:8]
R39	[7:0] Channel E Margin High Bits [7:0]

R3A	[7:4] Unused [3:2] Channel F Margin High Vref Bits [1:0] [0:1] Channel F Margin High Voltage Bits [9:8]
R3B	[7:0] Channel F Margin High Bits [7:0]
R3C to R3F	Unused
R40	[7:4] Unused [3:2] Channel A Margin Low Vref Bits [1:0] [0:1] Channel A Margin Low Voltage Bits [9:8]
R41	[7:0] Channel A Margin Low Bits [7:0]
R42	[7:4] Unused [3:2] Channel B Margin Low Vref Bits [1:0] [0:1] Channel B Margin Low Voltage Bits [9:8]
R43	[7:0] Channel B Margin Low Bits [7:0]
R44	[7:4] Unused [3:2] Channel C Margin Low Vref Bits [1:0] [0:1] Channel C Margin Low Voltage Bits [9:8]
R45	[7:0] Channel C Margin Low Bits [7:0]
R46	[7:4] Unused [3:2] Channel D Margin Low Vref Bits [1:0] [0:1] Channel D Margin Low Voltage Bits [9:8]
R47	[7:0] Channel D Margin Low Bits [7:0]
R48	[7:4] Unused [3:2] Channel E Margin Low Vref Bits [1:0] [0:1] Channel E Margin Low Voltage Bits [9:8]
R49	[7:0] Channel E Margin Low Bits [7:0]
R4A	[7:4] Unused [3:2] Channel F Margin Low Vref Bits [1:0] [0:1] Channel F Margin Low Voltage Bits [9:8]
R4B	[7:0] Channel F Margin Low Bits [7:0]
R4C TO R4F	Unused



Application Note 40

The following registers are accessed using slave address 1001 A2 A1 A0

R85 (Read Only)	[7] DC Control Status [6] Unused [5:4] Channel A Margin Command Bits [3:2] Channel B Margin Command Bits [1:0] Channel C Margin Command Bits
R86 (Read Only)	[7] DC Control Status [6] Unused [5:4] Channel D Margin Command Bits [3:2] Channel E Margin Command Bits [1:0] Channel F Margin Command Bits
R87	[7:4] Write Protect Memory [3:0] Write Protect Config
R88	Status Tracking Code Revision

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