

SMM665, 605, 205, 105 Supply Voltage Marginers and Active DC Output Controllers COMPONENT SELECTION FOR OPTIMUM PERFORMANCE

INTRODUCTION

The SMM665, SMM605, SMM205 and SMM105 Supply Voltage Marginers and Active DC Output Controllers (ADOC) require proper external component selection to achieve best performance (Figure 1). The following discussion and formulae provide the design engineer the guidelines to obtain this performance. The values found may be used with DC-DC converters, LDOs and on-card converters.

COMPONENT SELECTION

Choosing the C_{TRIM_CAP} Value

The value of the C_{TRIM_CAP} determines both the time required to Margin the converter's output voltage and the amount of output ripple voltage induced by the ADOC function. To find the value of the C_{TRIM_CAP} that minimizes output ripple voltage while keeping the MARGIN settling time as short as possible, first find the converter's output voltage gain from its TRIM pin input:

$$\text{Eq. 1: } A_v \cong \frac{\Delta V_{\text{sense}+}}{\Delta V_{\text{Trim}}}$$

Where:

A_v = TRIM to converter's output voltage gain

$\Delta V_{\text{SENSE}+}$ = +SENSE voltage change

ΔV_{TRIM} = TRIM voltage change

For example, a typical converter with a nominal output voltage of 3.3V is found to have a voltage gain of:

$$\text{Eq. 1: } A_v \cong \frac{3.30V - 2.97V}{0.816V - 1.463V} = -0.51V/V$$

Note: See "Setting the Value of R_{TRIM} (Figure 2)" for determining A_v for discrete PWM controller circuits.

The converter ripple voltage induced (caused) by the ADOC function is:

$$\text{Eq. 2: } V_{\text{output_ripple}} = \frac{|A_v| \cdot i_s \cdot t_s}{C_{TRIM_CAP}}$$

Where:

$V_{\text{output_ripple}}$ = converter's output ripple voltage caused by the ADOC function.

i_s = current (30uA) used to charge the $C_{TRIMCAP}$ during the ADOC cycle.

t_s = sample period (5uS)

C_{TRIM_CAP} = value of the C_{TRIM_CAP} .

Rearranging Eq. 2 to solve for the $C_{TRIMCAP}$ value:

$$\text{Eq. 3: } C_{TRIM_CAP} = \frac{|A_v| \cdot i_s \cdot t_s}{V_{\text{output_ripple}}}$$

Choose a 100uV output ripple voltage for the 3.3V converter:

Insert this value into Eq. 4 to find the $C_{TRIMCAP}$ value:

Eq 4.

$$C_{TRIM_CAP} = \frac{|(-0.51V/V)| \cdot (30\mu A) \cdot (5\mu S)}{(0.0001V)} = 0.77\mu F$$

Use 1uF

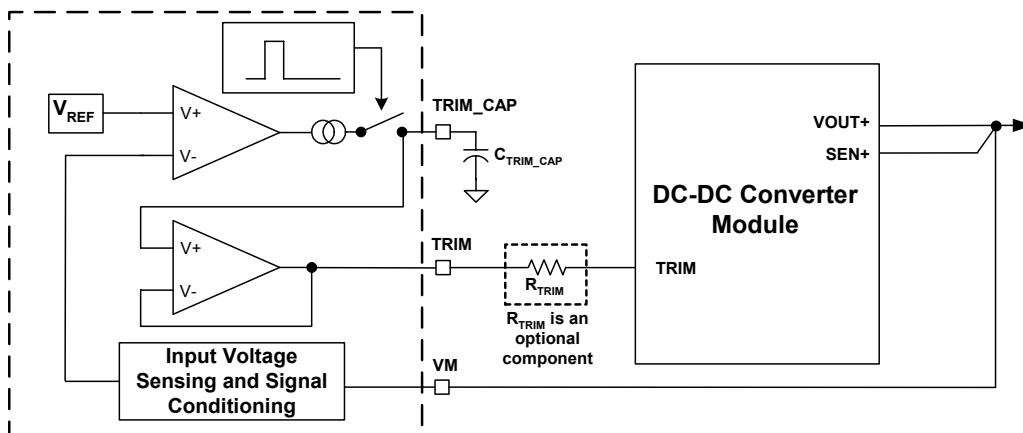


Figure 1: The ADOC function Controls DC-DC Converters via the TRIM pin. The C_{TRIM_CAP} and R_{TRIM} component type and values should be determined for best operation. The R_{TRIM} resistor is not necessary for DC_DC converter modules that have an on-board Trim Resistor.



Finding the Margin Settling Time

Once the $C_{TRIMCAP}$ value is chosen the MARGIN settling time is found:

$$\text{Eq. 5: } t_{MARGIN} \cong (t_{S/H}) \cdot \left(\frac{V_{MARGIN}}{V_{output_ripple}} \right)$$

Where:

t_{MARGIN} = time to MARGIN within V_{output_ripple} (0.1mV)

$t_{(S/H)}$ = the time required to complete an ADOC cycle = 0.00173sec

V_{MARGIN} = MARGIN (in percent) x V_{SENSE+} , e.g., 5% x 3.30V = 0.165V

Eq. 5:

$$t_{MARGIN} \cong (0.00173 \text{ sec}) \frac{(5\%) \cdot 3.30V}{0.0001V} = 2.85 \text{ sec}$$

The MARGIN time can be reduced by 1/10th by selecting the Fast Convergence feature of the device family or choosing a slightly larger ripple voltage.

Setting the Value of R_{TRIM} (Figure 2)

The device TRIM pin is connected to the Trim or VADJ pin of a DC-DC converter or adjustable switching regulator (PWM or LDO). Typically, the converter's Trim pin is internally connected to a resistor and the gain is determined either by inspecting the data sheet or empirically finding the value. In this example, the TRIM pin is connected to an external resistor (R_3 , R_{TRIM}) that is used as the equivalent resistor found in the converter module. R_3 connects to the negative input terminal of the error amplifier. This input is held at the internal reference voltage used by the converter. Another resistor (R_5) is connected from the negative input terminal to ground. Resistor (R_4) is connected from the negative input terminal to the positive sense line of the converter (output voltage) completing the resistive divider feedback network.

The current in R_5 is always $V_{REF(converter)}/R_5$. The part controls the voltage on the Trim pin that in turn controls the current through R_3 . The current through R_3 is $(V_{TRIM} - V_{REF(converter)})/R_3$. The current in R_4 (R_{TRIM}) is equal to $(V_{OUT(converter)} - V_{REF(converter)})/R_4$ where $V_{OUT(converter)}$ is the converter output voltage. With this configuration, the current in R_3 will change the converter output from its nominal output. The change in $V_{OUT(converter)}$ in Volts is equal to the current in R_3 times R_4 or $((V_{TRIM} - V_{REF(converter)})/R_3) * R_4$.

In order to minimize the ripple on the converter output due to changes in the TRIM pin voltage, R_3 can be chosen such that the maximum swing of the TRIM pin causes a maximum change of +/-10% in the converter output.

For the converter described above, R_3 is chosen as (with safety margin) less than:

$$(V_{REF(converter)} - 0.3V)/(10\% \text{ of voltage supply}) * R_4.$$

Once R_3 is chosen, the ripple on the converter output (usually set under 1mV) can be calculated as the ripple on the TRIM pin times R_4/R_3 .

TRIM_CAP Selection

The ADOC function requires attention be paid to minimize the leakage current from the TRIM_CAP pin. The maximum allowable leakage from this pin is:

$$\text{Eq. 6: } I_{L(TRIM_CAP_Node)} \leq \left(\frac{5\mu S \cdot 30\mu A}{0.0017S} \right) \leq 87nA$$

Allowing for PCB and other leakage sources use 50nA as the maximum leakage allowed from the TRIM_CAP node capacitor. For a circuit having an average voltage of 5V on the TRIM_CAP capacitor, the maximum allowable leakage (IR) resistance of the capacitor is:

$$\text{Eq. 7: } R_{L(TRIM_CAP)} \geq \left(\frac{5V}{50nA} \right) \geq 100M\Omega$$

Many vendors offer an X7R type ceramic of value 1uF with adequate IR (insulation resistance) to be suitable for the ADOC TRIM_CAP (see list below). Be certain the ceramic capacitor chosen also meets or exceeds the IR requirements at elevated temperatures. Film capacitors do offer much higher IR ratings but at both a cost and space premium. These may be used as an alternative but are generally not required.

- Kemet: C0805C105K9RAC, 1uF, 0805, +/-10%, 6.3V <http://www.kemet.com>
- AVX: 08056C105KAT4A, 1uF, 0805, +/-10%, 6.3V <http://www.avxcorp.com>
- TDK p/n: C2012X7R1C105K, 1uF, 2012, +/-10%, 16V <http://www.component.tdk.com>
- NIC Components Corporation: p/n NMC0805X7R105K16TRP, 1uF, 0805, +/-10%, 16V <http://www.niccomp.com>



Application Note 37

SUMMARY

The SMM665/605/205/105 family ADOC and Margining features achieve very high accuracy control of DC-DC converters, LDO's and other power supply regulators. They also have the added benefit of true user programmable ADOC and Margin voltage settings

along with many other valuable features useful for monitoring, sequencing and reacting to the performance of system power supplies. Flexible operation and in-field changes are made possible using the device's programmable, non-volatile configuration and General Purpose memory array.

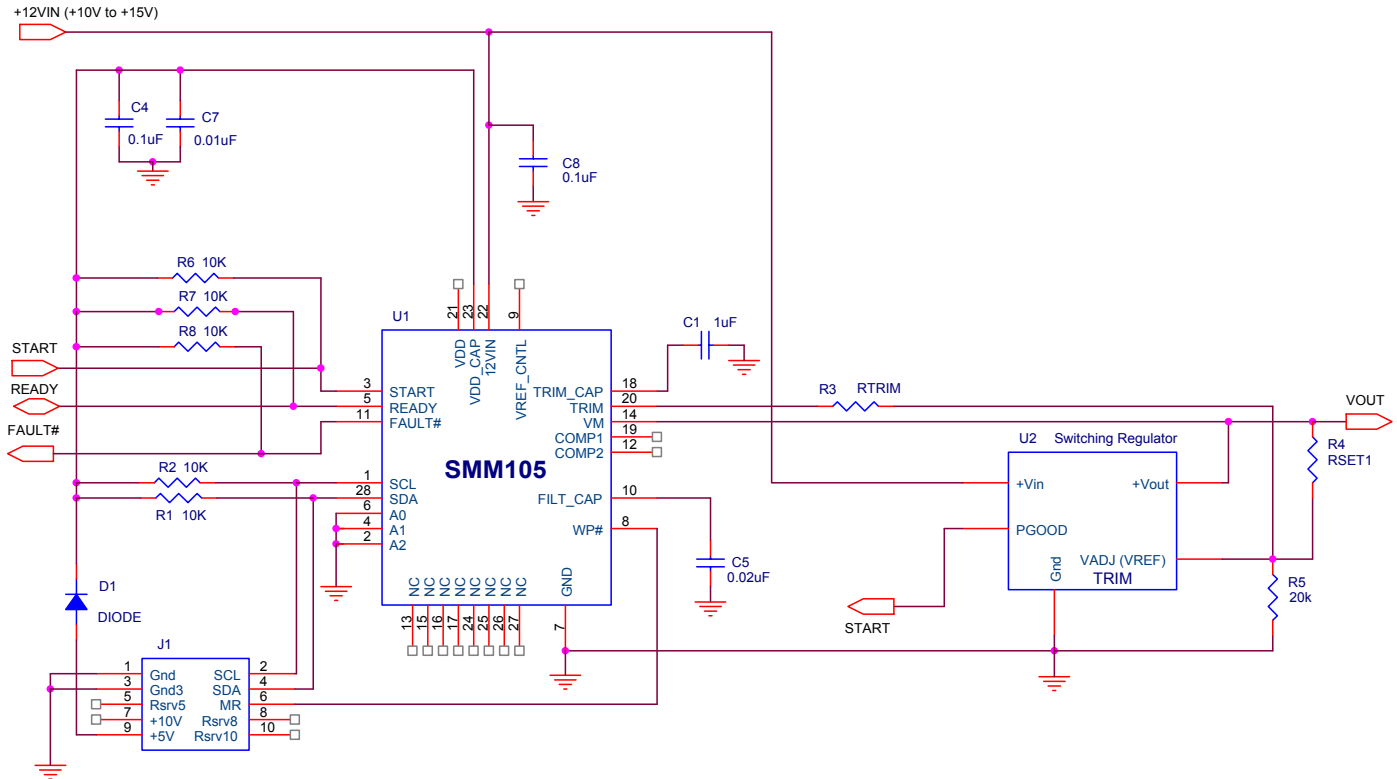


Figure 2: Typical SMM105 application schematic with interface to a DC-DC Converter or adjustable switching regulator. The SMM665/605 and SMM205 have the same interfaces.

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