

SMH4804 -48V Programmable Hot Swap Sequencing Power Controller Windows GUI Users Guide and Configuration Register Descriptions

Introduction

The information contained in Application Note 29 details the Configuration Register settings for the SMH4804 programmable Hot Swap power controller. The SMH4804 Windows Graphical User Interface (GUI) is also shown with the associated register and function highlighted. For additional explanation on device functionality related to the configuration registers, also refer to the SMH4804 Data Sheet.

Register Formats and Functions

A total of nine Configuration Registers define the set-up of the SMH4804. Some configuration registers are used to enable or disable a function, or to select between functions. Other registers determine various timeout intervals or voltage values. A final register allows the device to be powered on and off over the I²C bus and allows the device to be latched off under fault conditions. All Write and Read operations use either the 1010b or 1011b slave address (configurable) of the I²C protocol.

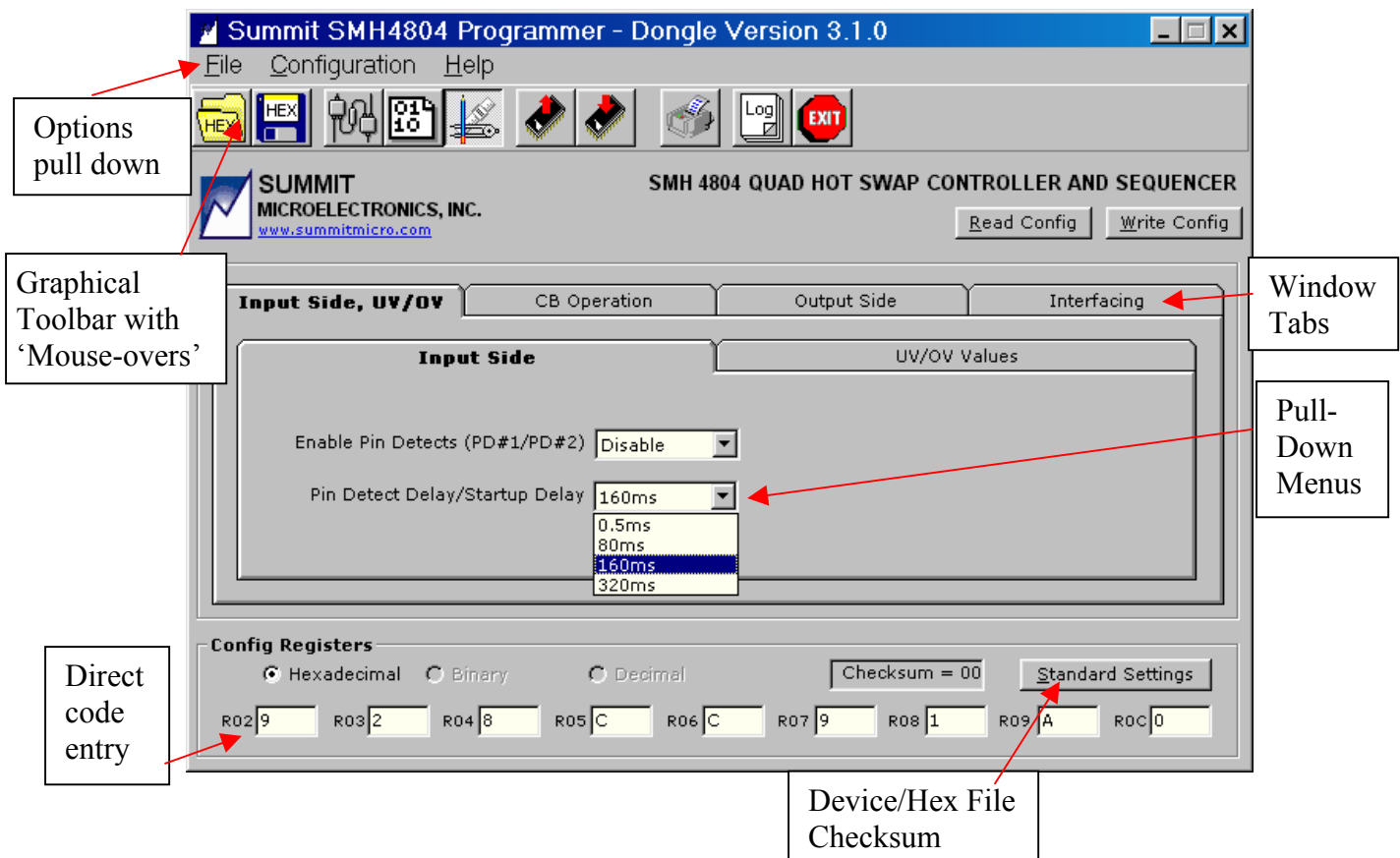


Figure 1 – SMH4804 Windows GUI Features

SMH4804 Windows Graphical User Interface

The Windows GUI (Figure 1) is used with the SMX3200 programming 'Dongle'. It is an easy to use Graphical Interface that is compatible with Windows 95, 98, NT, 2000 and XP operating systems. The GUI consists of pull-down menus, check boxes, up/down buttons, etc..

There are "mouse-overs" that define the buttons along the toolbar and an expert mode for directly entering data into the configuration registers. The GUI generates a checksum that can compare the programmed device configuration register values versus the hex file contents.



Application Note 29

Help Menu

The Help menu can be used to view the Datasheet or this app note while prototyping with the Windows GUI. During software installation, the datasheet and app note are loaded in the same directory as the program to automatically find them using this feature. The 'About' selection will show the GUI version number. Refer to Summit's web site for the most current datasheet and GUI software (www.summitmicro.com).

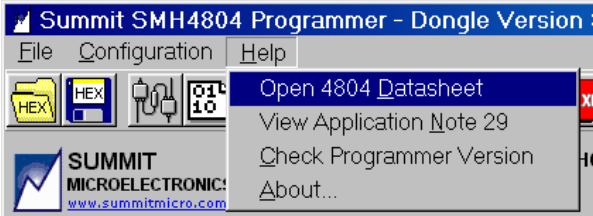


Figure 2 - Help Menu

Configuration Pull Down Menu

This menu has an option that will check for communications between the device and the PC. This selection should be tried first before changing any options. If the test passes, then all other options can be left in the default condition.

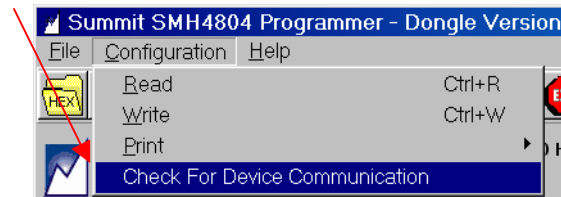


Figure 3 - Configuration Window

Setup Options

In the "File" pull-down menu under "Options", there are "Settings" to set the I²C clock frequency and delays before I²C Read and Write operations. The default settings work with most PCs, so these settings are only for circumstances where the PC cannot communicate successfully with the SMX3200 programming 'Dongle'. The "Auto-Read Configuration/Memory After Write" check box enables a checksum test which compares the GUI hex settings or file to the programmed device at the end of a Write operation. It does this by performing a Read immediately following a Write.

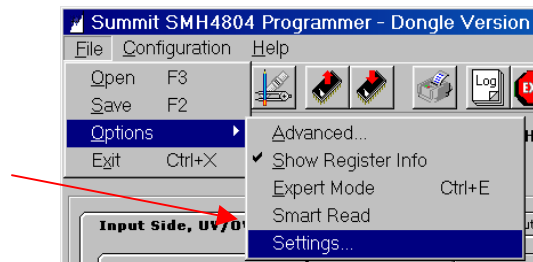


Figure 4 - Options Window

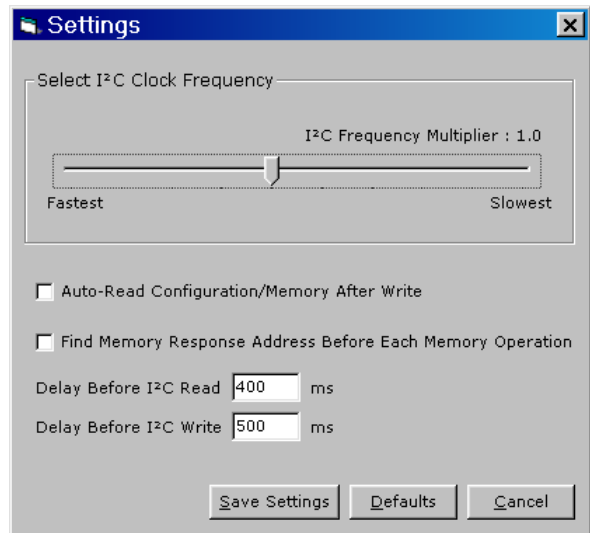


Figure 5 - Settings Options Window

Interfacing Options

In the "File" pull-down menu under "Options", there are "Advanced" settings for parallel Port Interfacing. The window in Figure 7 sets different options for programming the device using the PC parallel port. The 'Parallel Port Interfacing' should always be set to 'Dongle'. The 'Parallel Port Driver' and address is indicated here and can be changed if a problem is encountered.

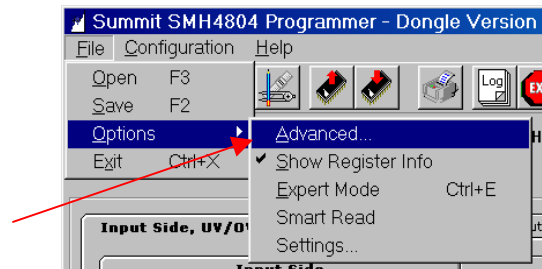


Figure 6 - Advanced Options Window

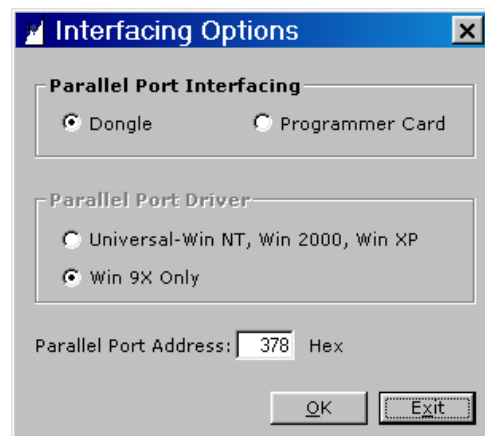


Figure 7 - Interfacing Options Window



Application Note 29

Register R02 – Over-Current and Quick Trip Thresholds

This register is used to select both the over-current delay and the quick trip threshold for the electronic circuit breaker.

| Bits | | | | Default | R/W | Description |
|------|---|---|---|---------|-----|---|
| 3 | 2 | 1 | 0 | | | |
| 0 | 0 | | | 0b10 | R/W | Set Over-current delay to 400 μ s. |
| 0 | 1 | | | | | Set Over-current delay to 150 μ s. |
| 1 | 0 | | | | | Set Over-current delay to 50 μ s. |
| 1 | 1 | | | | | Set Over-current delay to 5 μ s. |
| | | 0 | 0 | 0b01 | R/W | Set Quick Trip reference voltage to 200 mV. |
| | | 0 | 1 | | | Set Quick Trip reference voltage to 100 mV. |
| | | 1 | 0 | | | Set Quick Trip reference voltage to 60 mV. |
| | | 1 | 1 | | | Set Quick Trip reference voltage off. |

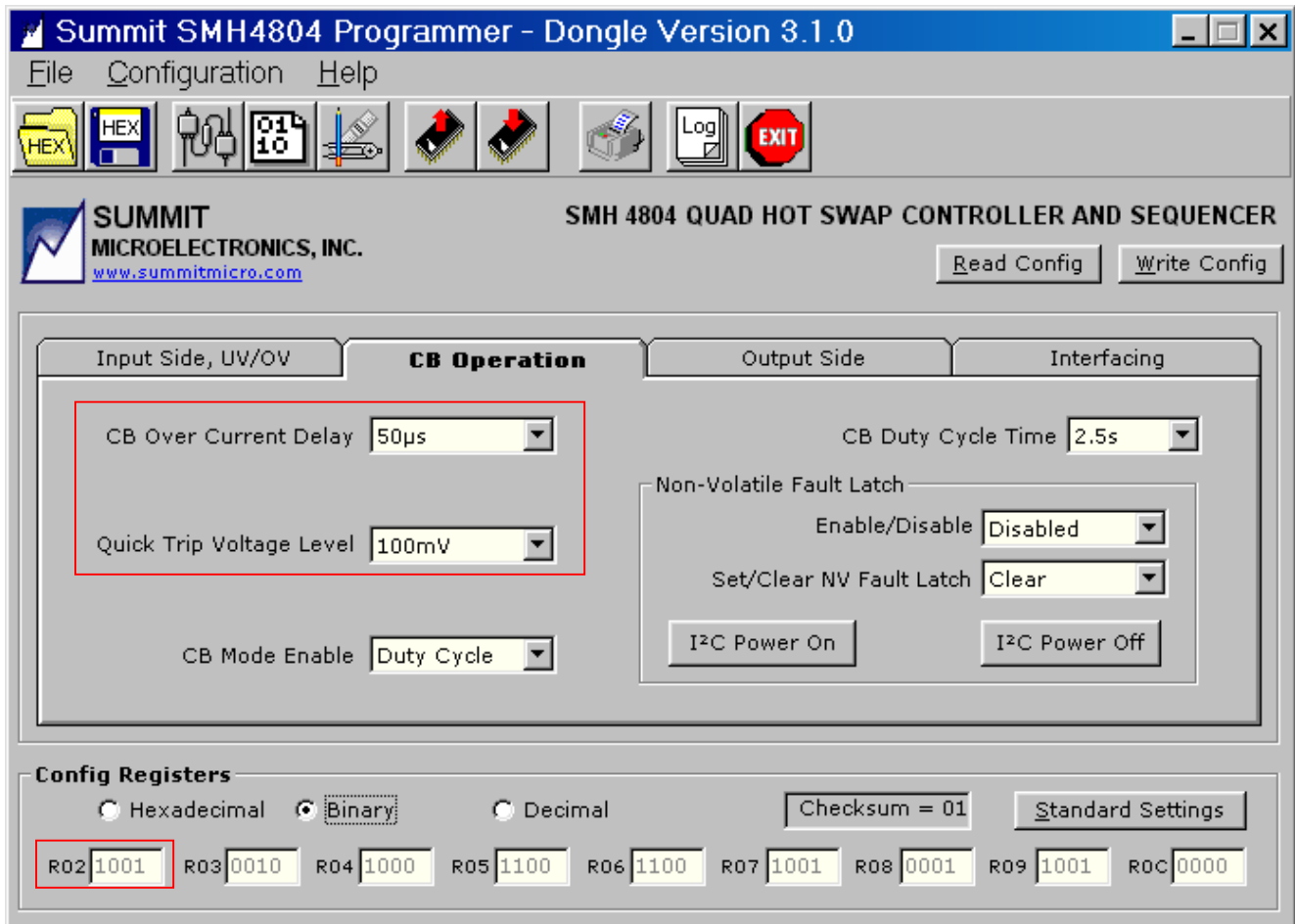


Figure 8 - Register R02 Windows GUI Tab



Application Note 29

Register R03 – Sequencing delay times, MODE pin function.

This register is used to control the sequencing delays from PG1# to PG2#, PG2# to PG3#, and PG3# to PG4#. The SMH4804 provides two levels of sequencing delay: fast and slow, which is selected by programming bit 3 of Register 9. These two bits are effectively concatenated with R9 bit 3, providing 8 programmable delay periods. Refer to Register 9 for more information.

NOTE - Bit 1 controls the effect of the MODE pin. When set (high) the pin functions as described in the pin descriptions. If the bit is cleared (low) the state of the pin is ignored and the circuit breaker enters latch mode.

Bit 0 enables or disables the function of the PD[4:1]# inputs.

| Bits | | | | Default | R/W | Description |
|--|---|---|---|---------|-----|--|
| 3 | 2 | 1 | 0 | | | |
| When Register 9, bit 3 = 0 | | | | | | |
| 0 | 0 | | | 0b00 | R/W | PG[4:1]# Sequencing delay: 1500 μ s. |
| 0 | 1 | | | | | PG[4:1]# Sequencing delay: 50 μ s. |
| 1 | 0 | | | | | PG[4:1]# Sequencing delay: 250 μ s. |
| 1 | 1 | | | | | PG[4:1]# Sequencing delay: 500 μ s. |
| When Register 9, bit 3 = 1 | | | | | | |
| 0 | 0 | | | 0b00 | R/W | PG[4:1]# Sequencing delay: 5 ms. |
| 0 | 1 | | | | | PG[4:1]# Sequencing delay: 20 ms. |
| 1 | 0 | | | | | PG[4:1]# Sequencing delay: 80 ms. |
| 1 | 1 | | | | | PG[4:1]# Sequencing delay: 160 ms. |
| Register 9, bit 3 = X, don't care | | | | | | |
| | | 0 | | 0b1 | R/W | When bit 1 is cleared (0), the CB MODE is disabled (see NOTE above). |
| | | 1 | | | | When bit 1 is set (1), the CB MODE is enabled (see NOTE above). |
| | | | 0 | 0b0 | | When bit 0 is cleared, the PD1# and PD2# signals are disabled. |
| | | | 1 | | | When bit 0 is set, the PD1# and PD2# signals are enabled. |



Application Note 29

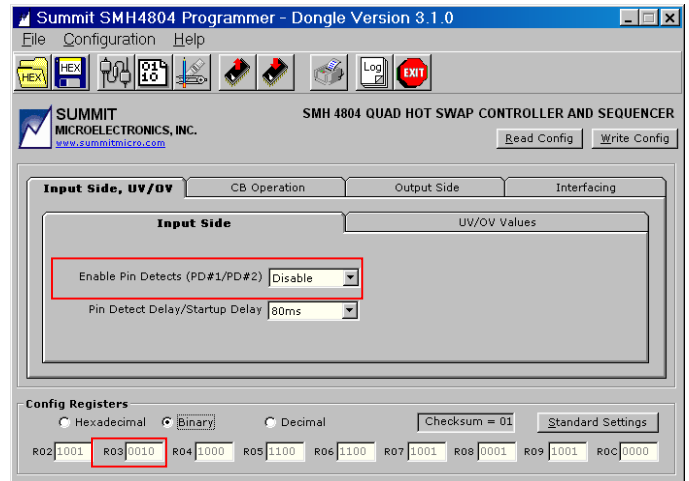
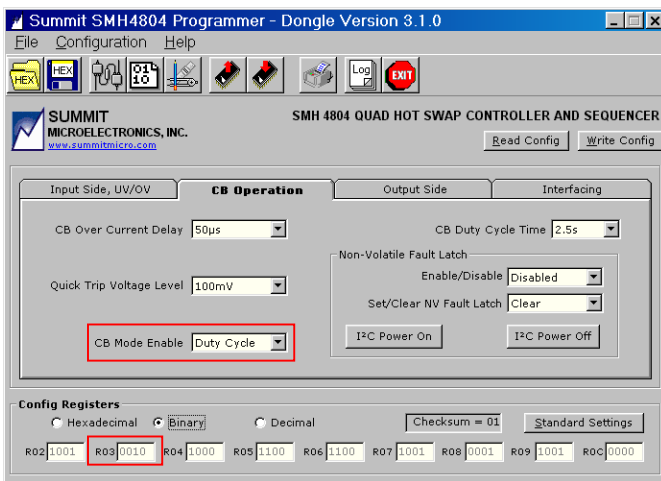
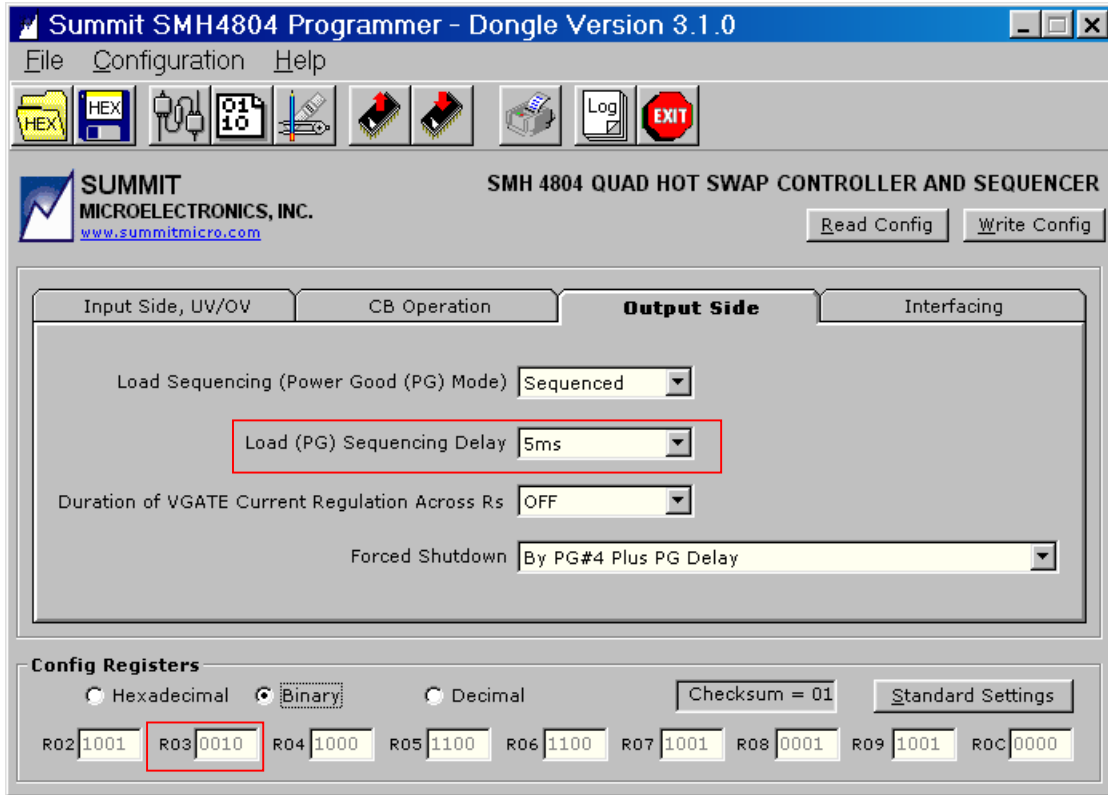


Figure 9 - Register R03 Windows GUI



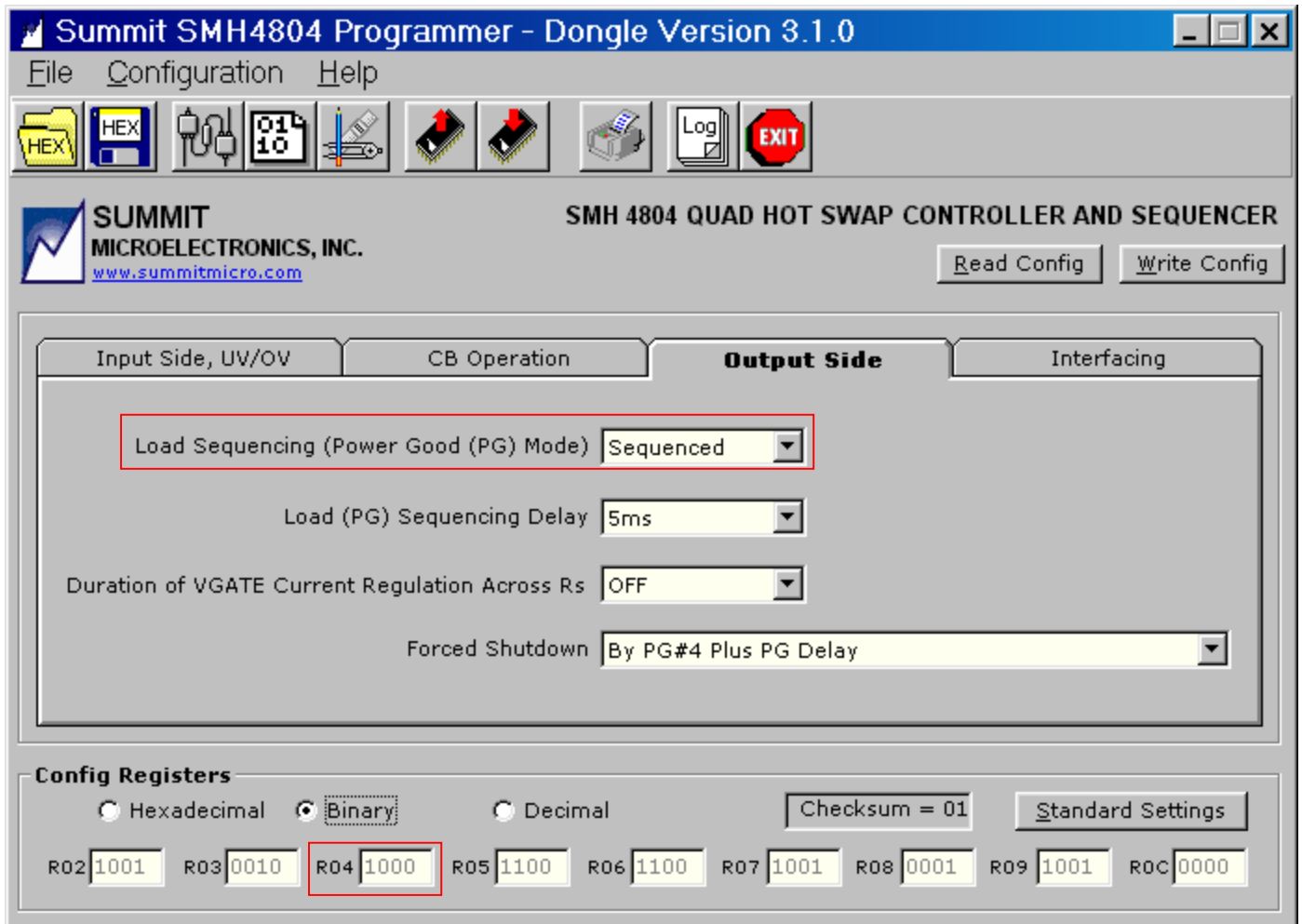
Application Note 29

Register R04 – Sequence, OV/UV filter time, Circuit breaker cycle time.

Register 4 enables PG[4:1]# signal sequencing, sets the O/U voltage filter timing, and selects the circuit breaker cycle time.

Bit 3 of this register enables or disables the PG[4:1]# sequence delays. When set, the delays are defined in registers 3 and 9. If bit 3 is cleared, no delay is incurred and sequencing is based solely on the state of the ENPGA#, ENPGB#, and ENPGC# inputs. If the ENPGx# inputs are tied high, the PG[4:1]# outputs turn on simultaneously.

| Bits | | | | Default | R/W | Description |
|------|---|---|---|---------|-----|--|
| 3 | 2 | 1 | 0 | | | |
| 0 | | | | 0b1 | R/W | When bit 3 is cleared, PG[4:1]# signal sequencing is simultaneous. |
| 1 | | | | | | When bit 3 is set, PG[4:1]# signal sequencing is enabled. |
| | 0 | 0 | | 0b00 | R/W | When bits 2:1 are set to 0b00, the over/under voltage filter is off. |
| | 0 | 1 | | | | When bits 2:1 are set to 0b01, the over/under voltage delay is 5 ms. |
| | 1 | 0 | | | | When bits 2:1 are set to 0b10, the over/under voltage delay is 80 ms. |
| | 1 | 1 | | | | When bits 2:1 are set to 0b11, the over/under voltage delay is 160 ms. |
| | | | 0 | 0b0 | R/W | When bit 0 is cleared, the circuit breaker cycle time is 2.5 sec. |
| | | | 1 | | | When bit 0 is set, the circuit breaker cycle time is 5 sec. |





Application Note 29

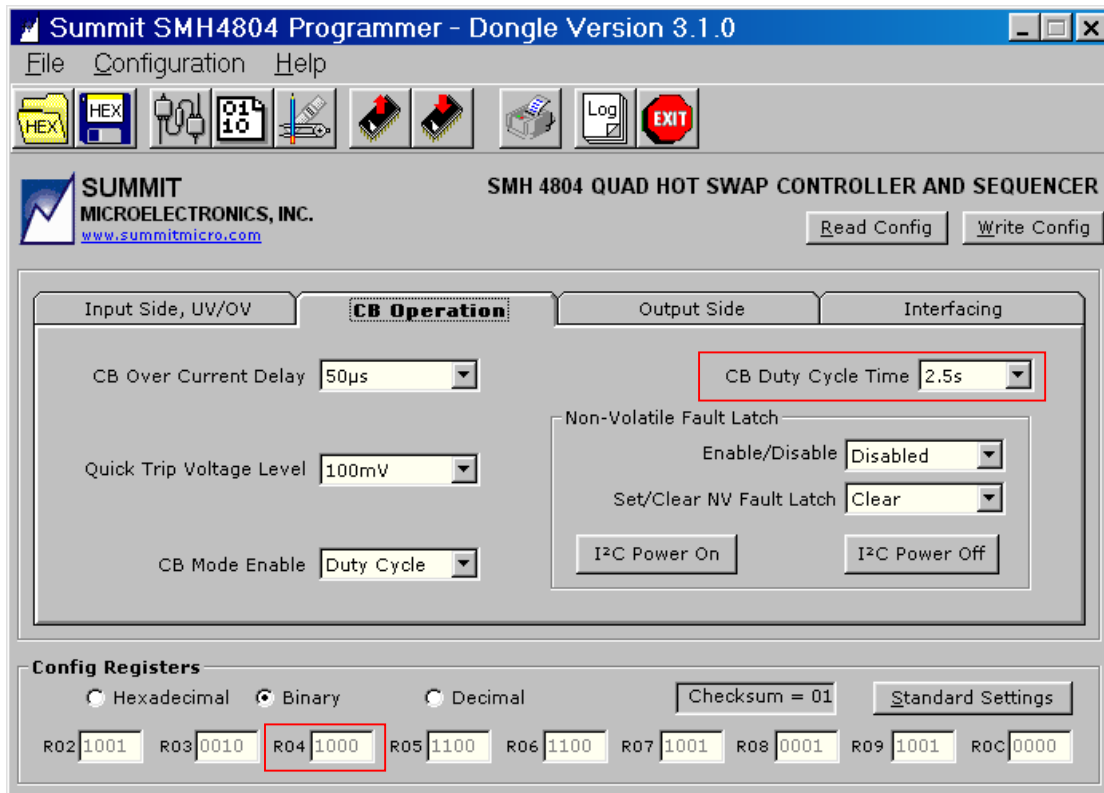
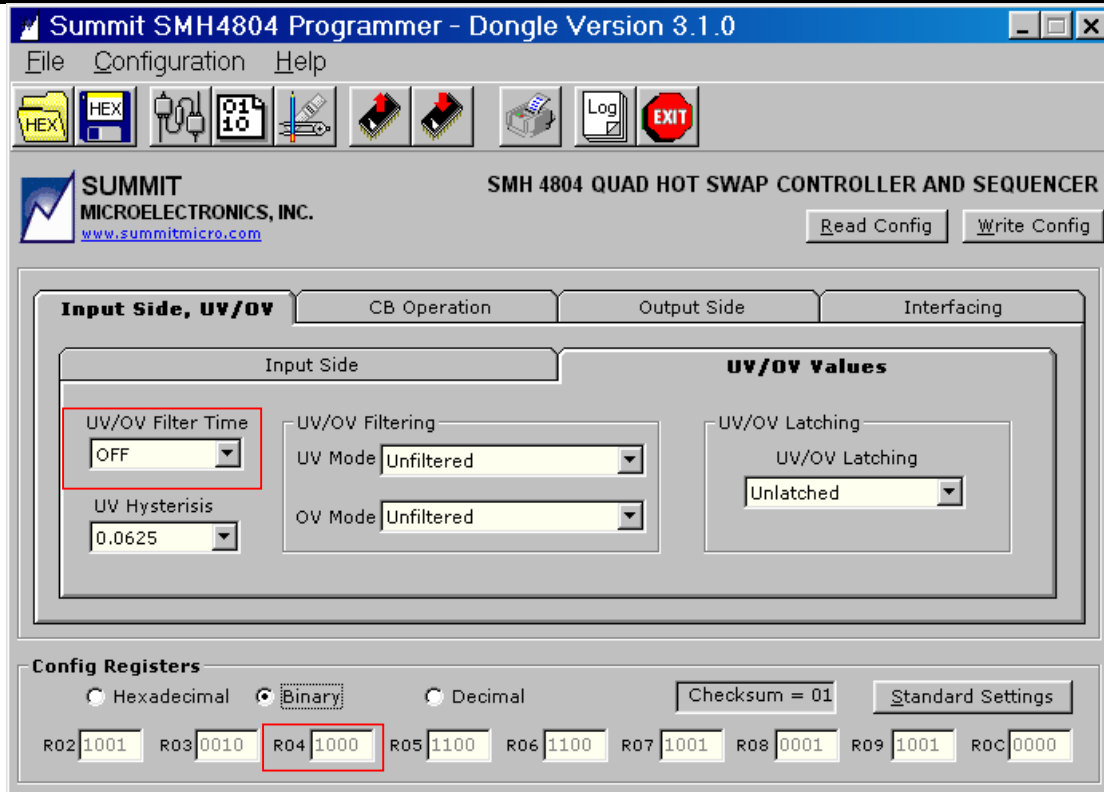


Figure 10 - Register R04 Windows GUI



Application Note 29

Register R05 – Latch function, FS# pin function, Cascade mode.

Register 5 controls the function of the nonvolatile fault latch and provides general control for the FS# input. Bit 3 controls the enabling of the non-volatile latch. Bits 2:0 configure the FS# input. The FS# pin has two basic functions: it can be programmed to act as an auxiliary enable input controlling the PG1# output, or it can be programmed to be an event monitor during the power-up sequence. These bits also control the interrelationship of the PG[4:1]# outputs. In a cascade operating mode PG1# must be true before PG2# can be true, etc. This interrelationship can be disabled so that each PG[4:1]# output is effectively controlled by its corresponding ENGPx# input, as long as the primary supply, VGATE and DRAIN SENSE pins are within their operating limits.

When programmed as an enable to PG1# there are two options: 010_{BIN} disables the cascade mode (the PG[4:1]# outputs can act independently) and FS# effectively becomes the enable input for PG1#; 011_{BIN} enables the cascade mode and makes FS# the enable input for PG1#. In this mode, PG1# must be active before PG2# can be activated, followed by PG3#, then PG4#.

The event monitor mode is generally implemented in conjunction with a monitoring device on the secondary side of the DC/DC converters, such as the SMS44, SMT4004 or SMS64. If FS# is not pulled high before the programmed condition then the PG[4:1]# and VGATE outputs are shut down. As an example, if the binary value is 111_{BIN}, VGATE and PG1# are shut down if FS# is not pulled high before t_{PGD} has elapsed after PG1# is true. None of the other PG[4:1]# outputs are activated. If a failure occurs due to the lapse of the event monitor timer, cycling the power resets the device.

One last event mode, 000_{BIN}, disables the cascade effect and sets up PG4# going true as the trigger event. FS# must be pulled high before t_{PGD} elapses, or VGATE and all of the PG[4:1]# outputs are disabled.

Cascade enabled:

- ENPGA enables PG2#, PG3# and PG4#;
- ENPGB enables PG3# and PG4#;
- ENPGC enables PG4#.

Cascade disabled:

- ENPGA enables PG2#;
- ENPGB enables PG3#;
- ENPGC enables PG4#.

Simultaneous:

PG1#, PG2#, PG3# and PG4# operate independently from one another.

Sequenced:

PG1#, PG2#, PG3# and PG4# are dependent upon activation of PG(N-1) — for N = 2, 3, and 4 — plus a programmable PG delay.p=On

| Bits | | | | Default | R/W | Description |
|------|---|---|---|---------|-----|---|
| 3 | 2 | 1 | 0 | | | |
| 0 | | | | 0b1 | R/W | When bit 3 is cleared, the non-volatile latch is enabled. |
| 1 | | | | | | When bit 3 is set, the non-volatile latch is disabled. |
| | 0 | 0 | 0 | 0b100 | R/W | When bits 2:0 are 0b000, the FS function: PG4 + t _{PGD} cascade is disabled for simultaneous assertion of the PG[4:1]# pins. |
| | 0 | 0 | 1 | | | When bits 2:0 are 0b001, the FS function is disabled (=1). |
| | 0 | 1 | 0 | | | When bits 2:0 are 0b010, the FS function is active (=1) before PG1 enabled. Cascade disabled for simultaneous assertion of the PG[4:1]# pins. |
| | 0 | 1 | 1 | | | When bits 2:0 are 0b011, the FS function must be high (de-asserted) before PG1 is enabled. |
| | 1 | 0 | 0 | | | FS function: PG4 + t _{PGD} (PG Delay) |
| | 1 | 0 | 1 | | | FS function: PG3 + t _{PGD} (PG Delay) |
| | 1 | 1 | 0 | | | FS function: PG2 + t _{PGD} (PG Delay) |
| | 1 | 1 | 1 | | | FS function: PG1 + t _{PGD} (PG Delay) |



Application Note 29

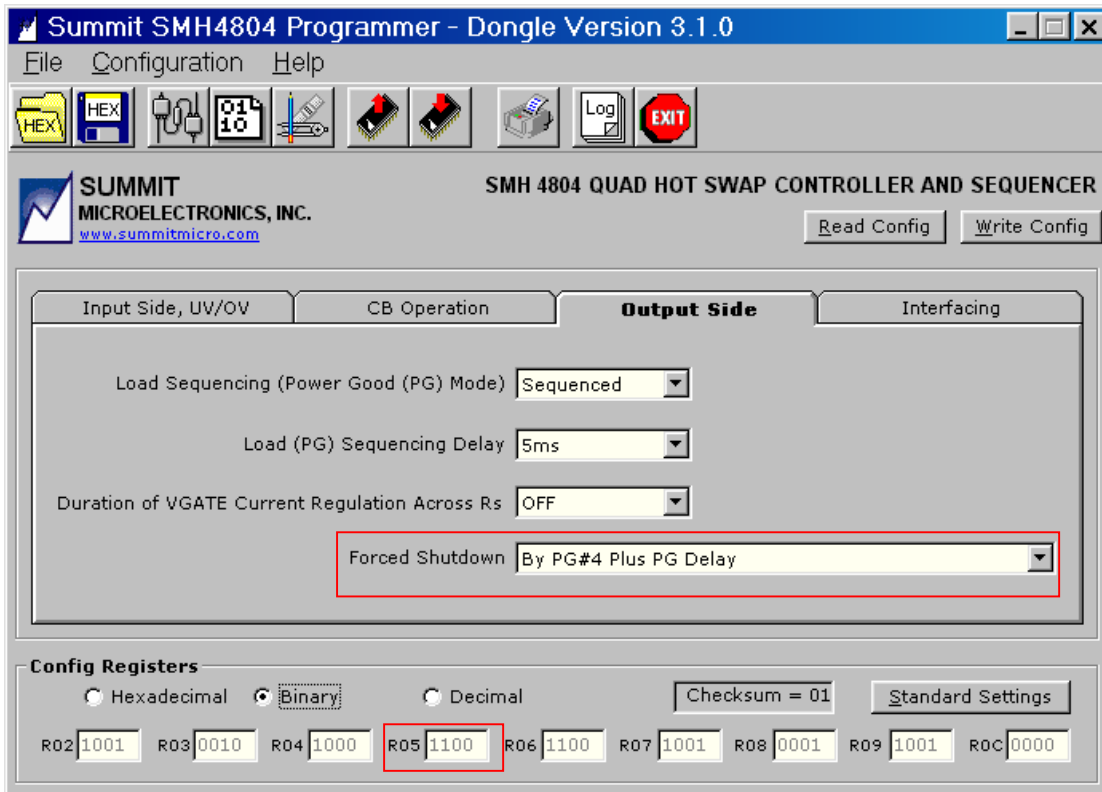
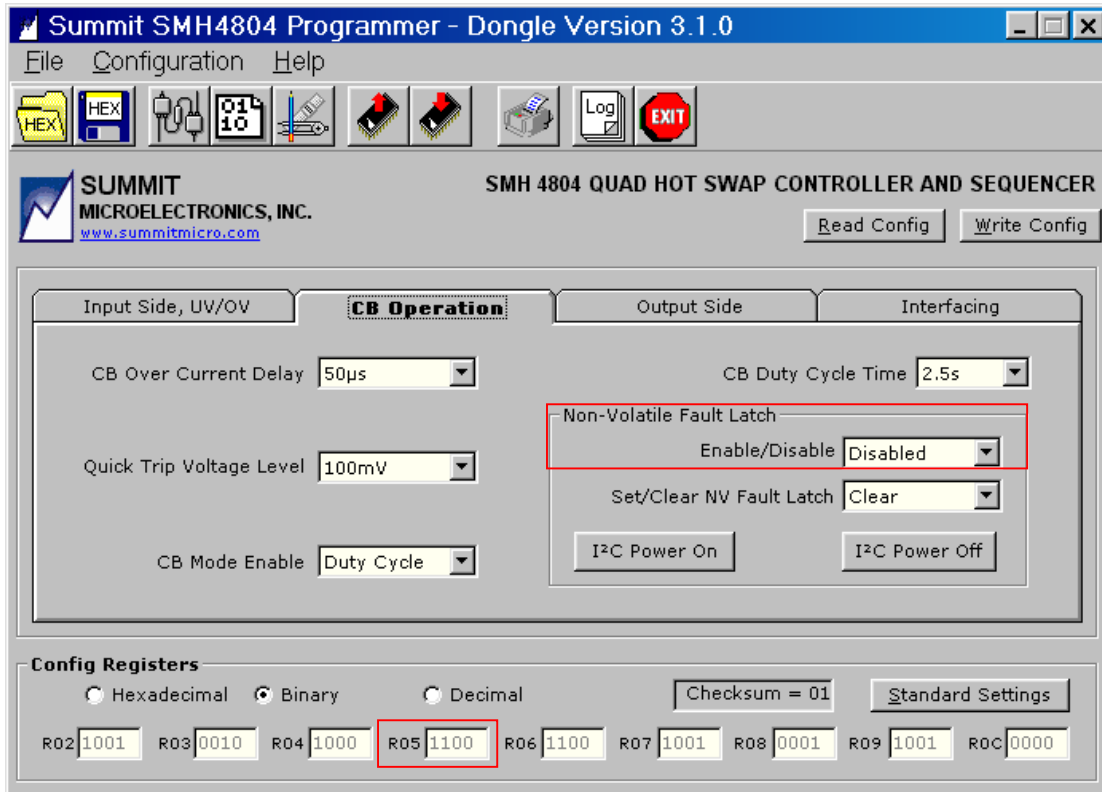


Figure 11 - Register R05 Windows GUI Tab



Application Note 29

Register R06 – Current regulation, UV/OV filters.

This register enables what events are recorded in the nonvolatile fault latch if bit 3 of R5 is cleared. The high order bits of this register control whether the under and over voltage pins are filtered, and the two low order bits program the current regulation time period.

| Bits | | | | Default | R/W | Description |
|------|---|---|---|---------|-----|--|
| 3 | 2 | 1 | 0 | | | |
| 0 | | | | 0b1 | R/W | When bit 3 is cleared, the under voltage is filtered. |
| 1 | | | | | | When bit 3 is set, the under voltage is not filtered. |
| | 0 | | | 0b1 | R/W | When bit 2 is cleared, the over voltage is filtered. |
| | 1 | | | | | When bit 2 is set, the over voltage is not filtered. |
| | | 0 | 0 | 0b00 | R/W | When bits 1:0 are set to 0b00, the current regulation is turned off. |
| | | 0 | 1 | | | When bits 1:0 are set to 0b01, the current regulation is 5 ms. |
| | | 1 | 0 | | | When bits 1:0 are set to 0b10, the current regulation is 80 ms. |
| | | 1 | 1 | | | When bits 1:0 are set to 0b11, the current regulation is 160 ms. |



Application Note 29

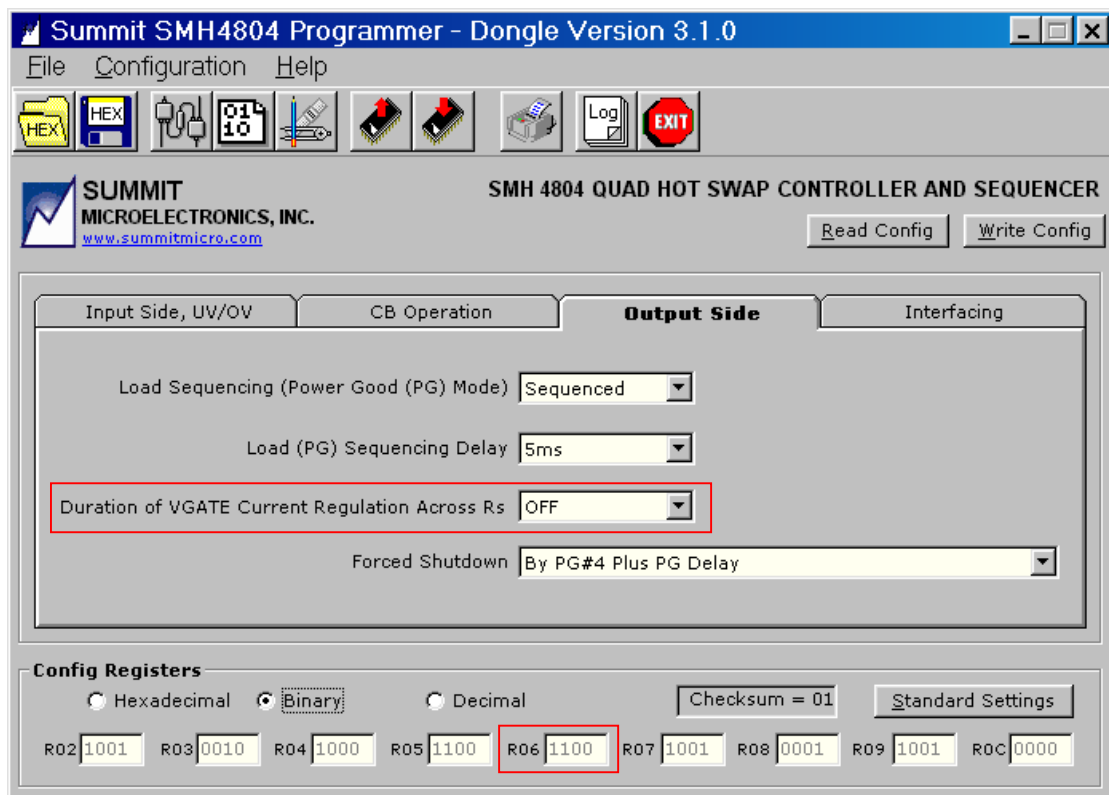
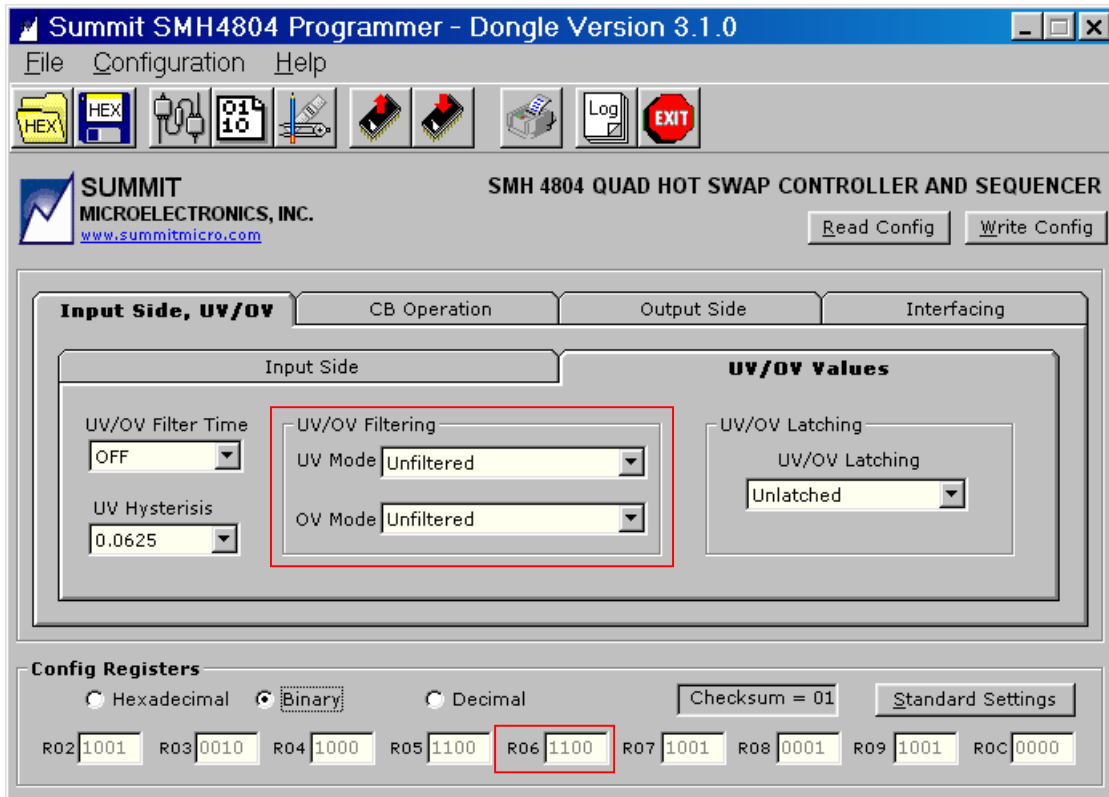


Figure 12 - Register R06 Windows GUI



Application Note 29

Register R07 – UV Hysteresis.

This register controls the UV hysteresis. The values shown are with respect to V_{ss}.

| Bits | | | | Default | R/W | Description |
|------|---|---|---|---------|-----|--|
| 3 | 2 | 1 | 0 | | | |
| 1 | | | | 0b1 | R/W | In this register, bit 3 is always set. |
| 1 | 0 | 0 | 0 | 0b001 | R/W | When bits 2:0 are 0b000, the UV hysteresis = 0.0 volts. |
| | 0 | 0 | 1 | | | When bits 2:0 are 0b001, the UV hysteresis = 0.0625 volts. |
| | 0 | 1 | 0 | | | When bits 2:0 are 0b010, the UV hysteresis = 0.125 volts. |
| | 0 | 1 | 1 | | | When bits 2:0 are 0b011, the UV hysteresis = 0.1785 volts. |
| | 1 | 0 | 0 | | | When bits 2:0 are 0b100, the UV hysteresis = 0.250 volts. |
| | 1 | 0 | 1 | | | When bits 2:0 are 0b101, the UV hysteresis = 0.3125 volts. |
| | 1 | 1 | 0 | | | When bits 2:0 are 0b110, the UV hysteresis = 0.375 volts. |
| | 1 | 1 | 1 | | | When bits 2:0 are 0b111, the UV hysteresis = 0.4375 volts. |

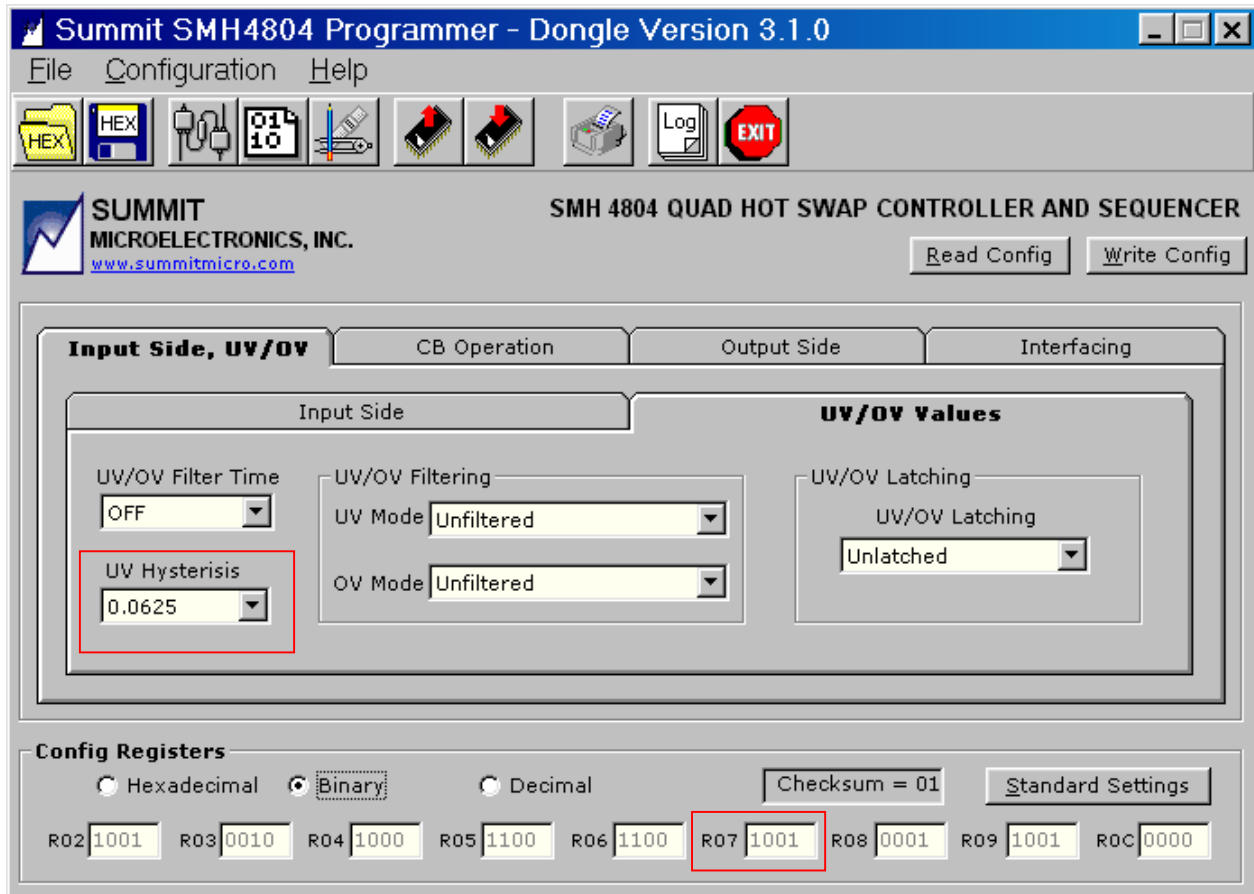


Figure 13 - Register R07 Windows GUI



Application Note 29

Register R08 – Device type address, write protect, slave address.

This register is used to control the I²C bus interface activity. Bit 3 determines the Device Type Address, bits 2 and 1 select the register access capability, and bit 0 determines whether the device must receive a bus address that corresponds to the biasing of the address pins. Note: If the fault latch option is selected and write access is denied the SMH4804 cannot be cleared of a fault condition.

| Bits | | | | Default | R/W | Description |
|------|---|---|---|---------|-----|--|
| 3 | 2 | 1 | 0 | | | |
| 0 | | | | 0b0 | R/W | When bit 3 is cleared, the device type address is 1011. |
| 1 | | | | | | When bit 3 is set, the device type address is 1010. |
| | 0 | 0 | | 0b00 | R/W | When bits 2:1 are set to 0b00, the Configuration registers are read/write (R/W). |
| | 0 | 1 | | | | When bits 2:1 are set to 0b01, the Configuration registers are read-only (RO). |
| | 1 | 0 | | | | When bits 2:1 are set to 0b10 or 0b11, access to the Configuration registers is disabled. |
| | 1 | 1 | | | | |
| | | | 0 | 0b1 | R/W | When bit 0 is cleared, the SMH4804 responds to all address pins. |
| | | | 1 | | | When bit 0 is set, the SMH4804 responds to the address set by the pin polarities (A0,A1 and A2). |

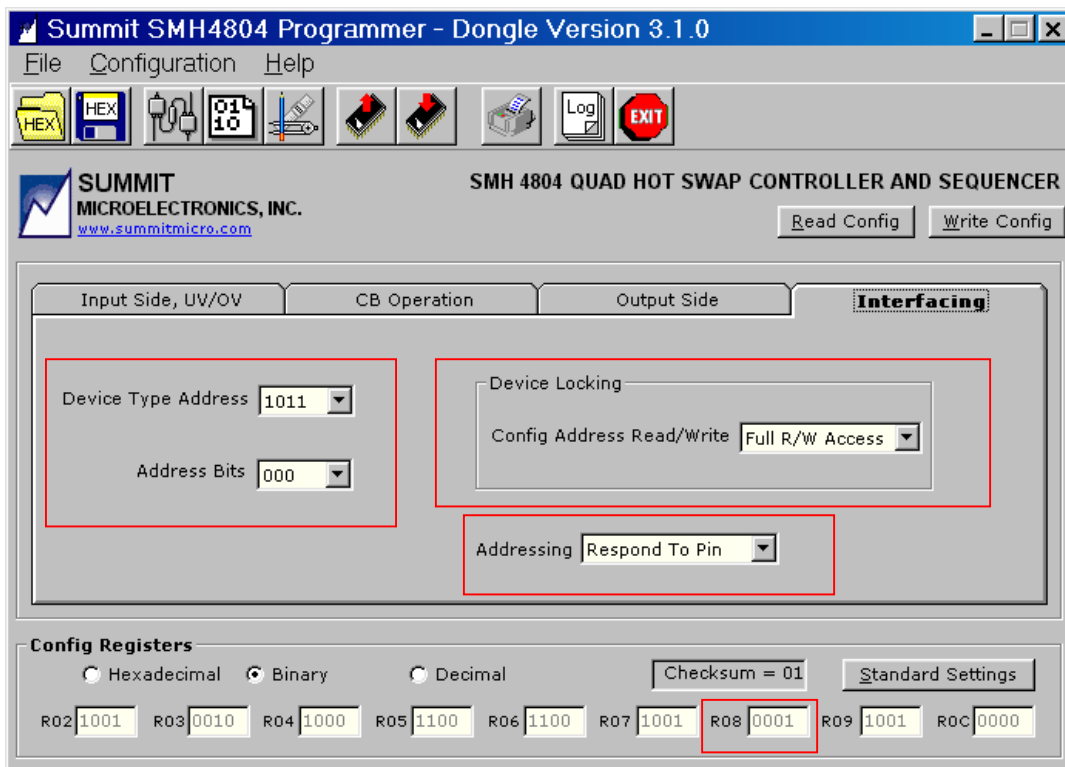


Figure 14 - Register R08 Windows GUI



Application Note 29

Register R09 – Fast/slow sequence times, PD delays.

In this register, bit 3 works in conjunction with Register 3, bits 2 and 3. Refer to the Register 3 description for details. Bit 2 sets UV/OV conditions to be either latched or not latched. Bits 1 and 0 select the delay from the point where both PD[2:1]# inputs are low (or initial power up conditions) to when sequencing can commence.

| Bits | | | | Default | R/W | Description |
|------|---|---|---|---------|-----|--|
| 3 | 2 | 1 | 0 | | | |
| 0 | | | | 0b1 | R/W | When bit 3 is cleared, the power good sequence is set to Fast. |
| 1 | | | | | | When bit 3 is set, the power good sequence is set to Slow. |
| | 0 | | | 0b0 | R/W | When bit 2 is cleared, UV/OV conditions are not latched. |
| | 1 | | | | | When bit 2 is set, UV/OV conditions are latched. |
| | | 0 | 0 | 0b01 | R/W | When bits 1:0 are set to 0b00, the PD delay is 0.5 ms. |
| | | 0 | 1 | | | When bits 1:0 are set to 0b01, the PD delay is 80 ms. |
| | | 1 | 0 | | | When bits 1:0 are set to 0b10, the PD delay is 160 ms. |
| | | 1 | 1 | | | When bits 1:0 are set to 0b11, the PD delay is 320 ms. |

The screenshot shows the Summit SMH4804 Programmer software interface. The main window title is "Summit SMH4804 Programmer - Dongle Version 3.1.0". The interface includes a menu bar (File, Configuration, Help), a toolbar with icons for file operations and hardware control, and a main configuration area. The "Output Side" tab is selected, showing "Load Sequencing (Power Good (PG) Mode)" set to "Sequenced". A dropdown menu for "Load (PG) Sequencing Delay" is open, showing options: 1500µs (selected), 50µs, 250µs, 500µs, 5ms, 20ms, 80ms, and 160ms. Below the configuration area, the "Config Registers" section shows a row of registers: R02 (1001), R03 (0010), R04 (1000), R05 (1100), R06 (1100), R07 (1001), R08 (0001), R09 (0001), and R0C (0000). The R09 register value is highlighted with a red box.



Application Note 29

The screenshot shows the Summit SMH4804 Programmer software interface. The title bar reads "Summit SMH4804 Programmer - Dongle Version 3.1.0". The menu bar includes "File", "Configuration", and "Help". The toolbar contains icons for HEX files, configuration, and other functions. The main window title is "SMH 4804 QUAD HOT SWAP CONTROLLER AND SEQUENCER". Below the title bar, there are buttons for "Read Config" and "Write Config". The interface is divided into several sections:

- Input Side, UV/OV**: This section is currently selected. It contains sub-sections for "Input Side" and "UV/OV Values".
 - Input Side**:
 - UV/OV Filter Time: OFF
 - UV Hysteresis: 0.0625
 - UV/OV Filtering: Unfiltered
 - UV Mode: Unfiltered
 - OV Mode: Unfiltered
 - UV/OV Values**:
 - UV/OV Latching: Unlatched
- Config Registers**: This section shows a row of registers with their values in binary format. The registers are R2 (1001), R3 (0010), R4 (1000), R5 (1100), R6 (1100), R7 (1001), R8 (0001), R9 (1001), and RC (0000). The R9 register is highlighted with a red box.



Application Note 29

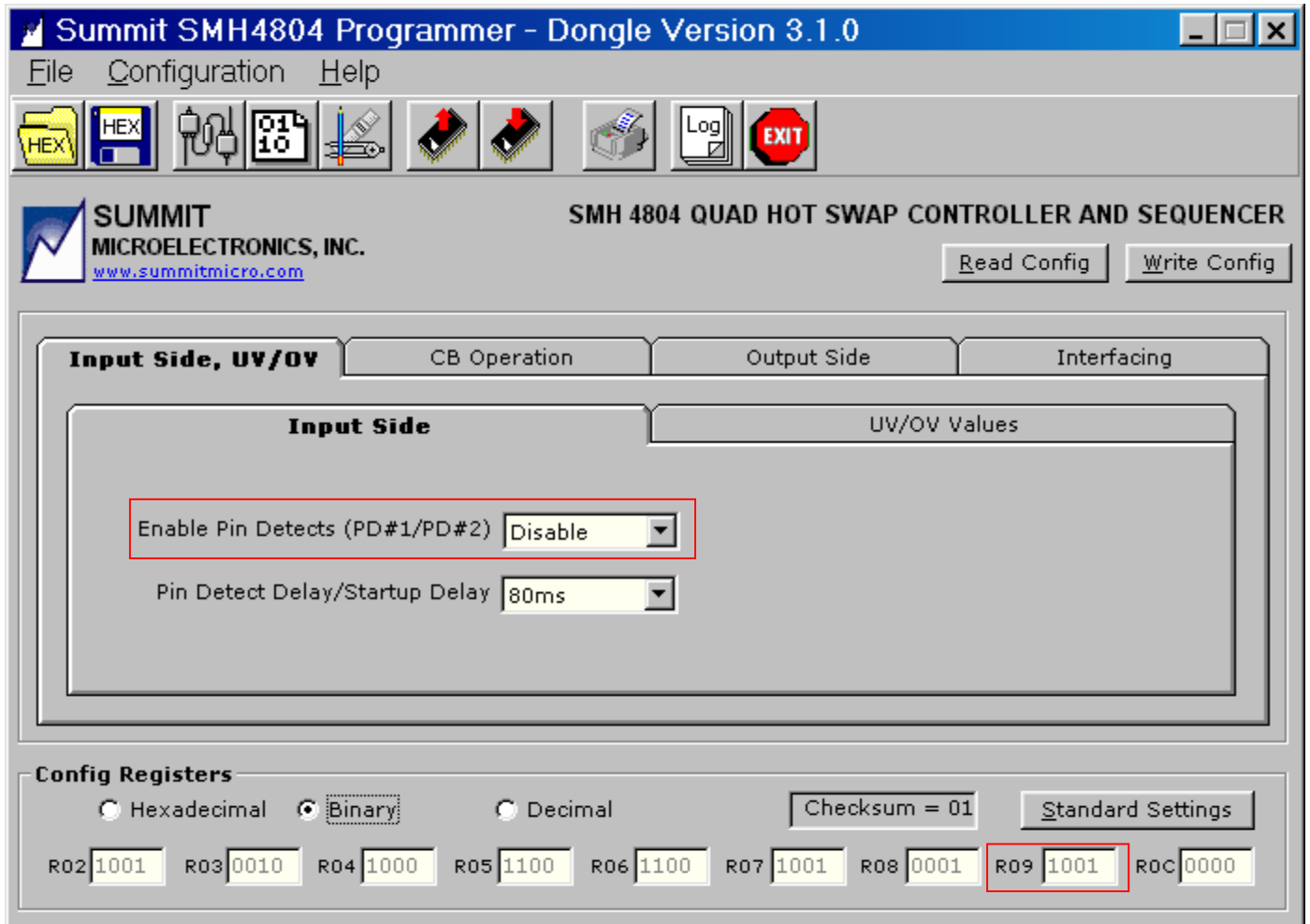


Figure 15 - Register R09 Windows GUI



Application Note 29

Register R0C – Nonvolatile fault latch (NVFL) setting, I²C power on/off

This register is not a configuration register, but rather a nonvolatile fault latch (NVFL). If a circuit breaker fault condition is detected and the NVFL is enabled (Register 5, Bit 3 cleared), bit 0 of Register C is automatically set (written with a logic '1') when the circuit breaker trips. So long as the bit remains set, the SMH4804 is not able to drive VGATE or the PG[4:1]# outputs. The host or service center must access the register and clear the bit (write a '0') once the fault condition has been resolved. The bit can also be used as a nonvolatile Power on/off control to power the SMH4804 and system through the I²C bus.

| Bits | | | | Default | R/W | Description |
|------|---|---|---|---------|-----|--|
| 3 | 2 | 1 | 0 | | | |
| | | | 0 | 0b0 | R/W | When bit 0 is cleared, the NV fault latch is cleared. This bit is cleared by software once the fault condition is resolved. When cleared by an I ² C command, the VGATE and PG[4:1]# outputs will power the system on. |
| | | | 1 | | | When bit 0 is set, the NV fault latch is set. This bit is set automatically by hardware when a fault is detected. When set by an I ² C command, the VGATE and PG[4:1]# outputs will power the system off. |

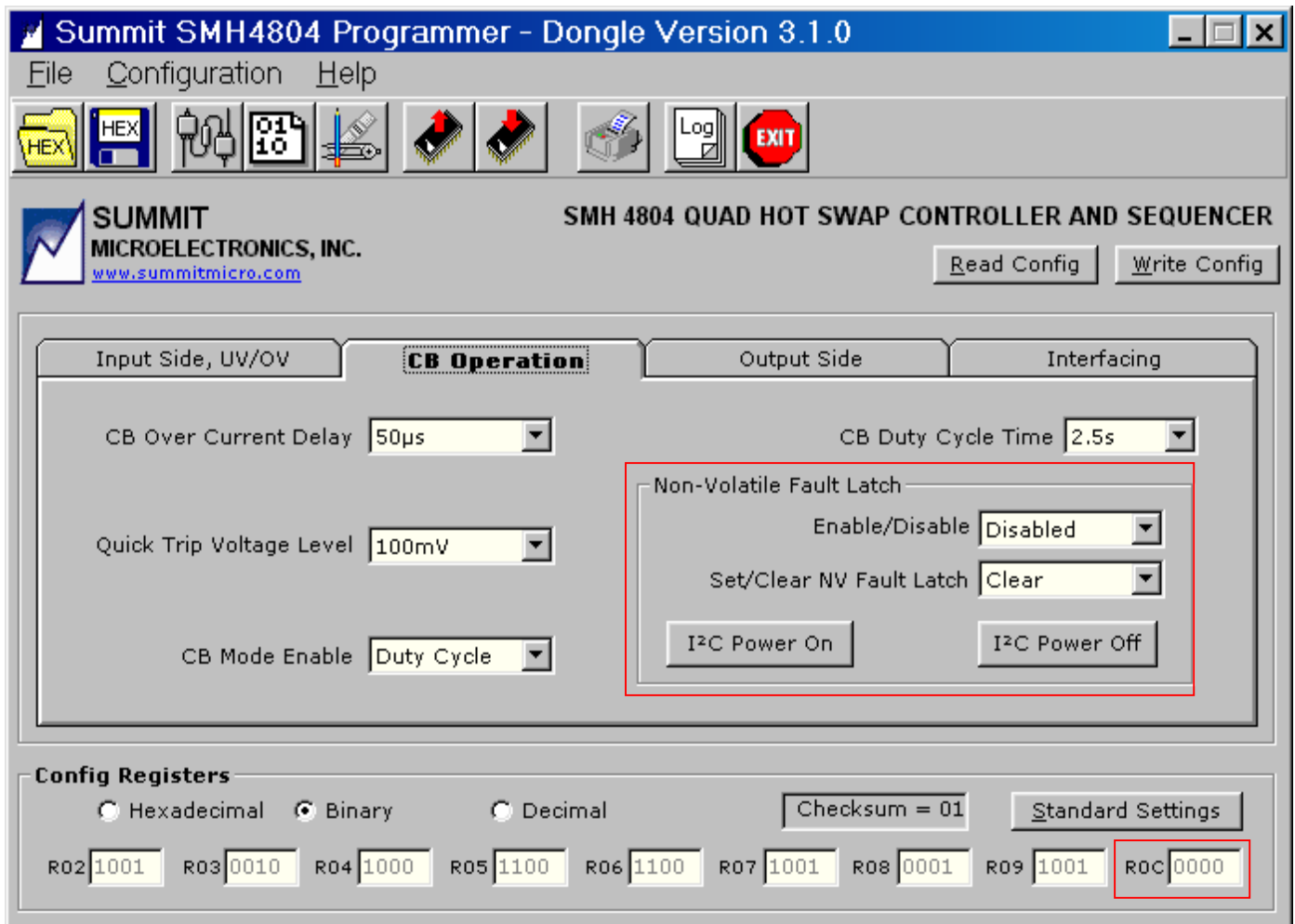


Figure 16 - Register R0C Windows GUI



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