

Disabling the Watchdog Timer

There are numerous instances when it would be convenient to shut down the watchdog timer. This note will illustrate a simple method that can be implemented with any MCU or ASIC.

Background

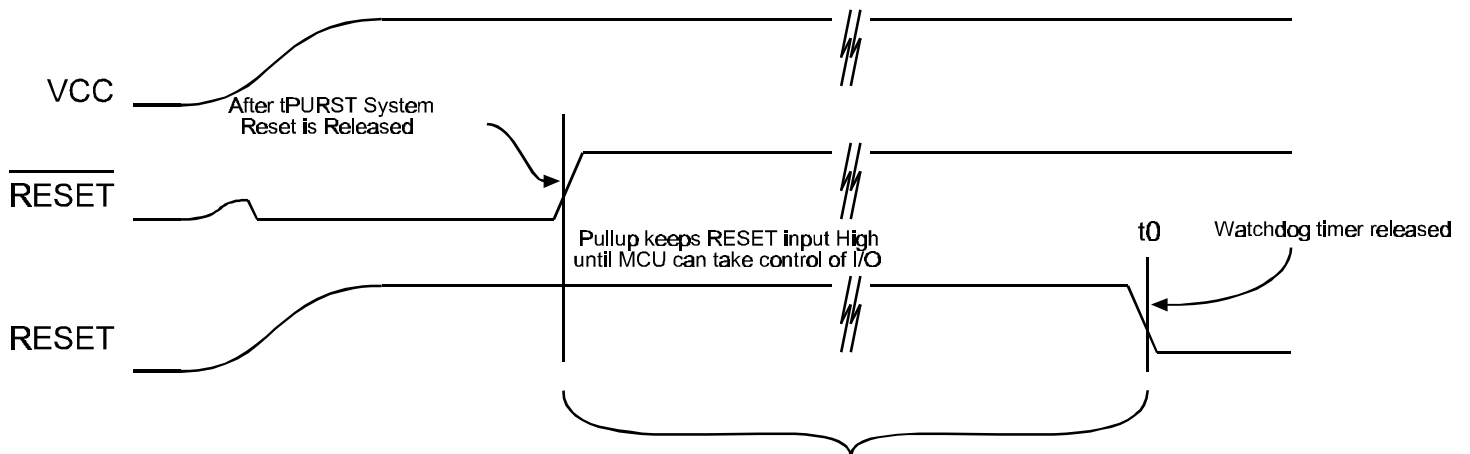
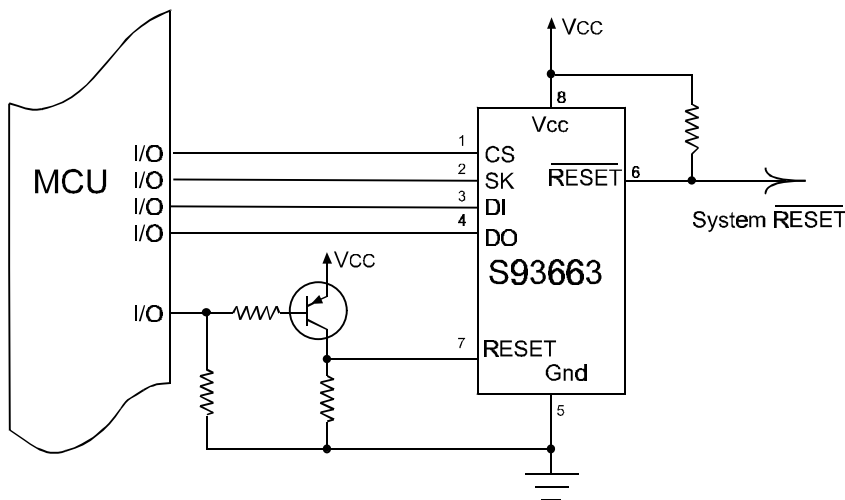
Whenever the S93WD662/663 is held in a reset condition the watchdog timer will be disabled. When a single reset I/O is forced to the reset state the watchdog timer is effectively disabled. The other reset I/O would operate normally providing a clean reset to the rest of the circuitry.

The Circuit

The RESET I/O is used as the system reset, which includes the MCU's, and the RESET I/O is used as the watchdog timer control input. We want to eliminate any possibility of establishing a

continuous reset loop situation; therefore, the circuit is designed to insure the RESET pin is high throughout the power-on and the transition period when the MCU begins to actively drive its I/Os. This implementation allows the system a chance to 'boot up' without the watchdog initiating unwanted resets. Plus, the memory is protected against inadvertent writes, yet it can still be read.

Similarly, it also allows a method for prototyping software in an established hardware design. The MCU can control the action of the watchdog timer or alternatively the timer can be held in reset through the use of a jumper.



As long as the RESETE input is held High
The watchdog timer will be held in reset
The memory will be write protected
The memory can be read after t_{PURST}