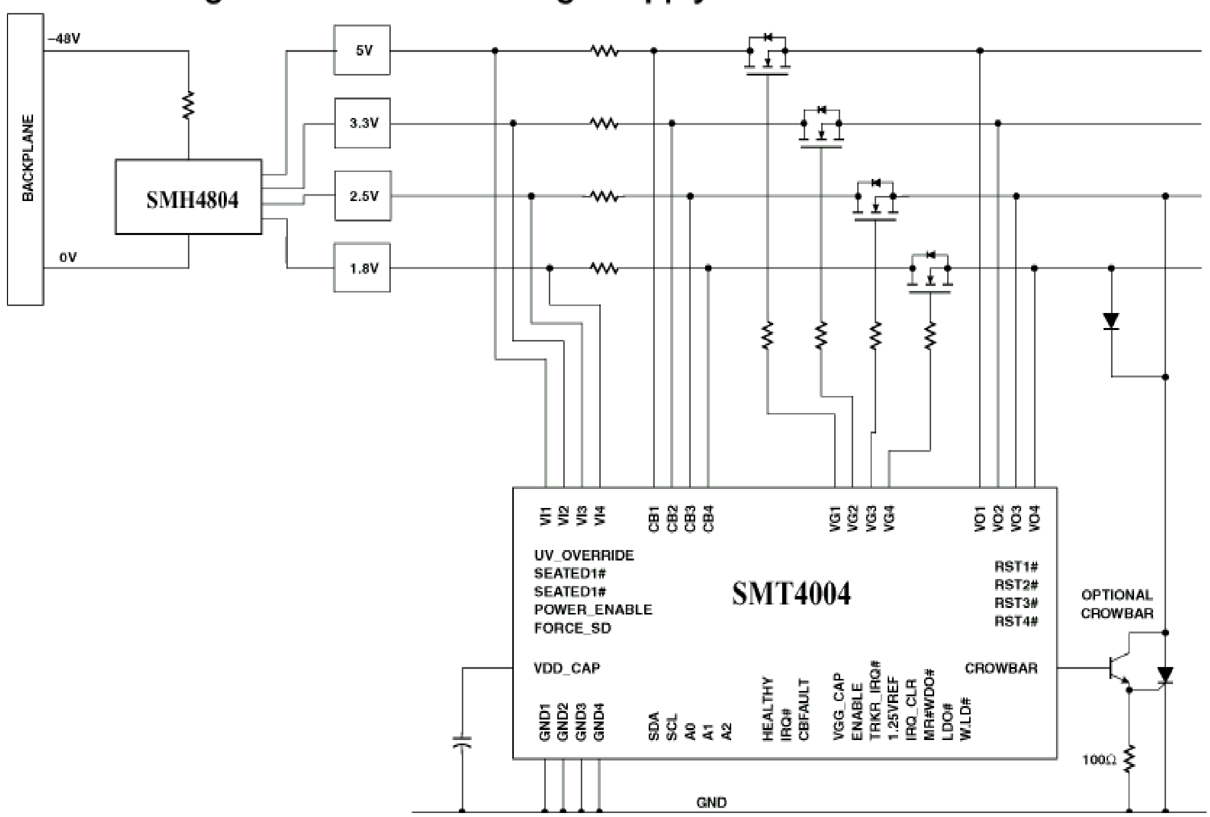
SUMMIT SMT4004 DESIGN GUIDE

SMH4804 Programmable Sequencing Hot Swap Controller +
SMT4004 Programmable Quad Voltage Supply Trakker ™ and Controller



Simplified Application schematic

Terminology

Since many of the applications for the SMT4004 are Hot Swap Implementations, we will use the following convention

- Bus Side – Input Voltage, or supply to the FET
- Card Side – Output voltage or output from the FET
- Tracking – maintaining control of two (or more) supplies during power up/down keeping the differential to a minimum
- GUI – Graphic User Interface, which can be downloaded from www.summitmicro.com

Scope

This document relates to silicon dated 3601(week 36 2001) or later, marked on the top of the device, there may be variances to earlier devices. Contact your local Summit representative if you are unsure.

Principles Of Operation

Power Managers

The SMT4004 Consists of 4 Power Managers(1-4) which control the manner in which 1-4 power supplies can be powered up and powered down either in a standalone system or a Hot Swappable card. Each Power Manager uses an external High Side Driven N Channel FET to control the distribution of the supply to the card side.

The Power Manager also monitors bus and card side voltages as well as the current drawn.

The major benefit of the SMT4004 is that multiple power managers can be connected internally so that the respective supplies are powered up and down at the same time, maintaining less than 100 mV of differential voltage during the entire power up and power down cycle, or supply tracking.

Since the SMT4004 is designed to operate in a wide variety of power supply environments from 2.7V to 5.5V, the device will operate off of any of the Power Manger input voltages which are above 2.7V, and will in fact operate off of the highest potential available at a given time.

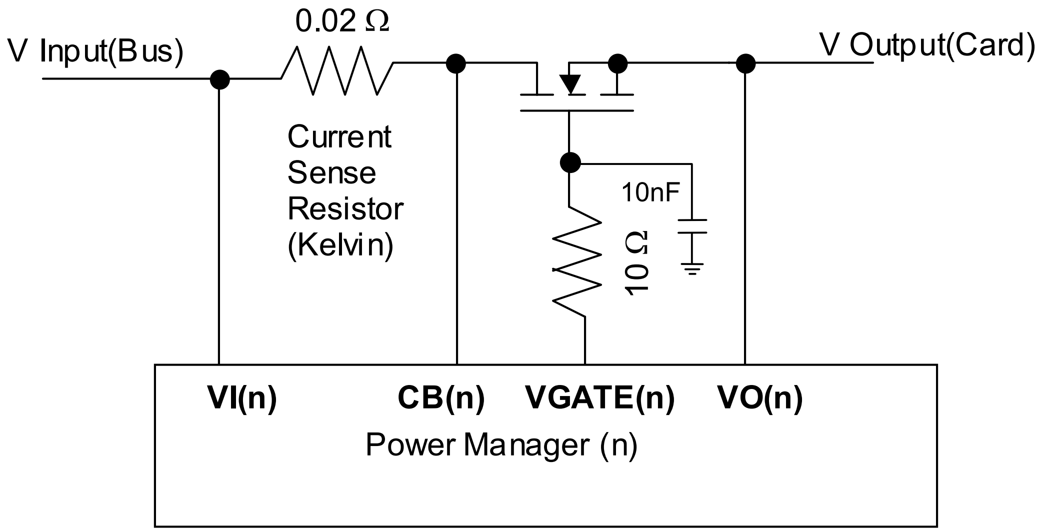


Figure 1 Shows a Simplified Schematic for a Single Power Supply Manager.

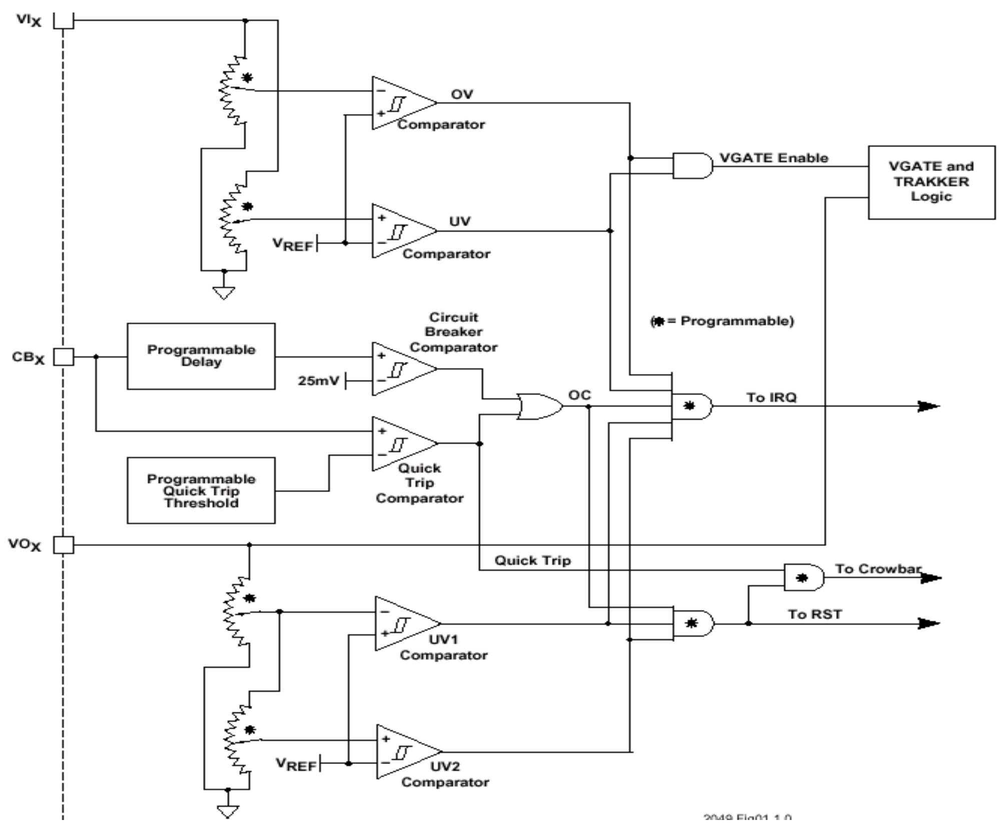


Figure 1b Shows a Simplified internal Schematic for a Single Power Supply Manager.

Power Manager Modes

Each Power Manager can operate in one of two modes, both modes are shown in Fig 2

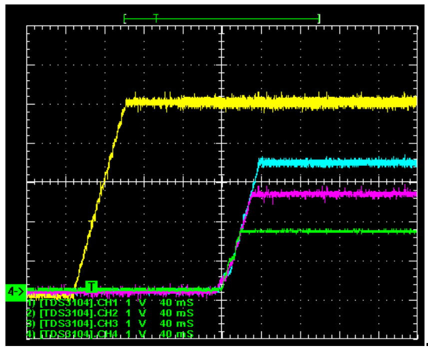


Fig 2. 5V Ch1(Yellow) Softstarting, other channels tracking.

- **Softstart mode**

The Power Manager will be configured to Soft Start the supply, where the **VGATE** will be driven based on a selectable slew rate. All channels programmed to softstart will wait until all input supplies are in range. The SMT4004 will always start softstart supplies before tracking supplies(does not apply to 4 tracking supplies).

The slew rate for the softstart and the tracking is identical, however the rate up and the rate down(note: down only applies to tracking supplies) may be different, as shown in figure 3 below:

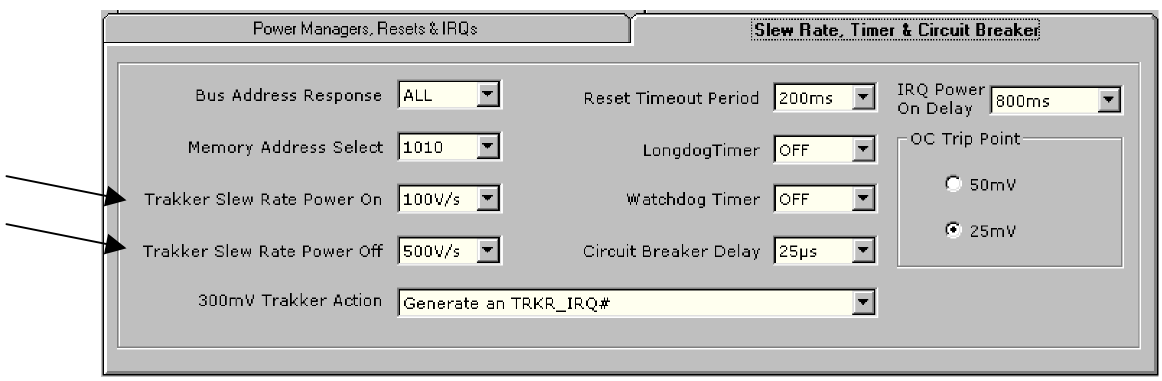


Figure 3 The Slew Rate Menu

All Soft Start Supplies will be powered up once the Control signals are valid and the Input voltage(s) to the specific power manager(s) is(are) within the programmed valid range.

- **Tracking**

The SMT4004 will track supplies up and down, by controlling the supplies against a reference ramp voltage, i.e. the internal slew rate generator. If two or more Power Manager are configured to Track, the SMT4004 will ramp the **VGATE** outputs while monitoring the output voltages(**VO(n**)) to maintain a differential voltage between all tracked voltages of less than 100 mV. If the SMT4004 cannot maintain the <100mV tracking of the output voltages, a Tracker error(TRKn) will be internally generated and the Power Manager can be programmed to either ignore the error or shut down all tracking supplies in the event of an error. Tracking will commence one all Soft Started Supplies are active and the card side voltages(**VI(n**)) of the tracking channels are within the programmed valid range. The time interval between the beginning of the Soft Start Channel turn on and the beginning of the tracking channel turn on will be a factor of the Programmed Slew Rate as well as the loading on the soft started channels **VGATE** outputs.

Note: If a single Power Manager is configured to Track while all others are configured to soft start, the result will be a soft start off all channels, with the tracker configured channel being delayed by some interval.

Configuring Power Managers

Each Power Manager Channel has a number of programmable voltage sensors which to be configured correctly in order to obtain the best results from the SMT4004. Summit recommends that the Card side UV level should always be higher than the board side UV1 level and if UV2 is enabled then it should be below the UV1 level.

Figure 4 shows a correctly configured manager:

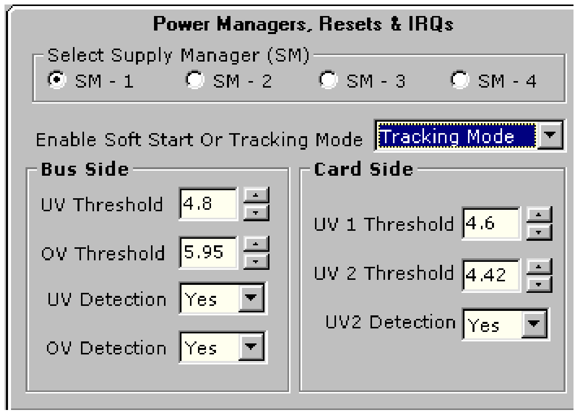


Figure 4 – Power Manager Configuration

Please note a channel will not start (or will be disabled) if the input voltage reaches the OV voltage detection level and the OV detection is enabled. Please note the absolute maximum ratings of the SMT4004.

Similarly if a channel is under the UV threshold on the bus side the power manager will not start.

Enable Signals for Tracking and Softstart

In order for any of the softstart or tracking supplies to be active the following signals must be in a true condition:

Seated 1

Seated 2

Enable

Power ON

In addition there is a software enable control, see section software control, and also some shutdown signals may prevent the supplies from starting, see section shutdown.

- **Seated Pins(Seated 1 and 2)**

These pins should be used as the enable signal if you are using the SMT4004 as a hotswap controller. These pins would normally be connected to the shortest pin on an edge connector.

These pins must be low.

- **Enable Pin**

This signal is provided to control the internal charge pump, which generates the gate drive voltages for the N channel MOSFETS. By disabling this signal the standby current drawn will be reduced. Enable polarity can be programmed active high or low, see Fig 5. Once Seated Pins are active and enable is active you should be able to measure the charge pump voltage across VGG_CAP to GND.

- **PWR _ON Pin**

This signal should be controlled for tracking supplies up and down.

PWR_ON does enable the softstart channel, however it does **not** disable any softstarting channels.

PWR_ON polarity can be programmed active high or low See Fig 5

This pin is not debounced and is not recommended as the control signal for hotswapping(see Seated).

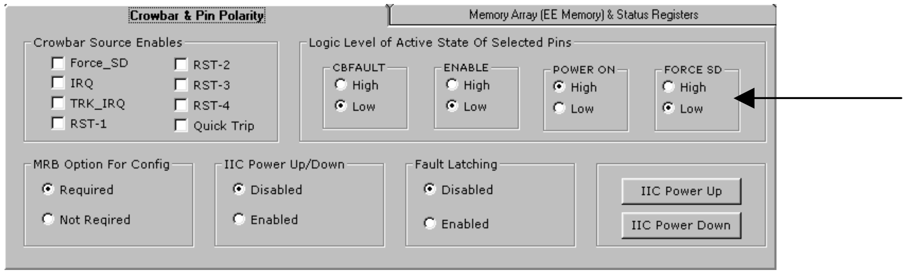
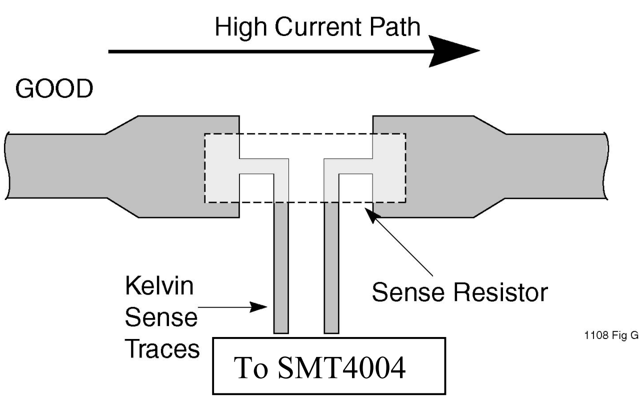


Figure 5 Pin Polarity Menu

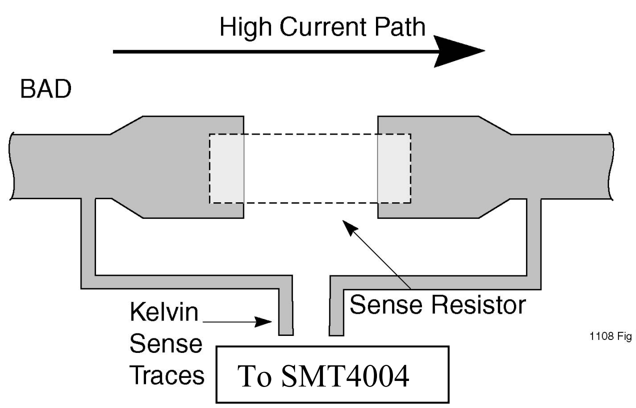
Current Sensors and Circuit Breakers.

The circuit breaker has two modes of operation, normal and Quicktrip, however both rely on the board layout of the physical sense resistor.

In Fig 1 we showed the small sense resistor in series with the current path to the FET, this sense resistor and the circuit board layout associated with it. The majority of problems with over current come from back layout of the sense resistor, which should be treated, like a Kelvin sense or 4 terminal resistor.



Correct Kelvin connection PCB layout



Incorrect Kelvin connection PCB layout

The Circuit Breaker or Overcurrent Sensors on each Power Manager have two modes of operation. The first of these is the normal circuit breaker, which can be programmed to detect either a 25 or 50 mvolt drop across the sense resistor.

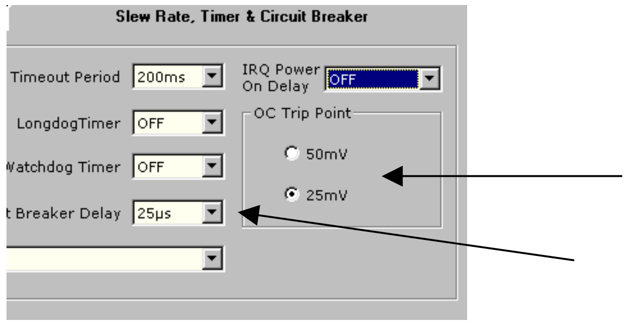
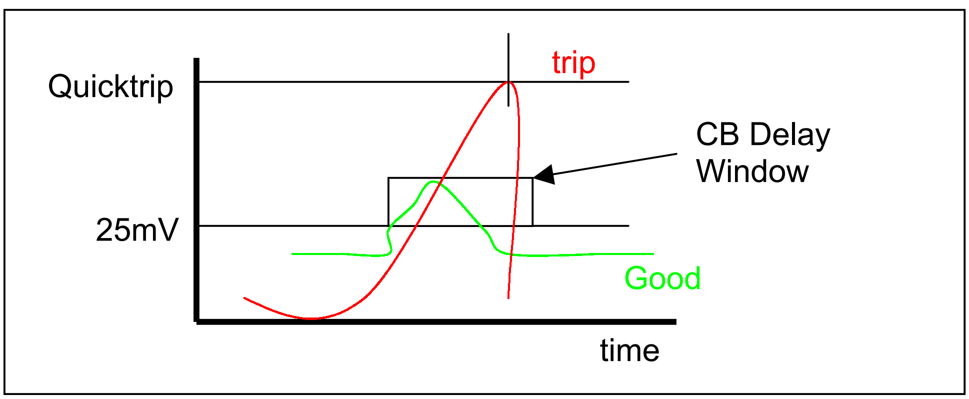


Figure 6. Circuit Breaker Configuration

Therefore the value for the sense resistor is very easy to calculate, i.e. for an absolute maximum 4 amp supply at 25mV the sense resistor would be 25mV / 4 or 6.25mOhms. Engineers should allow sufficient room when calculating this value to allow for noise and any addition tracking errors.

The normal mode of operation allows a programmable filter to be used to insure that the programmed voltage drop is seen for a long enough period(25, 50, 100, 200 µs) to prevent spurious shutdowns of the channel. This circuit breaker delay time is also shown in Figure 6 and is one value for all channels.

However in the event of a major short circuit a time delay may allow the current to grow too large too quickly, so the SMT4004 has a second level which acts immediately without ant time delay, this is called the Quicktrip level and is a multiple of the normal voltage drop across the sense resistor.



Note each power manager has its own quick trip level , these may be set at OFF, 75mV 100mV or 150mV, the level setting for these is shown in Fig 7

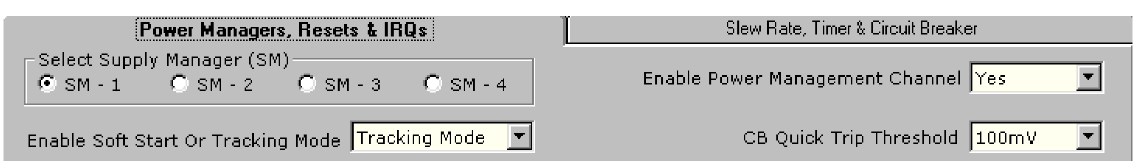


Fig 7 – Quick Trip Level Setting

In both modes of operation(normal and quicktrip) in the event of an over current condition the N Channel MOSFET gate drive is disabled and driven to ground immediately, the CB Fault output is activated(active sense can be programmed).
A global enable for current sensors is also provided, this is for designs, which do not require current sensing because the supply feeding the SMT4004 is current limited. This can also be used during debug if a supply is thought to be in overcurrent (current limited feed is recommended).

System Control

The SMT4004 featured several signals which allow it to control the target system based upon the status of the power supplies.

Each Power Manager has a Reset Output(**RST#1-4**) to generate Reset conditions to the downstream circuitry operating off of the controlled voltage. The source of the Rest condition is programmable to include UV, OV and CB in any combination for the specific Power Manager. The Reset Interval is globally programmable. Multiple Resets can be combined by external wire ANDING of the desired outputs. Figure 8 shows the different settings for the RESET output from each of the Power Managers. Any combination of the Output Voltage undervoltage sensors(UV1 and U2), the TRACKER ERROR or Circuit Breaker for each channel can be configured to drive the appropriate RESET output.

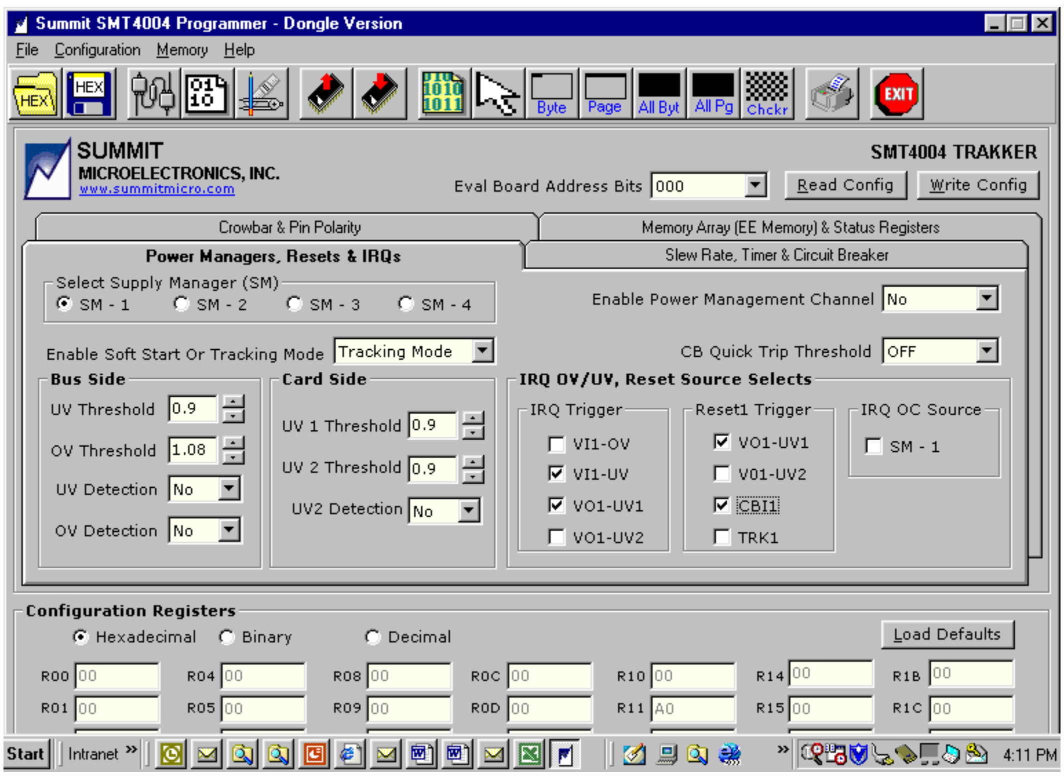


Figure 8 Reset and IRQ Configuring

In many cases, the system will need to be informed of power supply issues rather than being put into Reset. The SMT4004 has a flexible Interrupt Generation Architecture to facilitate such as system alert. The **IRQ#** output can be driven as a function of the UV, OV, UV1, UV2, CB from each of the Power Managers as well as an internal Tracking error(TRK(n)). Up to 20 sources for the IRQ can be independently enabled. The **IRQ#** is latched, and can only be cleared by asserting the **IRQ_CLR#** signal or by removing power to the SMT4004.

Note: Any IRQs generated prior to or during power down remain latched; i.e., IRQ# is low, until the voltage on the VDD_CAP node falls below 0.5V.

Figure 8 shows that for each channel, any combination of the Input Undervoltage and Overvoltage sensors(UV OV) or the Output side Undervoltage sensors(UV1, UV2) can be used to generate an IRQ or an overcurrent condition, either Quick Trip or Normal.

TRKR_IRQ is a second interrupt which can be generated from the Tracker Error signals from each of the Power Managers. It is also latched and can only be cleared with the **IRQ_CLR#.**

Shutdown, Crowbar

Forced Shutdown

Assertion of the **FORCE_SD** (Forced Shutdown) will cause all **VGATE** outputs to be driven to GND, turning off all of the supplies regardless of whether they are configures to Soft Start or to Track. When the N channel MOSFETS are disabled the high impedance created between input and output means that the output gate voltages will decay to ground dependant upon the bulk capacitance and the circuit load(i.e. there is no tracking).

The active state of Force Shutdown can be programmed, see Fig5

Crowbar

The **CROWBAR** output is used to crowbar all output voltages through the use of an external SCR. The Crowbar condition can be programmed to be internally derived form any combination of **IRQ#**, **TRK_IRQ#**, **RST#1-4** or a Quick Trip condition. A crowbar condition will also cause all Power Mangers Gate voltages to be driven to Ground

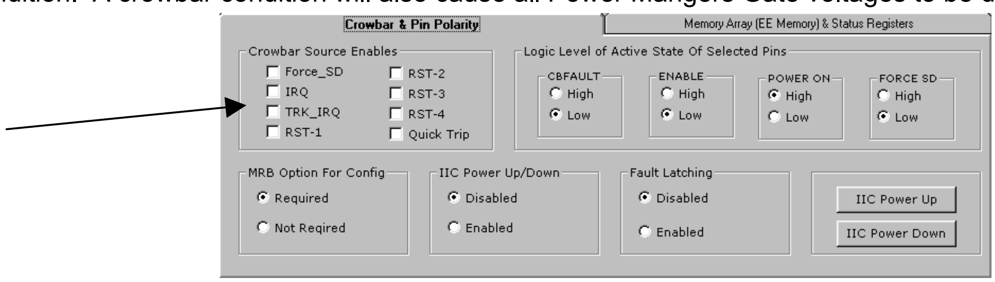


FIGURE 9 Crowbar Source Selection

Figure 9 shows the selection criteria for generating a Crowbar Output. IRQ, TRK_IRQ, RST1-4 and Quick Trip all have additional configuration options for their control and derivation. Force_SD is an input, which can be configured either as active high or active low.

Power Supply Status Reporting

The SMT4004 contains advanced features to allow the system to query the status of the Power Supplies that the SMT4004 is controlling.

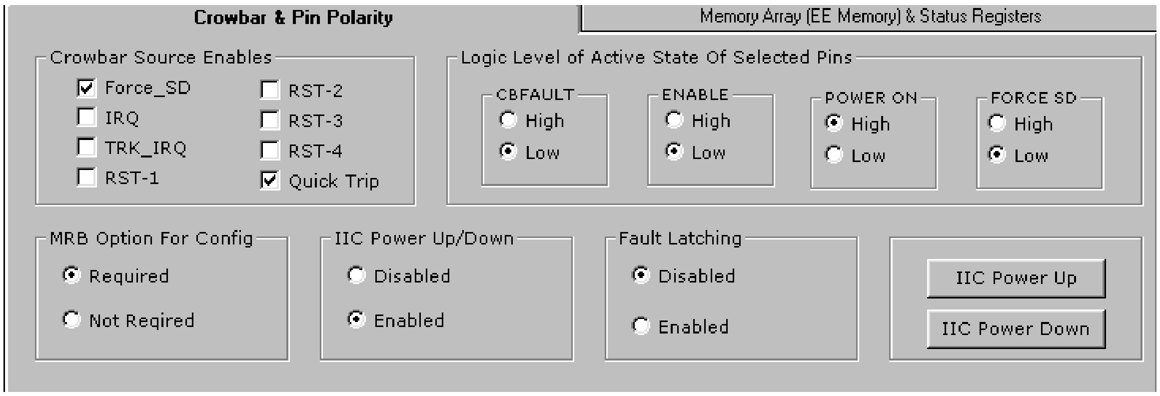
The **HEALTHY#** signal is used to indicate that all supplies are operating within their programmed valid ranges.

The **CBFAULT#(**Circuit Breaker Fault) is driven active whenever an overcurrent situation is detected.

The SMT4004 also features a status register which can be queried over the I^2C bus. The status register will report the current status of any of the 20 interrupt generating conditions as well as the 4 Power Manager Tracker Errors.

SMT4004 Software Control

The SMT4004 Power Managers can be controlled via the I^2C bus, first the SMT4004 must be programmed to work in this mode, by changing the configuration registers.



Once the I^2C power up/down mode has been enabled, the SMT4004 will not enable any channels from power up(including softstart and tracked). Once a power IIC message is received, the SMT4004 will enable all channels. Softstarts will be activated before tracked channels as with the PWR_ON pin. See figure 10 below:

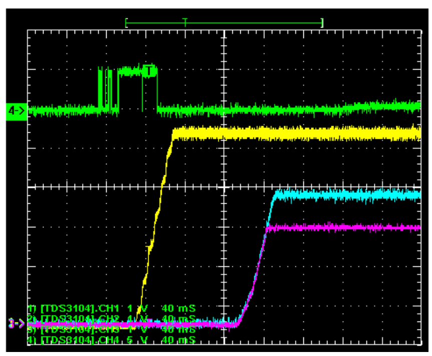


Fig 10 I^2C Power Up Command, Initial start up

The power down command, this will only power off the tracked channels(the same as PWR_ON pin)

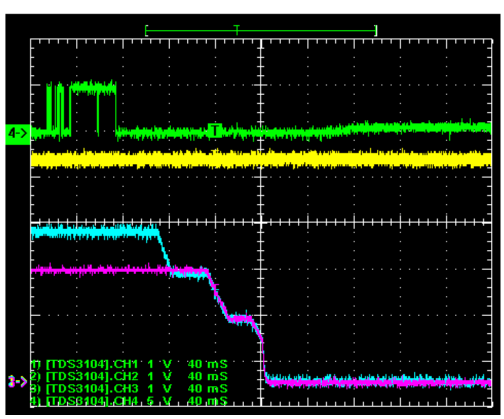


Fig 11 Power Down Command, note Softstart 5V(yellow) remains on

Other Goodies

The SMT4004 features a 1.25V precision reference(**1.25Vref**) voltage output to be used to build additional analog functions external to the device.

An I^2C bus is used to communicate with the SMT4004 during configuration as well as to access the internal 4K of General Purpose E2PROM. Status Reporting and Software Control is also accomplished over this bus using the **SCL** and **SDA** pins. Multiple SMT4004s can be put on the same I^2C bus, using the address inputs **A0, A1,A2** to select between on of up to 8 devices.

The **UV_OVERIDE** input is a test mode and should not be used by the end user. It disables all UV monitors.

Timers .

WDO#: The watchdog timer output is an active-low open-drain output that can be wire-ORed with other open-drain signals. The watchdog timer is generally programmed to generate an output at a time interval shorter than the longdog timer. The WatchDog functions like a re-triggerable one-shot with a low to high transition on the WLDI acting as the input. Since the WDO# output is open drain, it may require a pullup resistor.

LDO#: The longdog timer output is an active-low open-drain output that can be wire-ORed with other open-drain signals. The longdog timer is generally programmed to generate an output at a time interval longer than the watchdog timer. The LongDog functions as a 50% duty cycle oscillator with the WLDI, MR# inputs and any RST# output (all RST# outputs or-ed together internally) acting as trigger inputs when they transition from low to high. Asserting the WLDI restarts the LongDog timer to the beginning of the oscillator cycle (high) regardless of the state of the LDO# output at the time the assertion occurred.

WLDI: Watchdog and longdog timer reset input. A low-to-high transition on this pin will reset both the watchdog timer and the longdog timer. Generally, the longdog will be programmed to time out sometime after the watchdog. As an example, the WDO# output could be used to generate a warning interrupt and the LDO# output could be tied to a system reset line. Both timers can be turned off, facilitating system debug and also allowing operating systems to ‘boot up’ and configure themselves without interrupts or resets. The WLDI and MR# inputs must remain high for at least 100nS.

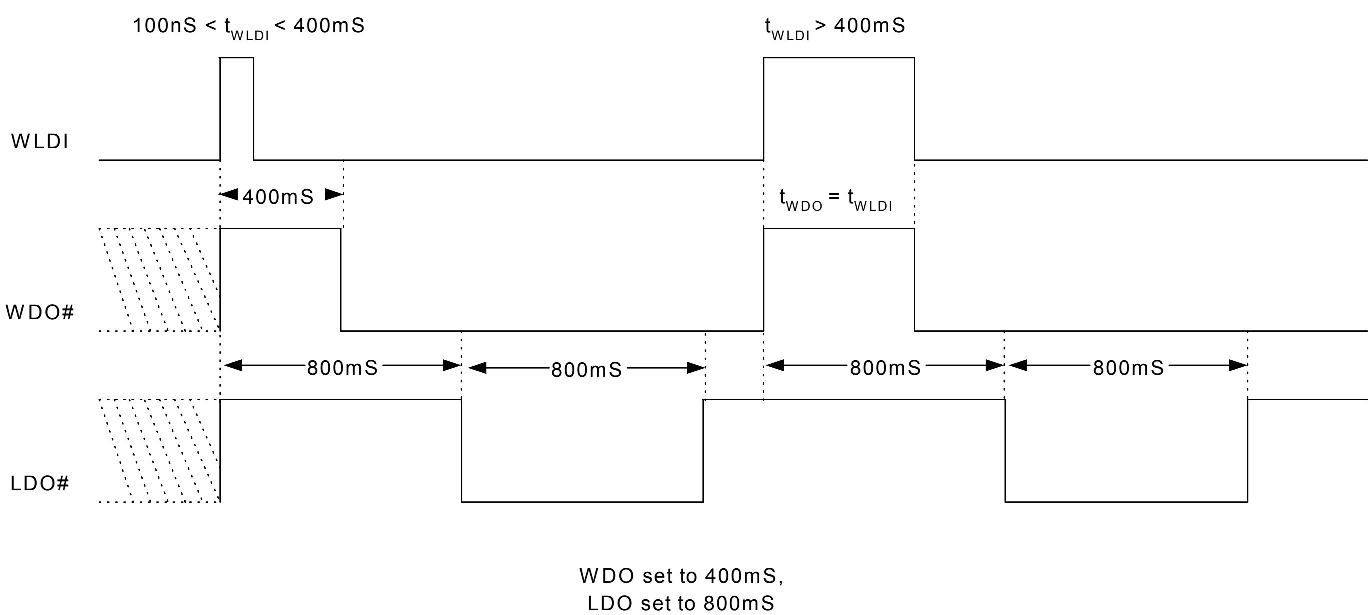


Figure 12 – WLDI, WDO# and LDO# timing diagram.

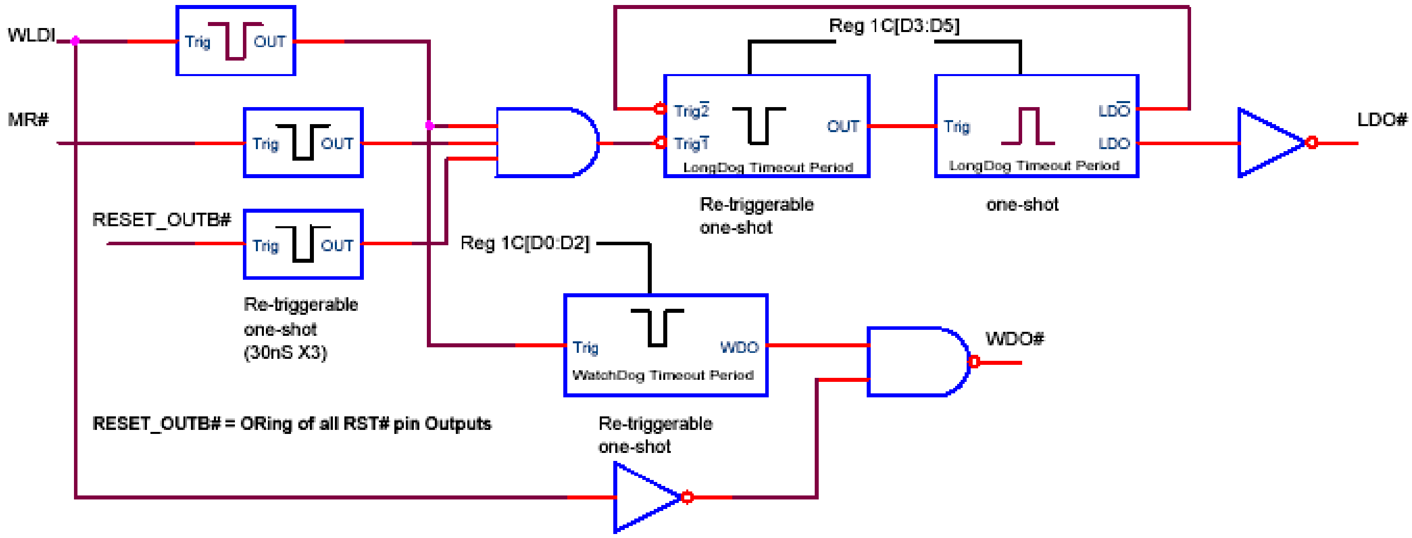


Figure 13 – WLDI, WDO# and LDO# internal block diagram.

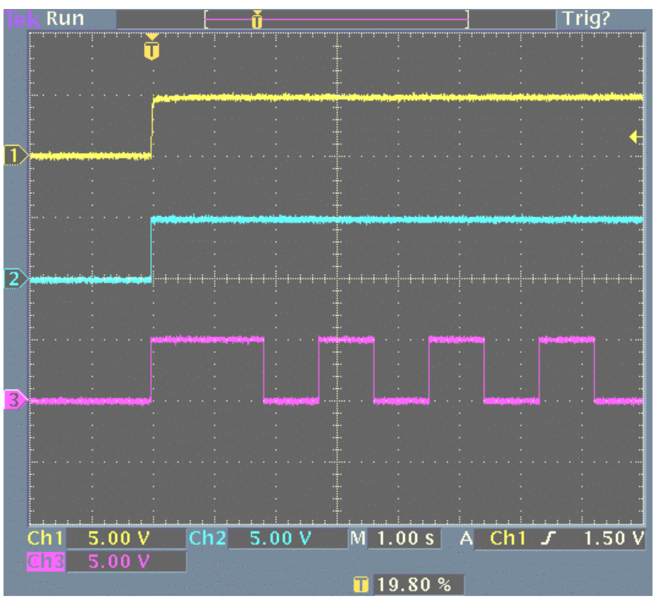


Figure 14 - WDO = 400mS(Blue), LDO = 800mS(Purple), WLDI = High, PWR_ON(Yellow)

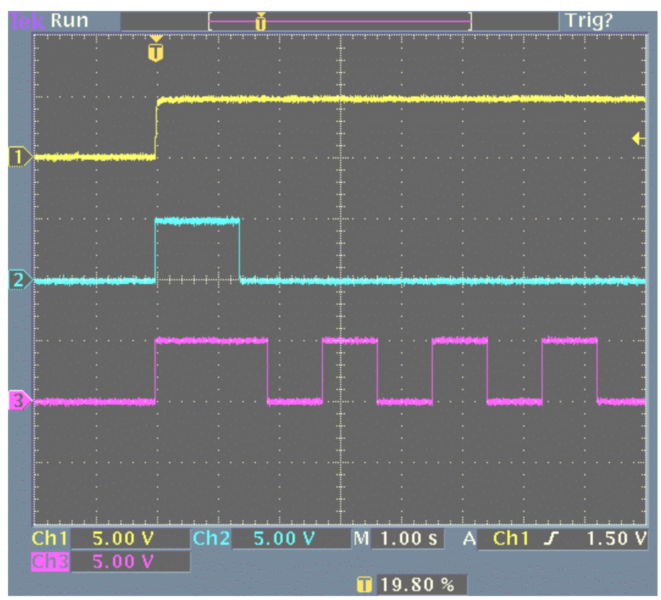


Figure 15 - WDO = 400mS(Blue), LDO = 800mS(Purple), WLDI = Low, PWR_ON(Yellow)

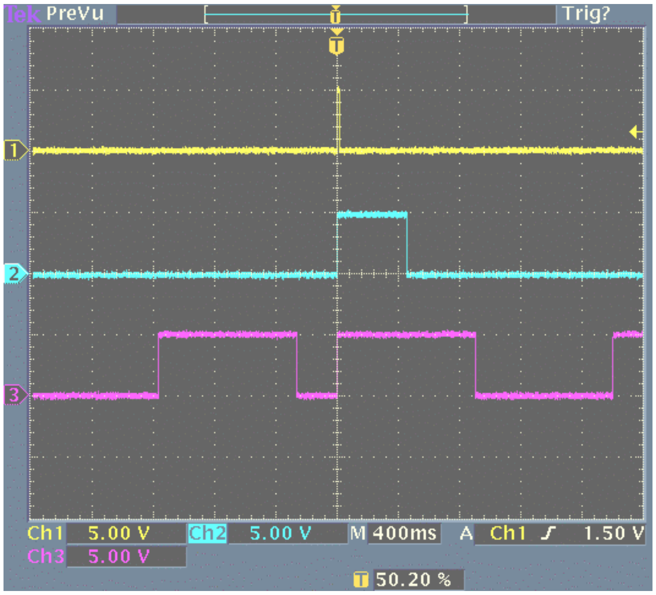


Figure 16 - WDO = 400mS(Blue), LDO = 800mS(Purple), WLDI = 500Hz, 20% Duty Cycle, Single-Pulse (Yellow)

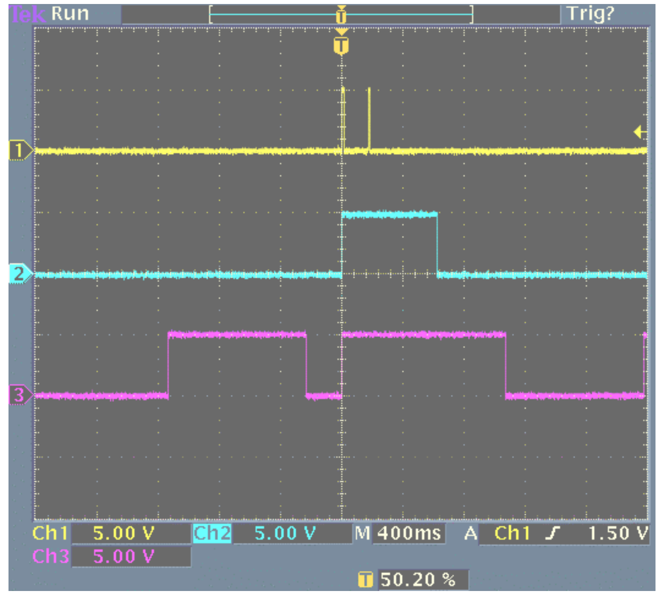


Figure 17 - WDO = 400mS(Blue), LDO = 800mS(Purple), WLDI = 500Hz, 20% Duty Cycle, Double-Pulse (Yellow)

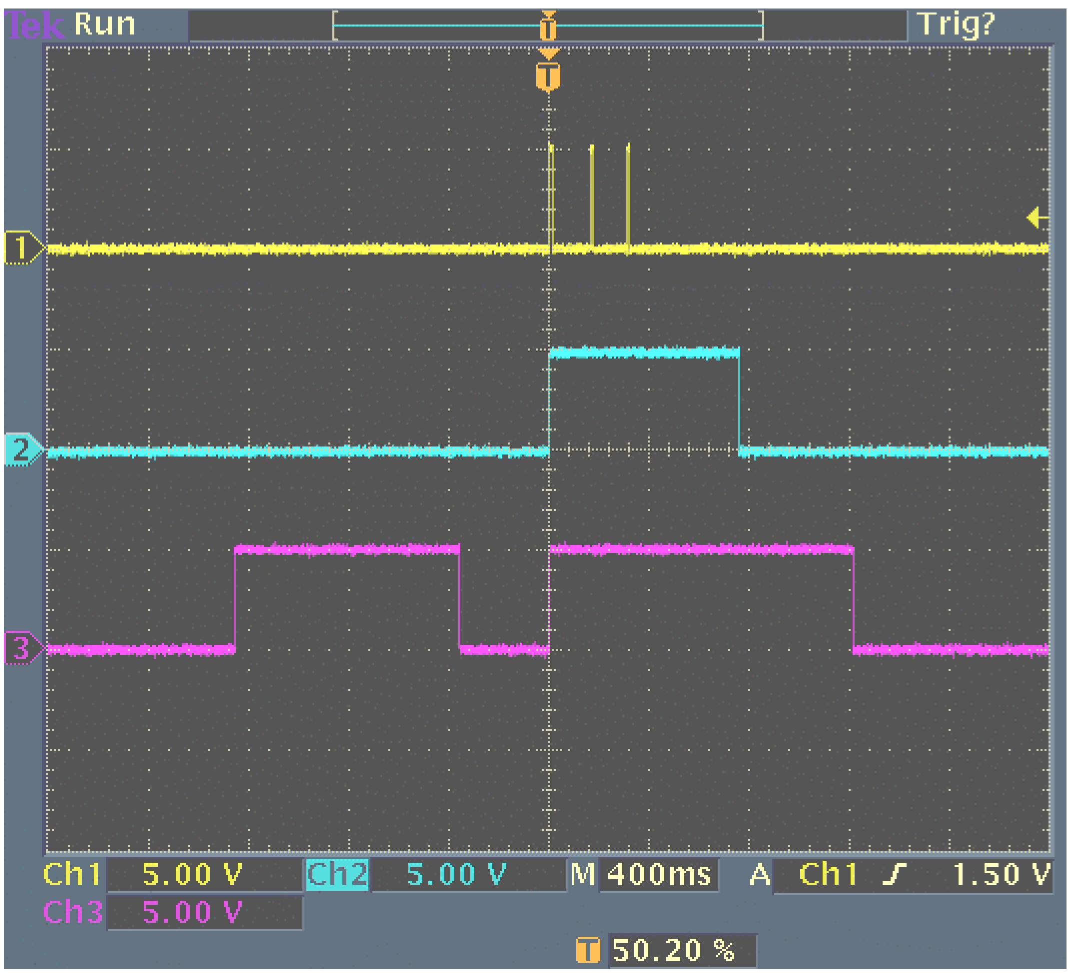


Figure 18 - WDO = 400mS(Blue), LDO = 800mS(Purple), WLDI = 500Hz, 20% Duty Cycle, Triple-Pulse (Yellow)

Table 1 Pin Descriptions.

Pin Number	Name	Description	Input or Output	Type	Usual Connection	Programmable Options
1	LDO#	Long Dog Timer Output	O	Digital, Open Drain, Active Low	Wire AND with Reset or IRQ	Programmable Interval, Off, 800, 1600, 3200, 6400 ms
2	WDO#	Watchdog Timer Output	O	Digital, Open Drain, Active Low	Wire AND with Reset or IRQ	Programmable Interval, Off, 400, 800, 1600,3200 ms
3	Crowbar	Crowbar Pulse Output	O	Digital, Totem Pole, Active High, 5 µs Pulse	Drives SCR Control to Crowbar Output Voltages	Programmable Source FORCE_SD, IRQ#, TRK_IRQ#, RST1-4#, Quick Trip
4	1.25V Ref	Reference Voltage Output	O		A 0.1uF, high-quality (low-ESR) capacitor **must** be connected from this pin directly to the SMT4004 ground pins	
5	MR#	Manual Reset Input	I	Digital, Active Low, Internal 100K Pull up	Must be pulled low when writing to the SMT4004. Refer to Table 3 for proper operation	Is not required if I^{2}C Power On/Off is enabled
6	IRQ_CLR#	Clear IRQ	I	Digital, Active Low, Internal 100K Pull Up		
7	IRQ#	Interrupt Output	O	Digital, Open Drain, Active Low, Latched	Drives Interrupt Request	Programmable Source (Power Manager 1-4) TRK, OV, UV, IV1, UV2, CB Programmable Power On Delay (Global) 0, 200, 400, 800, 1600 ms
8	PGND	Power Ground	I		Connected to Input Ground	
9	TRKR_IRQ#	Trakker Interrupt	O	Digital, Open Drain, Active Low, Latched	Drive Interrupt Request	
10	SEATED1#	Card Seated Detector1	I	Digital, Active Low, Internal 100K Pull Up	Usually Connected to Ground on Backplane	
11	SEATED2#	Card Seated Detector2	I	Digital, Active Low, Internal 100K Pull Up	Usually Connected to Ground on Backplane	
12	UV_Override	Undervoltage Sensor Override	I	Digital, Active High, Internal 100K Pull Up	Usually Connected to Ground	
13	RST1#	Reset 1	O	Digital, Open Drain, Active Low, Gated	Connected to System Resets	Programmable Source (Power Manager 1-4) UV1, UV2, CBI, Programmable Reset Interval (Global) 25, 50, 100, 200 ms
14	RST2#	Reset 2	O	Digital, Open Drain, Active Low, Gated	Connected to System Resets	
15	RST3#	Reset3	O	Digital, Open Drain, Active Low, Gated	Connected to System Resets	
16	RST4#	Reset4	O	Digital, Open Drain, Active Low, Gated	Connected to System Resets	
17	PGND	Power Ground	I		Connected to Input Ground	
18	DGND	Digital Ground	I		Connected to Input Ground	
19	AGND	Analog Ground	I		Connected to Input Ground	

Table 1 Pin Descriptions Continued.

Pin Number	Name	Description	Input or Output	Type	Usual Connection	Programmable Options
20	VO1	Power Manager 1 Output Voltage(CARD)	I	Analog, Voltage Sensor	Connected to the output(drain) side of the FET for Power Manager 1	Two Programmable Undervoltage Detectors, (Power Manager 1-4) UV1, .9-6.0 Volts (Power Manager 1-4) UV2 UV1 + Offset
21	VO2	Power Manager 2 Output Voltage(CARD)	I	Analog, Voltage Sensor	Connected to the output(drain) side of the FET for Power Manager 2	
22	VO3	Power Manager 3 Output Voltage(CARD)	I	Analog, Voltage Sensor	Connected to the output(drain) side of the FET for Power Manager 3	
23	VO4	Power Manager 4 Output Voltage(CARD)	I	Analog, Voltage Sensor	Connected to the output(drain) side of the FET for Power Manager 4	
24	ENABLE	Charge Pump Enable	I	Digital, Programmable Polarity, Internal 100K Pull Up	Must Be active for Power On, Asserting During operation will Cause Tracked Power Managers to Track Down	Programmable, Active High or Low
25	CBFAULT	Circuit Breaker Fault	O	Digital, Totem Pole, Configurable Polarity		Programmable, Active High or Low
26	Healthy#	Power Supplies Healthy	O	Digital, Open Drain, Active Low, Latched or Gated		
27	FORCE_SD	Force Shutdown	I	Digital, Programmable Polarity, Internal 100K Pull Up	When Asserted, Causes all VGATE outputs to be driven to ground	Programmable, Active High or Low
28	VGG_CAP	Decoupling Capacitor for VGG	O	Analog	Connect to ground with a capacitor of (0.1uF-1uF). Use 1uF for slow-rising input voltages.	
29	VGATE4	High Side Driver Output for FET Gate, Power Manager 4	O	Analog, 0-14 Volts	Connected through Series Resistor to the Gate input of FET for Power Manager 4. Place a 10nF (25V) from VGATE output to GND.	Programmable Slew Rate on Power On(Global) 100, 250, 500, 1000 V/Sec Programmable Slew Rate on Power Down (Global) 100, 250, 500 1000 V/Sec
30	VGATE3	High Side Driver Output for FET Gate, Power Manager 3	O	Analog, 0-14 Volts	Connected through Series Resistor to the Gate input of FET for Power Manager 3. Place a 10nF (25v) from VGATE output to GND.	
31	VGATE2	High Side Driver Output for FET Gate, Power Manager 2	O	Analog, 0-14 Volts	Connected through Series Resistor to the Gate input of FET for Power Manager 2. Place a 10nF (25V) from VGATE output to GND.	
32	VGATE1	High Side Driver Output for FET Gate, Power Manager 1	O	Analog, 0-14 Volts	Connected through Series Resistor to the Gate input of FET for Power Manager 1. Place a 10nF (25V) from VGATE output to GND.	
33	PWR_ON	Power On	I	Digital, Programmable Polarity, Internal 100K Pull Up		Programmable, Active High or Low

Table 1 Pin Descriptions Continued.

Pin Number	Name	Description	Input or Output	Type	Usual Connection	Programmable Options
34	CB4	Circuit Breaker Sensor Power Manager 4	I	Analog, Voltage Sensor	Connect to the Output Side of the Current Sense Resistor for Power Manager (n) If Overcurrent sensing for a particular Power Manager is not used, connect to VI(n) for Power Manager (n)	Programmable Delay(Global) 25, 50, 100 and 200 µs Programmable Quick Trip Threshold (Power Manager 1-4) Off, 75, 100, 150 mV
35	CB3	Circuit Breaker Sensor Power Manager 3	I	Analog, Voltage Sensor		
36	CB2	Circuit Breaker Sensor Power Manager 2	I	Analog, Voltage Sensor		
37	CB1	Circuit Breaker Sensor Power Manager 1	I	Analog, Voltage Sensor		
38	VI4	Input Voltage Sensor Power Manager 4(Bus)	I	Analog, Voltage Sensor	Connect to Input Voltage 4, Input Side of Current Sense Resistor(If Used)	Programmable Undervoltage Sensor UV (Power Manager 1-4) .9 – 6.0 Volts Programmable Overvoltage Sensor OV UV + Offset
39	VI3	Input Voltage Sensor Power Manager 3(Bus)	I	Analog, Voltage Sensor	Connect to Input Voltage 3, Input Side of Current Sense Resistor(If Used)	
40	VI2	Input Voltage Sensor Power Manager 2(Bus)	I	Analog, Voltage Sensor	Connect to Input Voltage 2, Input Side of Current Sense Resistor(If Used)	
41	VI1	Input Voltage Sensor Power Manager 1(Bus)	I	Analog, Voltage Sensor	Connect to Input Voltage 1, Input Side of Current Sense Resistor(If Used)	
42	VDD_CAP		O	Analog, This node generates the internal VDD from the highest voltage on the VI1-VI4 input pins	Connect a 10uF capacitor from this pin directly to the SMT4004 ground pins.	
43	A0	I^2C Device Address Input 0	I	Digital, Internal 100K Pull Up		
44	A1	I^2C Device Address Input 1	I	Digital, Internal 100K Pull Up		
45	A2	I^2C Device Address Input 2	II	Digital, Internal 100K Pull Up		
46	SDA	I^2C Bidirectional Data	I/O	Digital, Internal 100K Pull Up	I^2C Bus	
47	SCL	I^2C Clock	I	Digital, Internal 100K Pull Up	I^2C Bus	
48	WLDI	Watch Dog and Long Dog Timer Reset	I	Digital, Internal 100K Pull Up		

POWER, GROUNDING & BYPASSING

1. Connect the Input(Bus) Side Voltages to Appropriate **VI1-VI4**

   Note: The highest voltage powers the SMT4004 (**VDD_CAP**).

2. Bypass all input pins (**VI1-VI4**) to ground with bulk capacitors (≥4.7uF) in parallel with low ESR capacitors (0.01uF-0.1uF). Locate the components nearby the SMT4004 making all connections as short as possible
3. Connect all ground pins together at the package using the shortest allowable connections and widest trace widths.
4. Make a single connection from the Output Side(Card) to the SMT4004 ground pins (pins 8, 17-19) and a single connection to the Bus Side(Input) Ground
5. Connect a low ESR 0.1uF ceramic or film capacitor directly from $\mathbf{1.25V_{REF}}$ (pin 4) to the SMT4004 ground. Place the capacitor as near the SMT4004 as possible.
6. Filter the **VGG_CAP** pin to ground with a capacitor of (0.1uF-1uF). Use 1uF for slow-rising input voltages.
7. Connect all managed output voltages from as near the system load as possible directly to the output sense pins (**VO1-VO4)**. Be certain the output sense pin connections correspond to the managed input (**VI1 with VO1, etc.**).
8. Insure that Proper Layout Guidelines for Kelvin Sense Resistors has been used. **90% of all problems with Overcurrent sensing are Layout related issues**
9. During hot swap events, the gate capacitors prevent transients on the outputs due to the MOSFETs turning on/off. The VGATE capacitors are needed to clamp the MOSFETs' gates off until the SMT4004 has reached its turn-on threshold and can hold the VGATE outputs low. The 10nF, 25V VGATE capacitors take about 10uS to charge, which is sufficient time for the SMT4004's internal circuitry to reach approximately 700mV and hold the VGATE outputs low. When the input supply voltages turn-on quickly, the Drain capacitance of the external MOSFETs can couple charge to the Gate and turn it on if the VGATE capacitors are not clamping the Gate at or about ground potential. This prevents latch-up of the processor/ASICs.
10. The VGATE capacitors improve the tracking performance by adding a necessary added capacitance to the new generation of low gate charge, higher gain MOSFETs with logic-level or lower turn-on thresholds. The capacitors prevent the MOSFET from prematurely turning fully on and slowly ramping off.

CONTROL INPUT PINS (L ≤ 0.3XVDD_CAP, H ≥ 0.7XVDD_CAP)

Caution! The SMT4004 will not function until all Control Input logic-levels match the internally programmed states! (See Figure 1 "Summit Micro's SMT4004 GUI program").

SEATED1#, SEATED2#: Although not user-configurable, both pins must be grounded before the user-configurable control inputs have any influence on the SMT4004!

ENABLE: When asserted puts the SMH4004 in sleep-mode and disables the charge pump.

PWR_ON: When asserted Power-on or Power-off management is initiated. When de-asserted, the charge pump is disabled.

FORCE_SD: When asserted pulls all VGATE outputs to ground.

Table 2: SMT4004 Power-Up/Down Truth Table (all inputs are stable and within the bus-side UV/OV limits)

Notes: X=Don't Care, L=Logic Low, H=Logic High,
TRUE = Programmed Polarity and Input Polarity Match
FALSE = Programmed Polarity and Input Polarity Do Not Match

POWER UP				
SEATED1#, #2 (10, 11)	***FORCE_SD (27)***	***ENABLE (24)***	***PWR_ON (33)***	**Action**
	Pin	Pin	Pin	
X, H or H, X	X	X	X	None, charge pump is disabled, all VGATE outputs pulled to ground.
X, X	TRUE	X	X	None, all VGATE outputs pulled to ground.
L, L	X	FALSE	X	None, all VGATE outputs pulled to ground.
L, L	FALSE	TRUE	FALSE	VGATE outputs ready, charge pump enabled, Soft Start Channels Power On
L, L	FALSE	TRUE	TRUE	VGATE outputs enabled, SMT4004 Soft-Starts then Tracks Outputs.
POWER DOWN				
SEATED1#, #2 (10, 11)	***FORCE_SD (27)***	***ENABLE (24)***	***PWR_ON (33)***	**Action**
	Pin	Pin	Pin	
H, X or X, H	X	X	X	Charge pump is disabled and all VGATES are pulled to ground.
L, L	TRUE	TRUE	X	All VGATES are pulled to ground; Charge Pump Remains Running
L, L	X	FALSE	X	Charge pump is disabled; all outputs will shutdown.
L, L	FALSE	TRUE	FALSE	All channels selected for Tracking will track down.

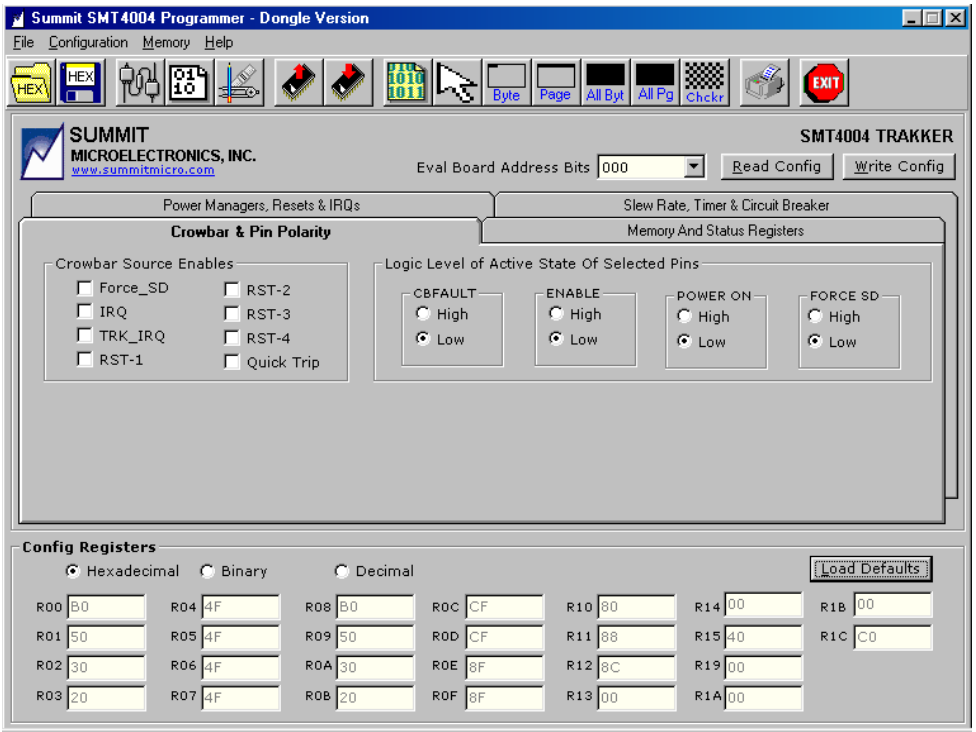


Figure 19: 'Crowbar & Pin Polarity' Tab of the SMT4004 GUI Program

FAULT ALERT OUTPUT PINS

Table 3: SMT4004 Fault Alert Output Truth Table

SMT4004 Fault Output Pins Truth Table		
Fault Pin, (pin #)	**Fault Sources (see Figures 1 & 2)**	**Comments**
RESET1#-4# (13-16)	Card-side UV1 or UV2, Trakker error and Overcurrent.	Open-drain, active low gated (unlatched) outputs. User-configurable delay time upon fault is removal.
IRQ# (7)	Bus-side UV or OV, Card-side UV1 or UV2 and Overcurrent.	Open-drain, active low latched output. User-configurable delay time upon fault is removal (on power-up only).
TRKR_IRQ# (9)	Excessive voltage differentials between tracked channels.	Open-drain, active low latched output.
HEALTHY# (26)	Any Reset (RST1#-RST4#), IRQ#, TRKR_IRQ# or CBFAULT	Open-drain, active low, gated or latched (by IRQ# or TRK_IRQ#) outputs.
CBFAULT (25)	An overcurrent on any channel set for current sensing.	Totem-pole, (user-configurable asserted-state) output. User-configurable delay time upon fault for noise filtering and to prevent nuisance tripping.
CROWBAR (3)	Can be enabled (triggered) by: RST#1-RST#4, IRQ#, TRKR_IRQ#, Quick-Trip Overcurrent or asserting the FORCE_SD pin.	Totem-pole, active-high 5uS pulse. High-level = VDD_CAP node voltage.

FAULT ALERT & TROUBLESHOOTING INPUT PINS (L = 0.3XVDD_CAP, H = 0.7XVDD_CAP)

Table 4: SMT4004 Fault Alert & Troubleshooting Input Truth Table

SMT4004 Fault Output Pins Truth Table		
Fault Pin, (pin #)	**Action**	**Comments**
IRQ_CLR# (6)	When taken low, resets (pulls high) the IRQ# and TRKR_IRQ# outputs.	IRQ# re-latches if an IRQ exists after IRQ_CLR# is taken high.
MR# (5)	When taken low, resets the RST#1-RST#4 outputs.	RST#1-RST#4 (exclusive) will be reasserted if a reset fault exists after MR# is taken high. Must be pulled low when writing to the SMT4004.
UV_OVERRIDE (12)	When taken high, disables all user-configured undervoltage settings.	Not recommended for the novice, as Trakking and other features are also disabled. This pin should be connected to ground. Undervoltage overrides should be set using the GUI or the I^2C interface.

TABLE 5: SMT4004 PIN ABBREVIATED DESCRIPTION & CONNECTION TABLE

Note: This table was prepared to permit the fastest possible 'first-time' design-in of the highly sophisticated SMT4004.

Pin name, number	Description & Connection Info	
Power, Ground & Sensing		
	IF USED	**IF UNUSED**
VI1, 41	Supply manager #1 input voltage (bus-side); connect to the input side of the current sense resistor (if used).	If Channel 1 is not used, connect VI1 directly to the highest input voltage
VI2, 40	Supply manager #2 input (bus-side) voltage; connect to the input side of the current sense resistor (if used).	If Channel 2 is not used, connect VI2 directly to the highest input voltage
VI3, 39	Supply manager #3 input (bus-side) voltage; connect to the input side of the current sense resistor (if used).	If Channel 3 is not used, connect VI3 directly to the highest input voltage
VI4, 38	Supply manager #4 input (bus-side) voltage; connect to the input side of the current sense resistor (if used).	If Channel 4 is not used, connect VI4 directly to the highest input voltage
PGND, 8 **PGND, 17** **DGND, 18** **AGND, 19**	**Connect all grounds together at the SMT4004. Make a single direct connection from the SMT4004 ground pins to the system's input ground.**	N/A
VDD_CAP, 42	Connect a 10uF capacitor from this pin directly to the SMT4004 ground pins. This node generates the internal VDD from the highest voltage on the VI1-VI4 input pins.	N/A
VGG_CAP, 28	Connect a 1uF capacitor from this pin directly to the SMT4004 ground pins. This node is used to filter the charge pump voltage used to enhance the external N-Channel MOSFETs. The voltage on this node is 12V-17V.	N/A
1.25V_{REF}, 4	A 0.1uF, high-quality (low-ESR) capacitor **must** be connected from this pin directly to the SMT4004 ground pins.	N/A
CB1, 37	Connect to the input side of the current-sense resistor (Kelvin sense method) corresponding to VI1.	If current sensing is not used, connect directly to VI1 at the SMT4004.
CB2, 36	Connect to the input side of the current-sense resistor (Kelvin sense method) corresponding to VI2.	If current sensing is not used, connect directly to VI2 at the SMT4004.
CB3, 35	Connect to the input side of the current-sense resistor (Kelvin sense method) corresponding to VI3.	If current sensing is not used, connect directly to VI3 at the SMT4004.
CB4, 34	Connect to the input side of the current-sense resistor (Kelvin sense method) corresponding to VI4.	If current sensing is not used, connect directly to VI4 at the SMT4004.

Table 5: SMT4004 PIN ABBREVIATED DESCRIPTION & CONNECTION TABLE Continued.

Pin name, number	Description & Connection Info	
Inputs		
	IF USED	**IF UNUSED**
PWR_ON, 33	Refer to Table 2 for proper connection and assertion/de-assertion polarities.	N/A
ENABLE, 24	Refer to Table 2 for proper connection and assertion/de-assertion polarities.	N/A
FORCE_SD, 27	Refer to Table 2 for proper connection and assertion/de-assertion polarities.	N/A
SEATED1#, #2, 10, 11	For normal operation ground these pins. Refer to Table 1 for proper operation.	N/A
IRQ_CLR#, 6	Refer to Table 4 for proper operation.	For normal operation leave this pin open or tie it to the VDD_CAP node with 100k≤ or less.
MR#, 5	Must be pulled low when writing to the SMT4004. Refer to Table 4 for proper operation.	For normal operation leave this pin open or tie it to the VDD_CAP node with 100k≤ or less.
UV_OVERRIDE, 12	Refer to Table 4 for proper operation.	Connect directly to ground.
WLDI, 48	Refer to '**INTERNAL TIMERS' section for proper operation.**	Leave open.
A0-A2, 43-45	I^2C interface device address inputs.	Leave open.
SCL, 47	I^2C clock input.	Leave open.
SCA, 48	I^2C data input/output.	Leave open.
Outputs		
RESET1#-4#, 13-16	Connect to VDD_CAP through a resistor, which limits the current to less than, or equal to 0.5mA. Refer to Table 3 for proper operation.	Leave open.
IRQ#, 7	Connect to VDD_CAP through a resistor, which limits the current to less than, or equal to 0.5mA. Refer to Table 3 for proper operation.	Leave open.
TRKR_IRQ#, 9	Connect to VDD_CAP through a resistor, which limits the current to less than, or equal to 0.5mA. Refer to Table 3 for proper operation.	Leave open.
HEALTHY#, 26	Connect to VDD_CAP through a resistor, which limits the current to less than, or equal to 0.5mA. Refer to Table 3 for proper operation	Leave open.
CBFAULT, 25	An overcurrent on any channel set for current sensing	Leave open.
CROWBAR, 3	Refer to Table 3 for proper operation.	Leave open.
VGATE1-VGATE4, 32, 31, 30, 29	Connect to the respective MOSFET gate through a 10Ω resistor. It is recommended a 10nF capacitor be connected from each output to ground	Leave open.
VO1-VO4, 20-23	Connect to each respective output. For optimum performance, connect close to the load.	If Channel is not used, connect VOx directly to the highest input voltage
LDO#, 1	Connect to VDD_CAP through a resistor, which limits the current to less than, or equal 0.5mA. Refer to '**INTERNAL TIMERS**' section for proper operation.	Leave open.
WDO#, 2	Connect to VDD_CAP through a resistor, which limits the current to less than, or equal 0.5mA. Refer to '**INTERNAL TIMERS**' section for proper operation.	Leave open.

For proper operation all inputs must be driven no higher than the voltage on the VDD_CAP node.

For proper operation all inputs must be driven no lower than the ground nodes.

Observe caution when interfacing to logic families powered by voltages dissimilar than the VDD_CAP node voltage.

All inputs' thresholds are: L ≤ 0.3XVDD_CAP, H ≥ 0.7XVDD_CAP.

Unless otherwise stated; all inputs are pulled up to the VDD_CAP node with a 100kΩ resistor and boast a Schmitt-trigger structure.

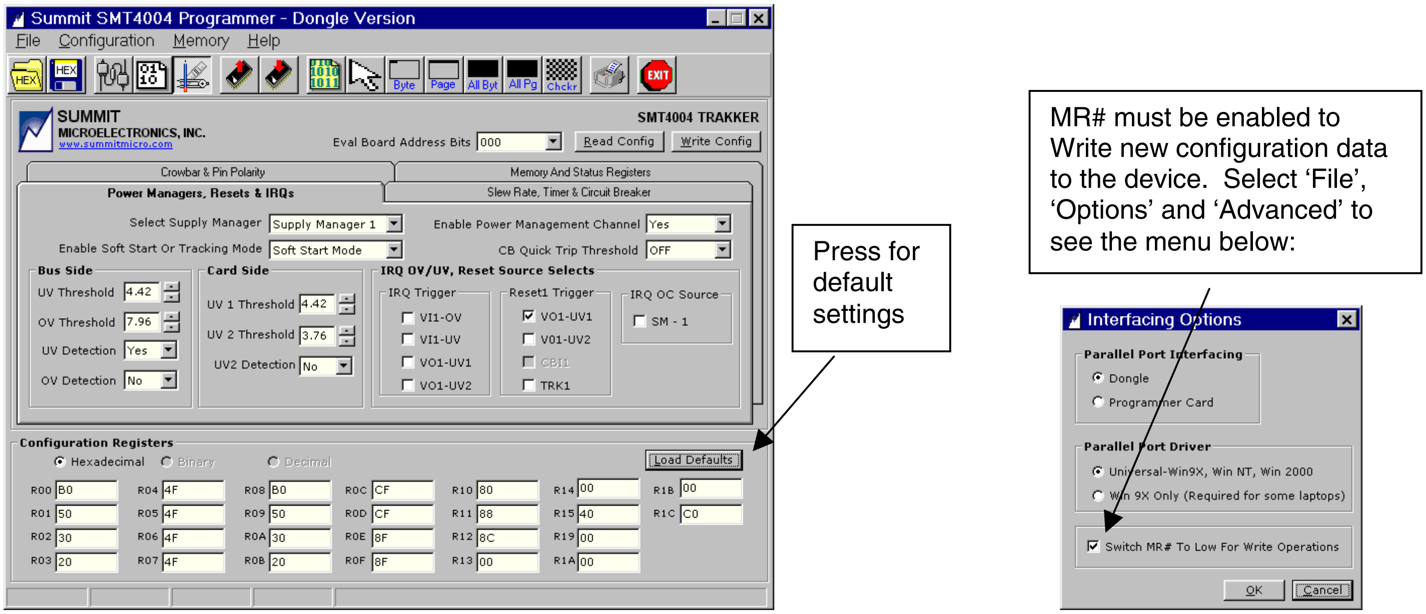


Figure 20 - SMT4004 Default Programmer Window with Default Data loaded into the Configuration Registers

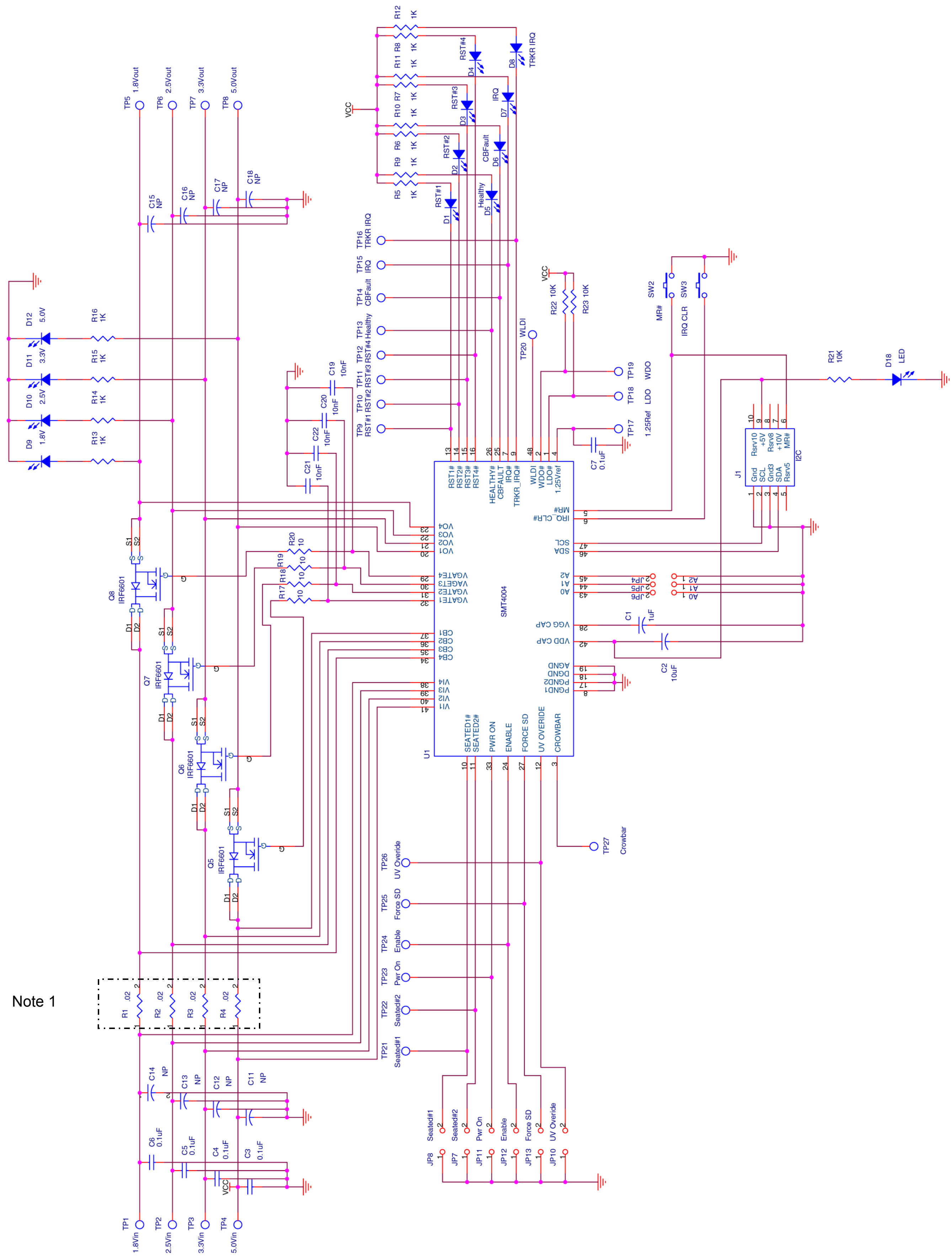


Figure 21 - SMT4004 Evaluation Board Schematic (Note 1-see AN-20 to calculate R1-R4 current-sense values)

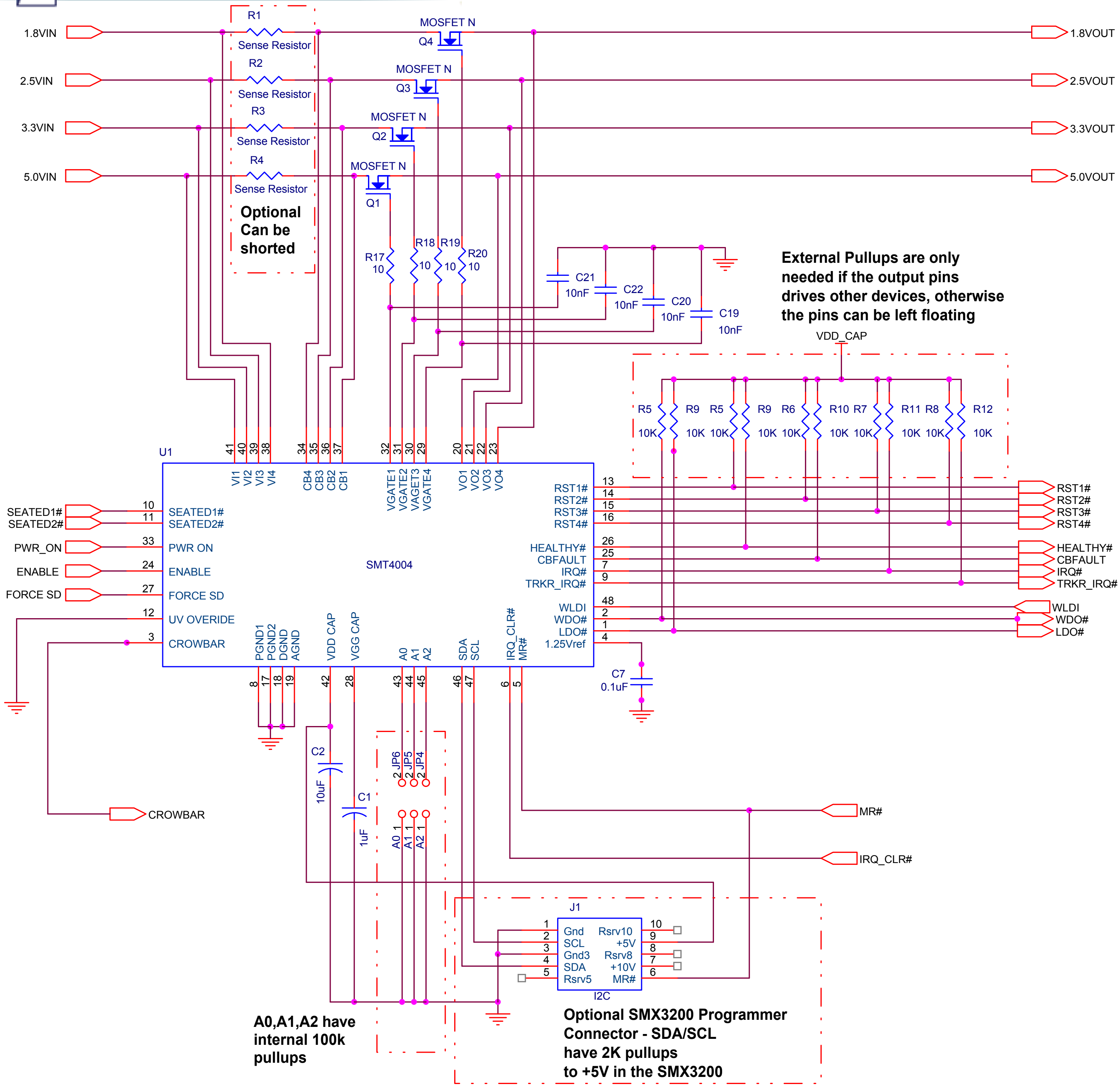


Figure 22 - Minimum external component requirements for an SMT4004 application. Please see application notes 20 and 25 for additional recommendations for operation in telecom systems or noisy environments.

NOTICE

Revision 4.2 - This document supersedes all previous versions and covers silicon revision U10 and Windows GUI revision 2.39.3 and later. Please check the Summit Microelectronics, Inc. web site at www.summitmicro.com for data sheet updates and errata Sheets.