



Compact PCI™ High Availability Hot-Swap Controller With IPMB Support

FEATURES

- IPMB and I²C bus Interface Compatible
- Detects, Monitors and Controls up to 4 independent supplies
- Software Controlled Power-Up/-Down
- Status Reporting: 5V, 3.3V, V1, V2, Healthy, Signal Valid, Reset
- 2k-Bit Non-Volatile E²PROM Memory
- 14V High Side Driver Generation Allows use of Low On Resistance N-Channel FETs
- Under-Voltage Lockout
- Electronic Circuit Breakers
- Programmable Over-current Levels
- Card Insertion Detection and Supply Sequencing
- Flexible Reset Control

APPLICATIONS

- High Availability Compact PCI™ Hot Swap Cards
- IPMI Servers requiring Environmental Reporting
- Compact PCI™ Telecom Line Cards

INTRODUCTION

The SMH4044 is a fully integrated hot swap controller that provides complete power control for add-in cards ranging in use from basic hot swap to high availability systems. It detects proper insertion of the card and senses valid supply voltage levels at the backplane. Utilizing external low on-resistance N-channel MOSFETs, card power is ramped by two high-side driver outputs that are slew-rate limited at 250V/s.

The SMH4044 continuously monitors the host supplies, the add-in card supplies and the add-in card currents. If the SMH4044 detects the current is higher than the programmed value it will shut down the MOSFETs and issue a fault status to the host.

An internal 256 × 8 E²PROM can be used as configuration memory for the individual card or as general purpose memory. Programming of configuration, control and calibration values by the user can be simplified with the interface adapter and Windows GUI software obtainable from Summit Microelectronics.

SIMPLIFIED APPLICATIONS DRAWING

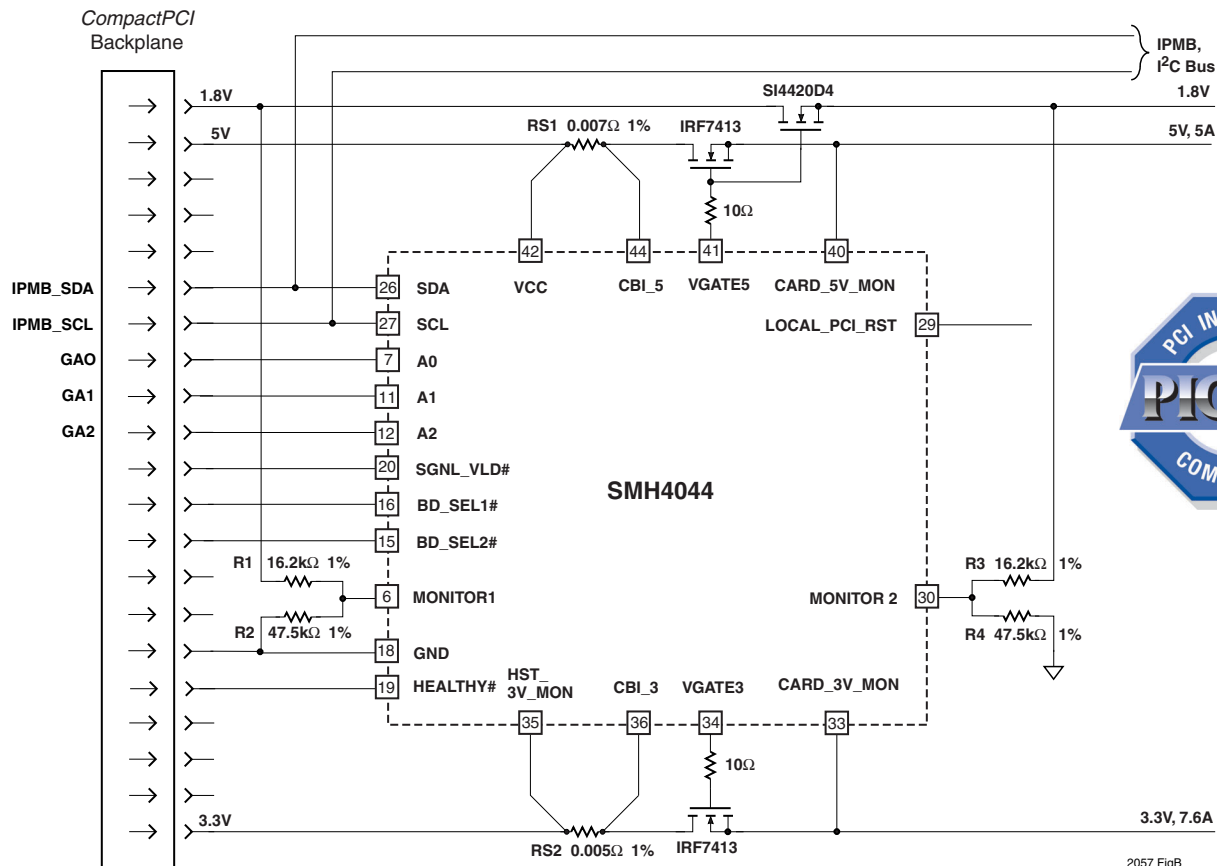


Figure 1. Triple Voltage Hot Swap Control (5V, 3.3V, 1.8V)

Note: This is an applications example only. Some pins, components and values are not shown.



DEVICE OPERATION

The SMH4044 is an integrated power controller for any hot swappable add-in card. It provides all the signals and control functions to be compatible with *CompactPCI™* Hot Swap requirements for basic hot swap systems, full hot swap boards, and high availability systems. The device has options to work in 5V only or mixed 5V and 3.3V cards. Additionally, extra control and monitor pins make it possible to switch *CompactPCI™* +12V and -12V or other voltage levels as required in Figure 1. Alternatively, the same pins can be used to sequence and monitor LDO's and other power devices as shown in Figure 2.

The part monitors over-current conditions, bus side and card side voltage levels which are internally programmable. There are also internal status registers that provide information on monitor conditions, reset and signal valid states. The device can be controlled by the I²C bus to power on/off the VGATE pins for software control of the card power.

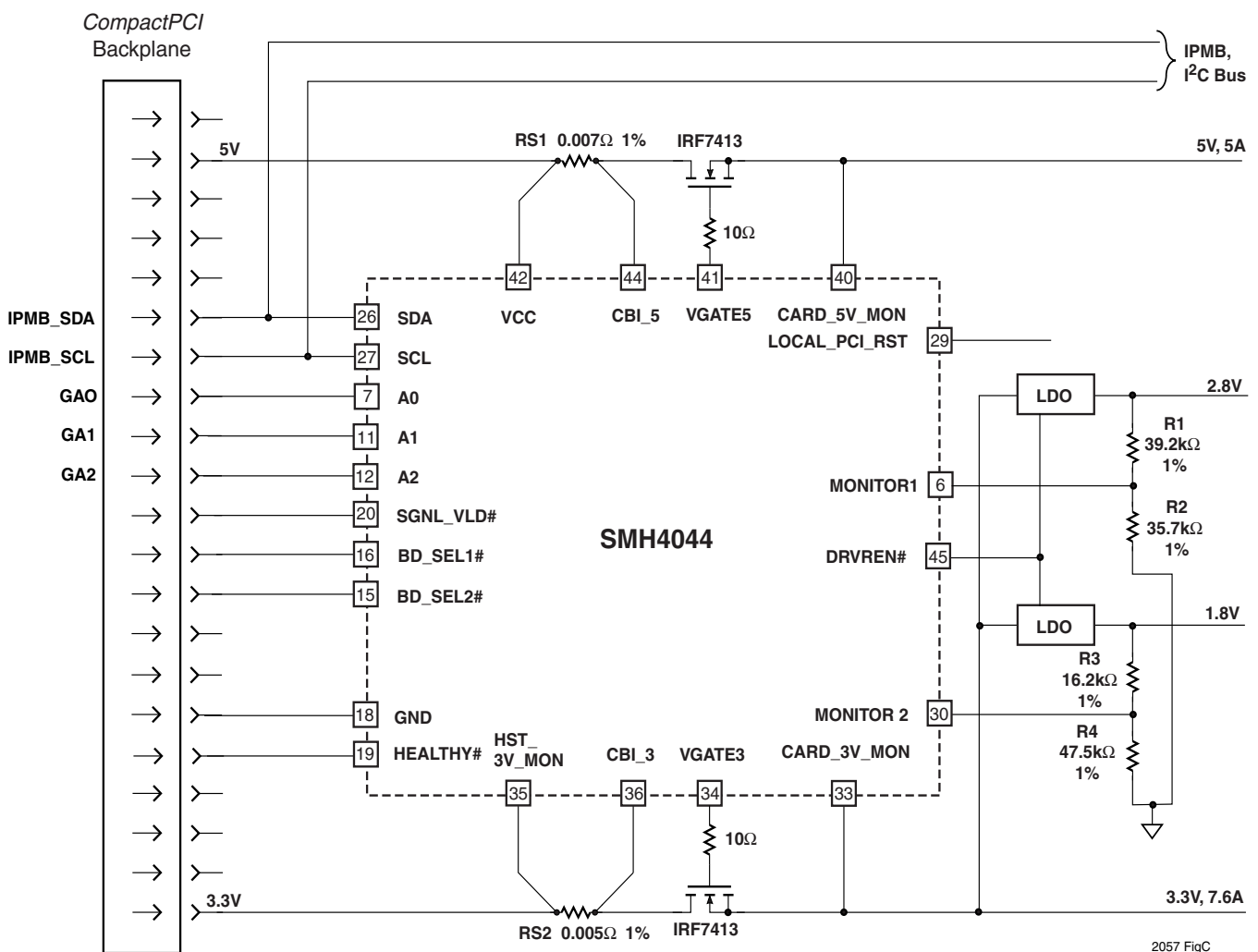
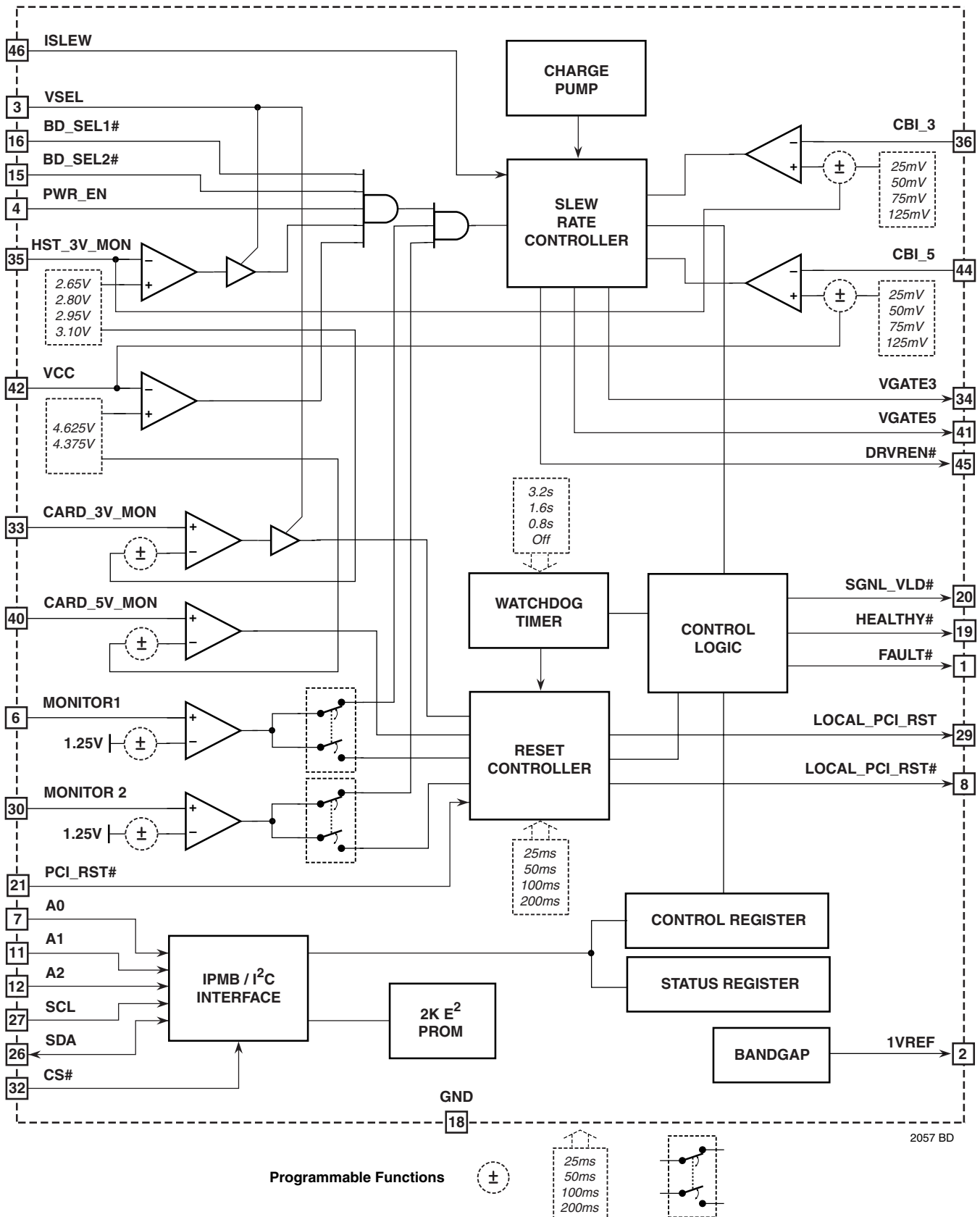


Figure 2. Hot Swap with LDO Sequencing and Output Sensing



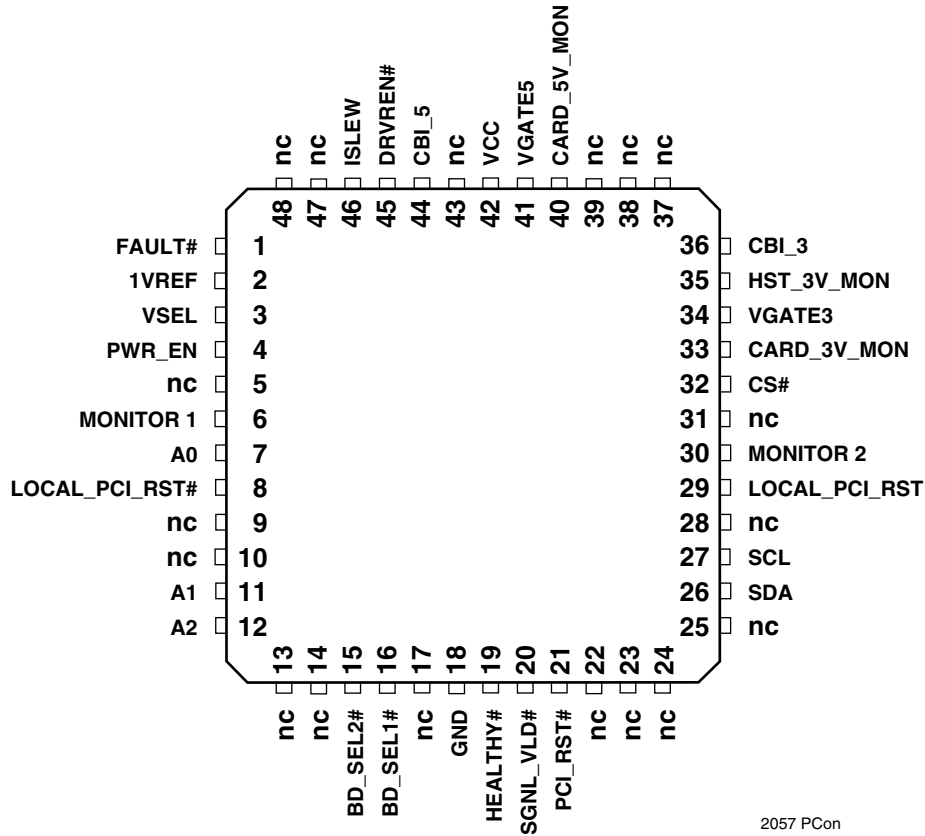
FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATION

48 PIN TQFP PACKAGE



2057 PCon

PIN DESCRIPTIONS

Pin #	Type	Pin Name	Pin Description
7, 11, 12	I	A0, A1, A2	Address inputs 0, 1 and 2 are used to set the three-bit device address of the SMH4044 configuration registers, status register and memory array. The state of these inputs will determine the device address for the SMH4044 if it is on a two-wire bus with multiple devices with the same device type identifier.
26	I/O	SDA	The SDA pin is a bidirectional pin used to transfer data into and out of the SMH4044. Data changing from one state to the other may occur only when SCL is LOW, except when generating START or STOP conditions. SDA is an open-drain output and may be wire-ORed with any number of open-drain outputs.
27	I	SCL	The SCL input is used to clock data into and out of the memory array. In the write mode, data must remain stable while SCL is HIGH. In the read mode, data is clocked out on the falling edge of SCL.
33	I	CARD_3V_MON	This input monitors the card-side 3.3V supply. If the input falls below VTRIP then the HEALTHY# and SGNL_VLD# outputs are de-asserted and the reset outputs are driven active.
40	I	CARD_5V_MON	This input monitors the card-side 5V supply. If the input falls below VTRIP then the HEALTHY# and SGNL_VLD# outputs are de-asserted and the reset outputs are driven active.



PIN DESCRIPTIONS (CONTINUED)

Pin #	Type	Pin Name	Pin Description
36	I	CBI_3	CBI_3 is the circuit breaker input for the low supply. With a series resistor placed in the supply path between HST_3V_MON and CBI_3, the circuit breaker will trip whenever the voltage across the resistor exceeds the Programmed CBI Threshold of 25, 50, 75 or 125mV.
44	I	CBI_5	CBI_5 is the circuit breaker input for the supply voltage. With a series resistor placed in the supply path between the 5V early power and CBI_5, the circuit breaker will trip whenever the voltage across the resistor exceeds the Programmed CBI Threshold of 25, 50, 75 or 125mV.
35	I	HST_3V_MON	This input monitors the host 3.3V supply and it is used as a reference for the circuit breaker comparator. If VCC3 falls below VTRIP then SGNL_VLD# is de-asserted, the high side drivers are disabled, and LOCAL_PCI_RST# is asserted.
46	I	ISLEW	A Diode-connected NFET input. It may be used to adjust the 250V/s default slew rate of the high-side driver outputs.
21	I	PCI_RST#	A TTL level reset input signal from the host interface. A high to low transition (held low longer than 40ns) will initiate a reset sequence. The LOCAL_PCI_RST# and LOCAL_PCI_RST outputs will be driven active for a minimum period of tPURST. If the PCI_RST# input is still held low after tPURST times out the reset outputs will continue to be driven until PCI_RST# is released.
4	I	PWR_EN	A TTL level input that allows the host to enable or disable the power to the individual card. During initial power up this signal would start in a low state, and then be driven high during software initialization. If this signal is driven low then the power supply control outputs will be driven into the inactive state and the reset signals asserted. In a non-High Availability system this input can be tied high. The PWR_EN input is also used to reset the SMH4044 circuit breakers. After an over-current condition is detected the VGATE outputs can be turned back on by first taking PWR_EN low then returning it high.
3	I	VSEL	A TTL level input used to determine which of the host power supply inputs will be monitored for valid voltage and reset generation. This is a static input and the pin should be tied to VCC or ground through a resistor. VSEL is high for 3.3V power, and low for 5V or mixed mode power.
6, 30	I	MONITOR1, MONITOR2	Voltage sensor inputs which will detect voltages and compare them to the internal 1.25V reference. The sensors can be independently configured to sense over voltage or under voltage and can be used as either Host side voltage sensors or Card side voltage sensors.
32	I	CS#	An active low Chip Select input. This signal must be asserted during I2C communications. The CS# signal allows external decoding to be used to extend the number of SMH4044 devices on the same serial bus from 8 — using the Address inputs — to an unlimited number. Bus Capacitive and Resistance loading must be considered when using multiple I2C devices on the same bus. Please refer to generic I2C documentation ("Bus Interface") in this Data Sheet for further information.
16, 15	I	BD_SEL1#, BD_SEL2#	These are active low TTL level inputs with internal pull-ups to VCC. When pulled low they indicate full board insertion. On the host side the signals should be directly tied to ground. In a High Availability application these inputs can be the last pins to mate with the backplane. Alternatively, they can be actively driven by the host, or be connected to switches interfaced to the board ejectors, or any combination. Both inputs must be low before the SMH4044 will begin to turn on the card side voltage.



PIN DESCRIPTIONS (CONTINUED)

Pin #	Type	Pin Name	Pin Description
45	O	DRVREN#	An open-drain, active-low output that indicates the status of the 3V and 5V high side driver outputs (VGATE5 and VGATE3). This signal may also be used as a switching signal for the 12V supply.
8	O or I/O	LOCAL_PCI_RST#	An open-drain active-low output. It is used to reset the card side circuitry on the add-in card. It is active whenever the card-side monitor inputs are below their respective VTRIP levels. It may also be driven low by a low input on the PCI_RST# pin. It can be programmed as an I/O pin and driven low to force a device Reset.
29	O or I/O	LOCAL_PCI_RST	An open-drain (PFET) active-high output. It operates together with LOCAL_PCI_RST#, providing an active high reset signal which is required by many 8051 style MCUs. It is active whenever the card-side monitor inputs are below their respective VTRIP levels. It may also be driven active by a low input on the PCI_RST# pin. It can be programmed as an I/O pin and driven high to force a device Reset.
1	O	FAULT#	An open-drain, active-low output. It is driven low whenever an over-current condition is detected. It is reset when the PWR_EN signal is brought low.
19	O	HEALTHY#	An open-drain, active-low output indicating card side power inputs are above their reset trip levels.
20	O	SGNL_VLD#	An open-drain, active-low output that indicates card side power is valid and the internal card side PCI_RST# timer has timed out.
34	O	VGATE3	A slew rate limited high side driver output for the 3.3V external power FET gate. The output-voltage is generated by an on-board charge pump.
41	O	VGATE5	A slew rate limited high side driver output for the 5V external power FET gate. The output voltage is generated by an on-board charge pump.
2	O	1VREF	This output provides a 1V reference for pre-charging the bus signal pins. Using a simple unity gain amplifier circuit will allow pre-charging a large number of pins.
42	PWR	VCC	The power supply input. It is monitored for power integrity. If it falls below the 5V sense threshold (VTRIP) and the VSEL input is low then the SGNL_VLD# and HEALTHY# signals are de-asserted, the high side drivers disabled, and reset outputs asserted. On a CompactPCI board this must be connected to early power.
18	PWR	GND	Power supply return line. Ground should be applied at the same time as early power.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias -55°C to 125°C
 Storage Temperature -65°C to 150°C
 Lead Solder Temperature (10 secs) 300°C
 Terminal Voltage with Respect to GND:
 CARD_3V_MON, CARD_5V_MON, MONITOR1,
 Monitor2, HST_3V_MON, SGNL_VLD#,
 HEALTHY#, LOCAL_PCI_RET#, VCC 7V
 VGATE3, VGATE5, DRVREN# 16V
 RESET VCC + 0.7V
 All Others VCC + 0.7V
 Junction Temperature 150°C
 ESD Rating per JEDEC 2000V
 Latch-Up testing per JEDEC +/- 100mA

RECOMMENDED OPERATING CONDITIONS*

Temperature Range (Industrial) -40°C to +85°C
 (Commercial) -5°C to +70°C
 Supply Voltage 2.7V to 6.0V
 Package Thermal Resistance (θ JA)
 48 Lead TQFP 80°C/W
 Moisture Classification Level 1 (MSL 1) per J-STD- 020

RELIABILITY CHARACTERISTICS

Data Retention 100 Years
 Endurance 100,000 Cycles

Note * - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.



DC OPERATING CHARACTERISTICS

(Over Recommended Operating Conditions; Voltages are relative to GND)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	Operating voltage	For valid reset only	1			V
I_{CC1}	Supply current (operating)				1	mA
I_{CC2}	Supply current (writing)				3	mA
V_{TRIP}	V_{TRIP} threshold levels (V_{CC5})	4.625V configuration	4.50	4.625	4.75	V
		4.375V configuration	4.25	4.375	4.50	V
	V_{TRIP} threshold levels (V_{CC3})	3.10V configuration	3.02	3.10	3.17	V
		2.95V configuration	2.87	2.95	3.02	V
		2.80V configuration	2.72	2.80	2.87	V
		2.65V configuration	2.57	2.65	2.72	V
	CARD_5V_MON	50mV configuration			V_{CC5} trip + 50mV	V
		-50mV configuration			V_{CC5} trip - 50mV	V
	CARD_3V_MON	50mV configuration			V_{CC3} trip + 50mV	V
		-50mV configuration			V_{CC3} trip - 50mV	V
	MONITOR1, MONITOR2		1.2	1.25	1.3	V
V_{TRHST}	Trip point hysteresis			20		mV
I_{LI}	Input leakage current				2	μ A
I_{LO}	Output leakage current				10	μ A
V_{IL}	Input low voltage		-0.1		0.8	V
V_{IH}	Input high voltage		2		$V_{CC} + 1V$	V
V_{OL}	Output low voltage	$V_{CC} = 5V, I_{OL} = 2.1mA$			0.4	V
V_{OH}	Output high voltage	$V_{CC} = 5V, I_{OH} = -400\mu A$	2.4			V
V_{OLRS}	LOCAL_PCI_RESET# output low voltage	$I_{OL} = 3.2mA$			0.7	V
V_{OHRS}	RESET output high voltage	$I_{OH} = 800\mu A$	$V_{CC5} - 1.3V$			V
V_{GATE}	VGATE3, VGATE5 output voltage	$I_{OH} = 20\mu A$	12	14	15	V
1VREF	Reference output voltage	No load	0.95	1.00	1.05	V
V_{CB}	Circuit breaker trip voltage ($V_{CC} - CBI_5$) or (HST_3v_MON - CBI_3)	125mV configuration	100	125	150	mV
		75mV configuration	60	75	90	mV
		50mV configuration	40	50	60	mV
		25mV configuration	20	25	30	mV

2057 Elect Table



AC OPERATING CHARACTERISTICS

(Over Recommended Operating Conditions; Voltages are relative to GND)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{VTPD}	V_{TRIP} to power down delay	$V_{Overdrive} = 20mV$		1	5	μs
t_{VTR}	V_{TRIP} to reset output delay	$V_{Overdrive} = 20mV$		1	5	μs
t_{PRLPR}	PCI_RST# to LOCAL_PCI_RST#			0.1	1	μs
t_{SLEW}	Slew rate		190	220	250	V/s
t_{HSE}	BD_SEL# to power on delay	25ms configuration	20	25	30	ms
		50ms configuration	40	50	60	ms
		100ms configuration	80	100	120	ms
		200ms configuration	160	200	240	ms
t_{PURST}	RESET pulse width	25ms configuration	20	25	30	ms
		50ms configuration	40	50	60	ms
		100ms configuration	80	100	120	ms
		200ms configuration	160	200	240	ms
t_{WD}	Watchdog timer duration	0.8s configuration	0.64	0.8	0.96	s
		1.6s configuration	1.28	1.6	1.92	s
		3.2s configuration	2.56	3.2	3.84	s
t_{GLITCH}	Glitch rejection pulse width			40	ns	
t_{OCF}	Overcurrent to FAULT# output		0.5	1	2	μs
t_{OCVG}	Overcurrent to gate off		0.5	1	2	μs
t_{CBTC}	Circuit breaker time constant	Operating	8	16	24	μs

Table 1. Card Insertion Timing

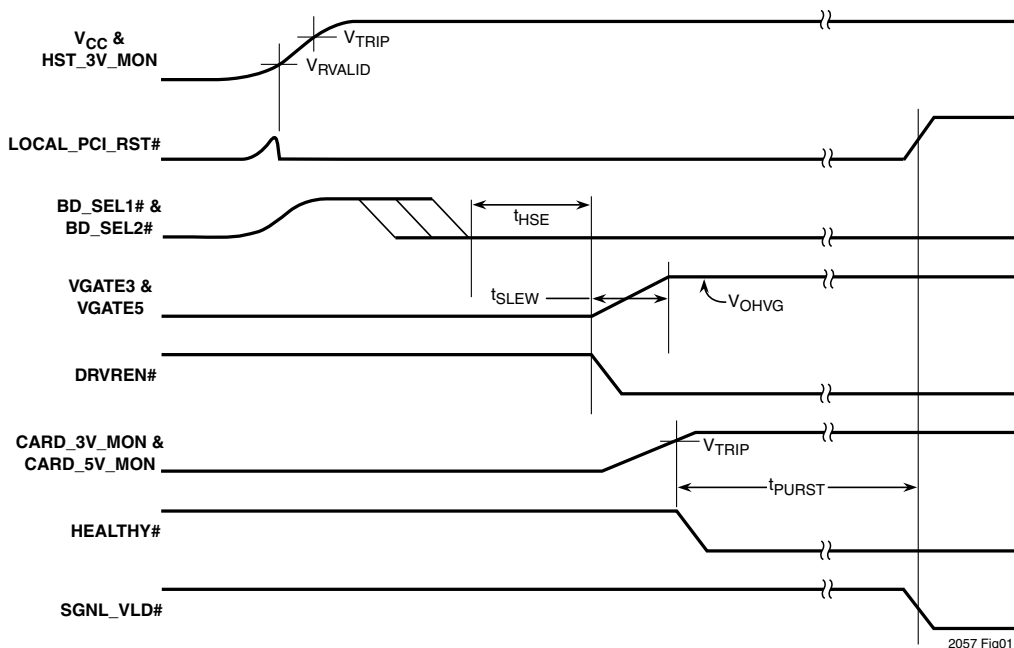


Figure 3. Card Insertion Timing Diagram



I²C 2-WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS - 100kHz

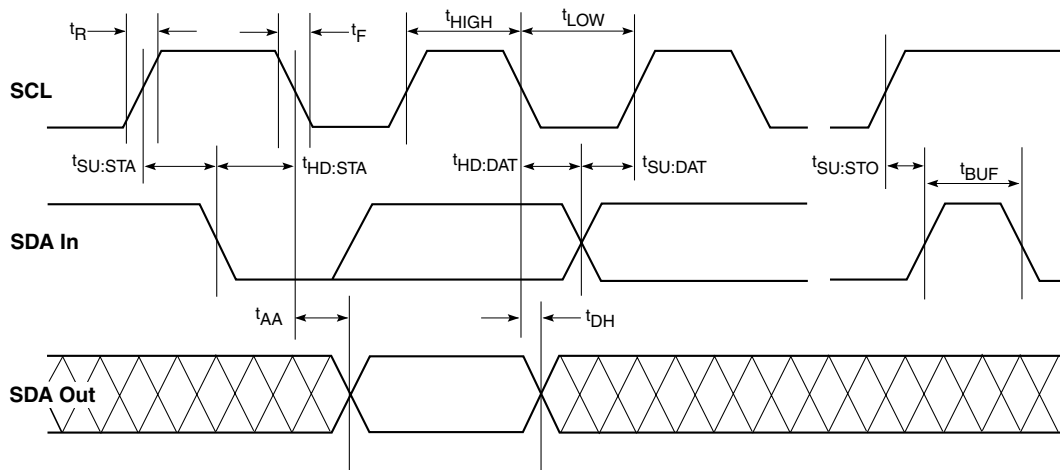
(Over Recommended Operating Conditions; Voltages are relative to GND)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f _{SCL}	SCL clock frequency		0		100	kHz
t _{LOW}	Clock low period		4.7			μs
t _{HIGH}	Clock high period		4.0			μs
t _{BUF}	Bus free time (1)	Before new transmission	4.7			μs
t _{SU:STA}	Start condition setup time		4.7			μs
t _{HD:STA}	Start condition hold time		4.0			μs
t _{SU:STO}	Stop condition setup time		4.7			μs
t _{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.2		3.5	μs
t _{DH}	Data Out hold time	SCL low (cycle n+1) to SDA change	0.2			μs
t _R	SCL and SDA rise time (1)				1000	ns
t _F	SCL and SDA fall time (1)				300	ns
t _{SU:DAT}	Data In setup time		250			ns
t _{HD:DAT}	Data In hold time		0			ns
TI	Noise filter SCL and SDA	Noise suppression		100		ns
t _{WR}	Write cycle time				5	ms

Note: (1) These values are guaranteed by design.

2057 Table02

Table 2. I²C Timing Specifications



2057 Fig07

Figure 4. I²C Timing Diagram



APPLICATIONS INFORMATION

POWER UP SEQUENCE

Insertion Process

As the add-in board (Figure A) is inserted into the backplane, physical connections are made with the chassis in order to properly discharge any voltage potentials to ground. The board will first contact the long pins on the backplane that provide early power (5V, 3.3V and ground). Depending upon the board configuration, early power and ground should be routed to the SMH4044. As soon as power is applied the SMH4044 will assert the reset outputs to the card side circuits, turn off the VGATE3 and VGATE5 outputs (disabling the external power FETs) and assert 1VREF. This signal can be used to pre-charge the I/O pins before they begin to mate with the bus signals. The open collector HEALTHY# output will be de-asserted. It should be actively pulled high by an external pull-up resistor (minimum 10k Ω).

The next pins to mate are the I/Os, and the balance of the power pins if they are not already mated. The I/Os will have been pre-charged by the 1VREF output.

The BD_SEL# pins are the last inputs to be driven to their true state. In most systems these will most likely be driven to ground when the short pins are mated. This would indicate the card is fully inserted and the power-up sequence can begin. If, however, the design is based on high availability requirements, the two pins can be actively driven by the host or combined with a switch input indicating the ejector handles are fully engaged.

Sequencing

Once the proper card insertion has been assured the SMH4044 will check the status of the Power Enable signal from the host. This input can be used to power down individual cards on the bus via software control. It must be held high in order for the SMH4044 to enable power sequencing to the card.

When these conditions have been met, the SMH4044 will drive the VGATE3 and VGATE5 outputs to turn on the external 3 volt and 5 volt power FETs. The slew rate of these outputs is controlled to 250V/s. Different slew rates can be accommodated by either adding an additional capacitor between the MOSFET gate and ground or by injecting current into the ISLEW input. All circuitry on the card is held in a reset condition until the 5V (or 3.3V) supply is stable and the reset interval timer has timed out. At this point, the reset signals are de-asserted, and proper operation of the card commences. See Figure 1, Table 1, and Flow Chart 1.

The SMH4044 will monitor the card's backend voltages. Once they are at or above the card V_{TRIP} levels the SMH4044 will drive the HEALTHY# output low.

Card Removal Process

The card removal process operates in the opposite sequence. For non-high-availability cards the action of card removal disconnects the BD_SEL# (short pins) from ground and the SMH4044 will instantly shutdown the VGATE outputs, change the HEALTHY# status, and assert the LOCAL_PCI_RST and LOCAL_PCI_RST# outputs.

Because connectors to the host backplane employ staggered pins, power will still be applied to the SMH4044 and the I/O interface circuits. The LOCAL_PCI_RST and LOCAL_PCI_RST# signals will place the interface circuits into a high impedance condition. The pre-charge voltage will be applied to the I/Os enabling a graceful disengagement from the active bus. Once the I/O pins are free of the backplane, power can be removed from the SMH4044 and other early power devices by releasing the long pins.

The removal process is slightly different for a high-availability system. As the ejector handle is rotated the ejector switch will open, causing a change of state that will activate the ENUM# signal to the host. In response to this notification the host will de-assert a hardware controlled BD_SEL# signal. This action will turn on an indicator LED on the card, notifying the operator it is now safe to proceed with the removal of the card. The sequence will then follow that outlined for the non-high-availability removal process.

Power Configurations

The SMH4044 can be used in 5V only, 3.3V-only and mixed voltage systems. For systems with a single power supply, connect V_{CC} and HST_3V_MON together to the bus power line. Also connect CARD_3V_MON and CARD_5V_MON together to the card side power. Now the state of VSEL determines the reset level that will be used to signal valid power. For 3.3V systems tie VSEL to V_{CC}, for 5V systems tie VSEL to ground.



APPLICATIONS INFORMATION (CONTINUED)

DESIGN CONSIDERATIONS FOR A COMPACTPCI BOARD

Figure 5 is a generic representation of a CompactPCI board and it illustrates how the SMH4044 is the key component in the board insertion/removal process. Details and schematics of how the various blocks interface to the SMH4044 are shown in the SMH4044EV Evaluation Kit Users guide available on the Summit web site.

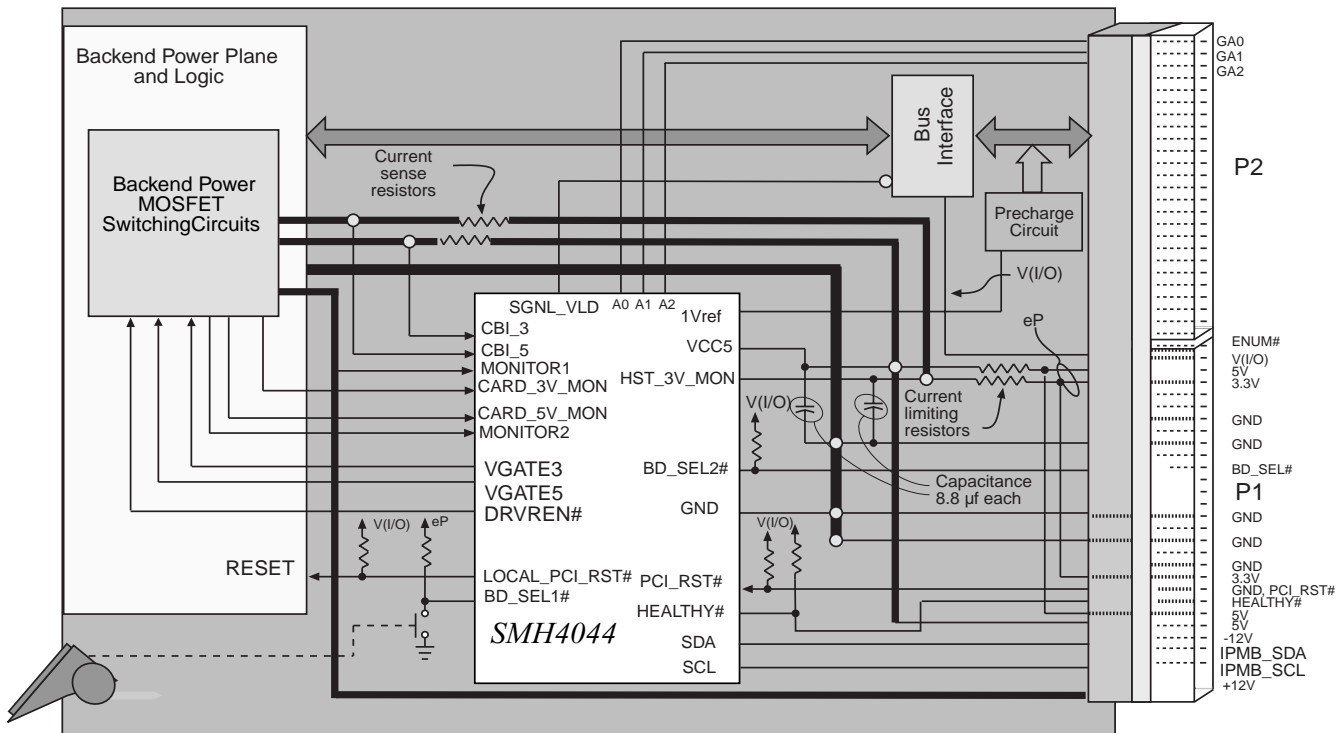


Figure 5. Example Compact PCI™ Hot Swap Card — Hot Swap (5V and 3.3V)

Power Busses

It is important in the design of the board to ensure the backend logic is isolated from the power control circuits and other early power circuits such as FPGAs and the I/O interface circuits. In Figure 5 the early power busses for 5V and 3V have series current limiting resistors. These values should be calculated so as to limit the in-rush current that will initially charge the capacitive load of the early power circuits. As the card is inserted further, the medium length pins engage and short out the current

limiting resistors. Note the placement of the sense (shunt) resistors. They are in series with the power FETs and no voltage drop will be detected across the resistor until VGATE is applied to the power FETs. The sense resistor values are determined by dividing 50mV by the current specification for that supply.

It should be noted that there is an inherent delay from VGATE5 turning on to VGATE3 turning on. The typical delay is illustrated in Figure 6.



APPLICATIONS INFORMATION (CONTINUED)

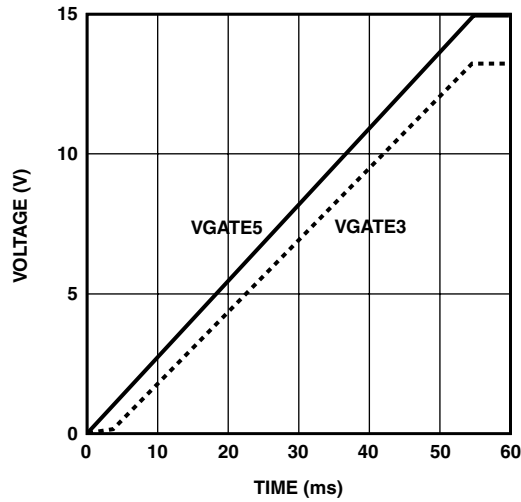
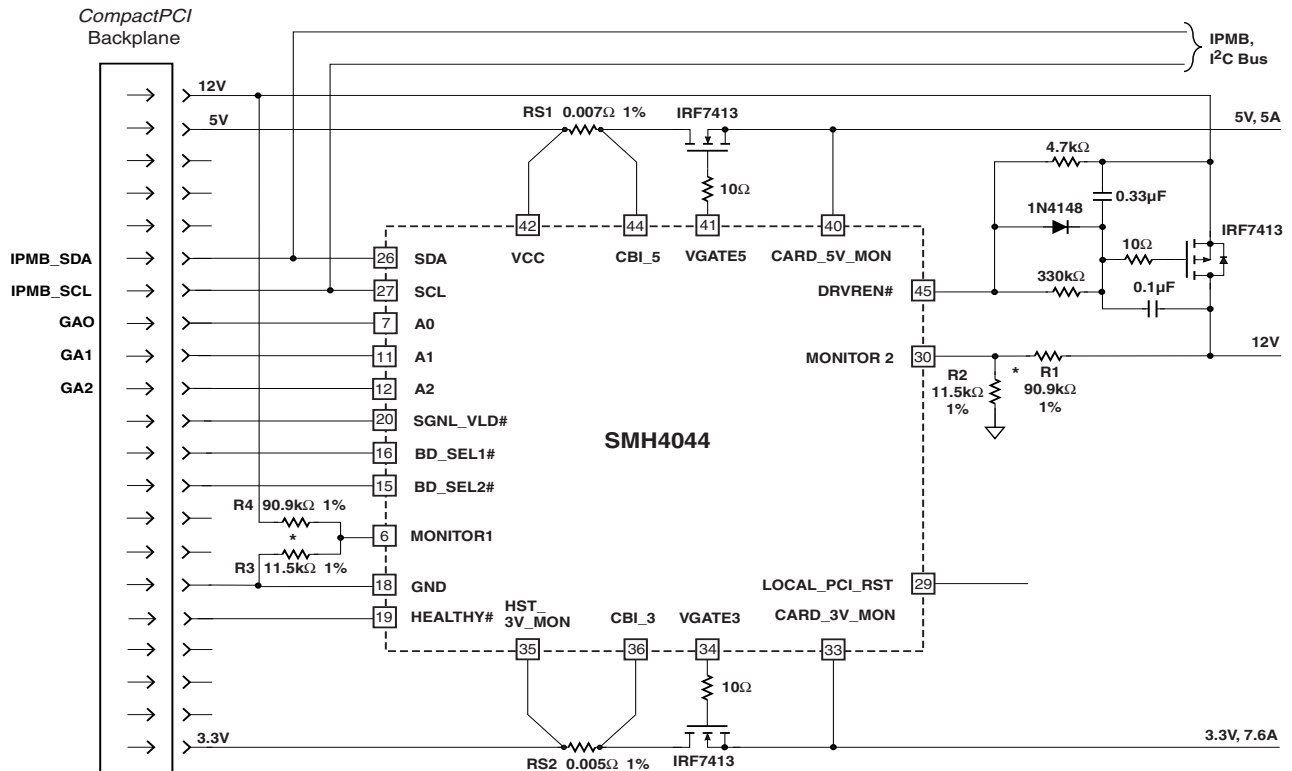


Figure 6. Typical Delay: VGATE5 to VGATE3

+12V and -12V Power Busses

Optionally, the +12V and/or the -12V supplies available from the CompactPCI bus can be hotswapped using the DRVREN# pin.

The +12V interface is shown in Figure 7. Both the +12V and -12V interfaces are shown in Figure 8.



* Note: The values of R1, R2, R3, and R4 are specified so that the inputs to MONITOR1 and MONITOR2 are above 1.3V for undervoltage monitoring.

2057 FigA

Figure 7. Application Drawing — Triple Voltage Hot Swap (12V, 5V, 3.3V)



APPLICATIONS INFORMATION (CONTINUED)

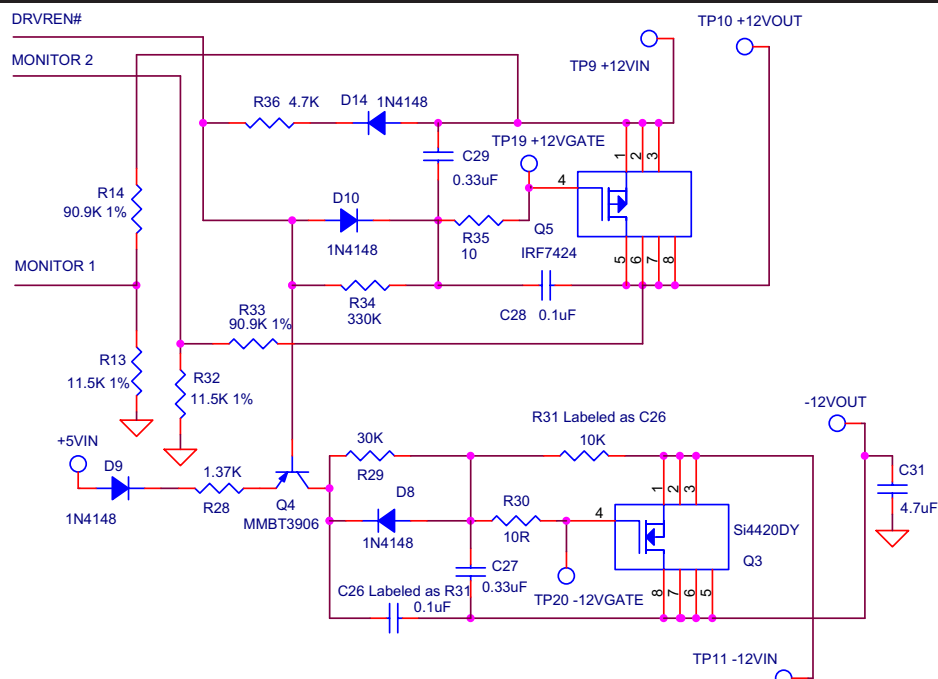


Figure 8 – The +12V and -12V Mosfet circuitry

+12V (Q5 and associated circuitry)**Turn On:**

To ensure Q5 (P-channel MOSFET) does not turn on with the application of the +12V input the ratio of C28 to C29 is chosen to limit the initial gate to source voltage well below Q5's threshold voltage. Upon application of power Q5's gate is quickly discharged to approximately +12V through D14, R36, D10 and R35. The SMH4044 asserts the DRVREN# output (low) after the VGATE outputs are turned on, allowing Q5 to slowly turn on (soft-started) by discharging the gate voltage through R34 into the DRVREN# pin. The rate of turn on of the 12V supply is set by the RC time constant of R34 and C29. R35 acts to prevent oscillations by damping the resonant circuit formed by Q5's to source capacitance and source inductance. D14 prevents the -12V supply from turning on when the +12V supply is not present or is low enough to allow Q4 (see -12V circuit explanation below) to become forward biased. D10 shunts R34 allowing rapid turn off of the +12V supply.

A precision voltage divider consisting of R33 and R32 is used by the SMH4044 to monitor 12V output for under or Overvoltage conditions. Resistors R13 and R14 perform the same function for the 12V input.

Turn Off:

After the +12V supply is turned on, de-assertion of the DRVREN# output (+5V or +3.3V circuits out of specification) initiates shutdown of the +12V supply. Q5 is shut off when DRVREN# goes high by quickly charging the gate to within 2 diode voltage drops (D14 and D10) of the

+12V via R36, D10 and D14. The turn off time of the +12V supply depends on the RC time constant of R36 and C29.

-12V (Q3 and associated circuitry)**Turn On:**

The -12V supply is turned on in a similar manner as the +12V. C26 and C27 prevent Q3 (N-channel MOSFET) from turning on when the -12V supply is applied to the circuit. The gate is discharged to the -12V supply through R31 and charged (turned on) to within 1 diode voltage drop through R29 into the collector of Q4. Like the +12V supply, assertion of the DRVREN# output begins soft-starting Q3 by forward biasing Q4 (PNP) allowing the gate turn on current to pass through Q4, R28 and D9 into the +5V input supply. R28 sets the voltage gain of Q4:

$$A_{V(Q4)} = \frac{R31 + R29}{R28}$$

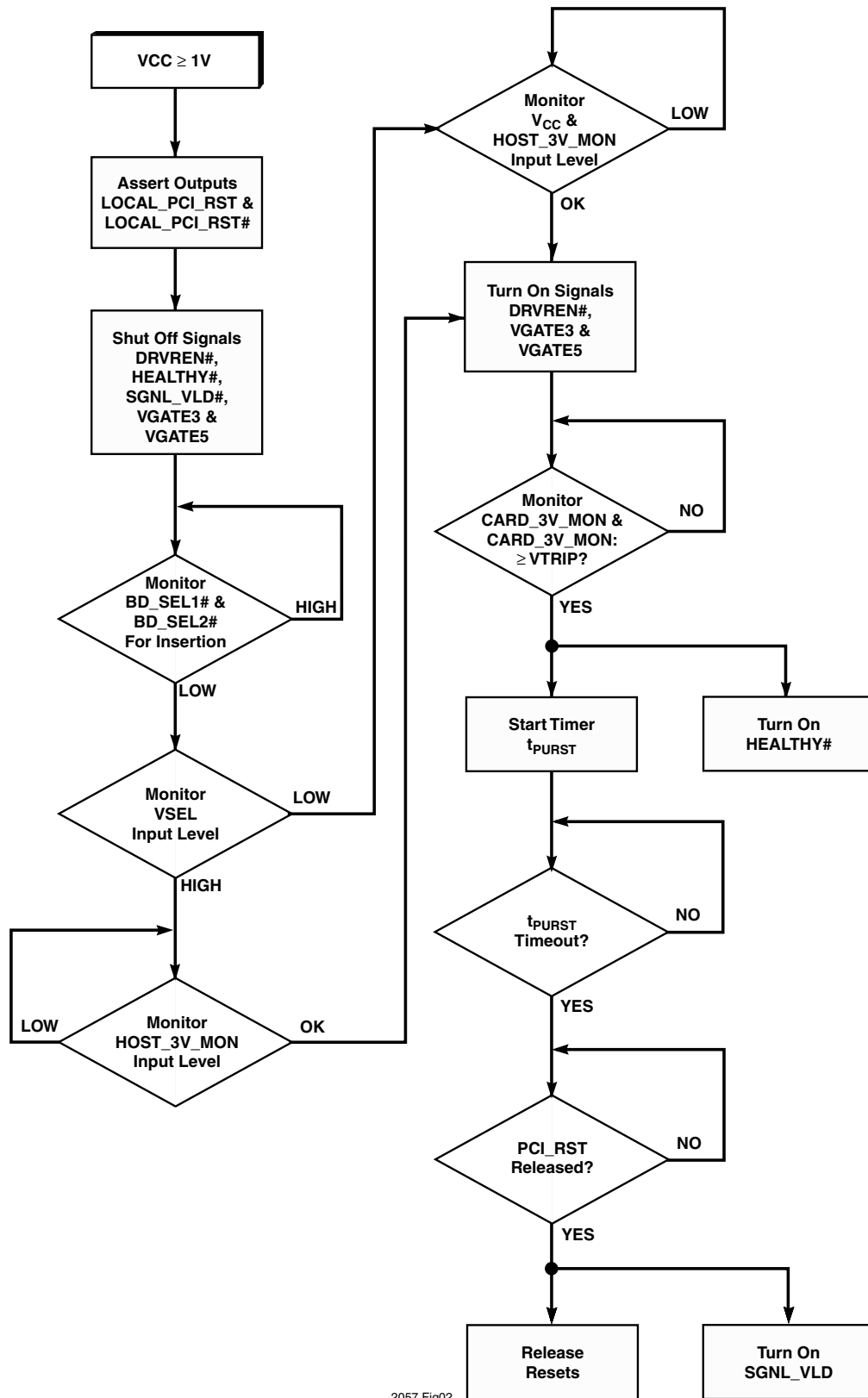
This voltage gain ratio ensures the voltage drop across R30 is sufficient to fully enhance Q3. D9 is used to drop enough voltage in the circuit to prevent reverse bias avalanching of Q4's emitter base junction.

Turn Off:

When DRVREN# goes high, Q4 is reverse biased allowing R31 to discharge the gate through R31. D8 also assists in turn off by allowing the charge across C26 to be discharged back into the gate.



APPLICATIONS INFORMATION (CONTINUED)



2057 Fig02

2057 Table01

Figure 9. Sequence Diagram Flow Chart



APPLICATIONS INFORMATION (CONTINUED)

MONITORING THE POWER SUPPLY HEALTH

The SMH4044 has a total of 8 comparators that are used to monitor the health of the Host platform supplies and the Card-side (backend) voltages. In hot swap applications each supply going to the backend logic needs to be monitored at three points.

The first point is at the source on the Host connector, V_{CC} and HST_3V_MON. If this voltage is not within specification the down stream sequencing of powering-on the backend logic will not proceed.

The next stage (the CBI inputs) is one step closer to the backend logic to monitor the current flowing into the backend logic. This cannot exceed the specification; however, If it does, then the SMH4044 must turn off the source to the backend logic.

The CARD_5V_MON and CARD_3V_MON inputs are used to sense the actual voltage level in the backend logic. If either comparator detects a low voltage condition the backend logic will be placed in a reset condition (LOCAL_PCI_RST and LOCAL_PCI_RST# asserted), but the VGATE outputs will remain active so long as the Host voltage and current sense are valid.

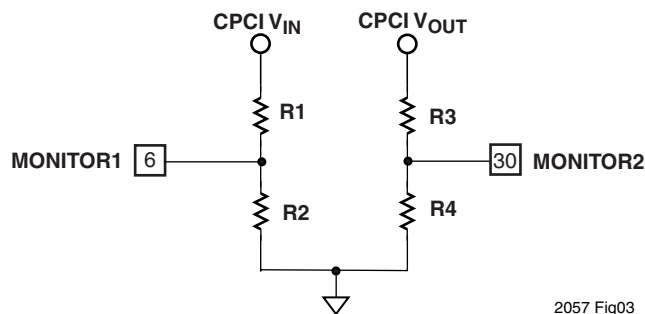
Two other monitor inputs, MONITOR1 and MONITOR2, can be used as additional voltage sensors on either the Host side or the Card side. When either or both of these monitor inputs are used on the Host side, their status will be logically ANDed with the V_{CC} and HST_3V_MON logic. When either or both are configured to be used as Card side monitors, their status will be logically ANDed with the CARD_5V_MON and CARD_3V_MON logic.

This allows the device to be configured in a variety of ways such as:

- A. 4 Host Side, 2 Card Side Monitors
- B. 1 Host Side, 3 Card Side Monitors
- C. 1 Host Side, 4 Card Side Monitors

The Programmable Monitor Inputs are compared to the internal 1.25V reference, simplifying the monitoring of voltages higher than V_{CC} or lower than ground.

In most cases, these monitor inputs will be set to monitor an under-voltage condition, as are the other voltage monitors on the chip. Both MONITOR1 and MONITOR2 can be configured to detect over-voltage conditions as well. See Figure 10. The formulas hold for those cases where $CPCIV_{IN}$ = the input monitored voltage, and where $CPCIV_{OUT}$ = the output monitored voltage.



2057 Fig03

Figure 10. Monitor Detection

To monitor an under-voltage condition:

$$\frac{R1}{R2} = \frac{CPCIV_{IN_{MIN}}}{1.3} - 1$$

$$\frac{R3}{R4} = \frac{CPCIV_{OUT_{MIN}} - I_{LOAD} R_{DS_{ON}}}{1.3} \frac{RS1}{RS1} - 1$$

To monitor an over-voltage condition:

$$\frac{R1}{R2} = \frac{CPCIV_{IN_{MAX}}}{1.2} - 1$$

$$\frac{R3}{R4} = \frac{CPCIV_{OUT_{MAX}} - I_{LOAD} R_{DS_{ON}}}{1.2} \frac{RS1}{RS1} - 1$$

WATCHDOG TIMER

The SMH4044 has an internal Watchdog Timer with a programmable watchdog interval of 0.8, 1.6 or 3.2 seconds. The watchdog is reset each time a valid I²C address command is received by the SMH4044. Each time the SMH4044 generates an acknowledge on the I²C bus, it will reset the Watchdog Timer. The Watchdog Timer will also be reset on any CS# edge.

V_{CC} vs. HST_3V_MON

The V_{CC} input is the supply input and in a **CompactPCI** application this pin must connect to an early power pin on the Host connector. The HST_3V_MON input is strictly a voltage monitoring input, not a supply input. The operating supply voltage range on the V_{CC} pin is 2.7V to 5.5V, but it will only monitor a 5V supply. This is not an issue with a dual supply application, but in a single supply application these two pins must be shorted and VSEL properly set.



APPLICATIONS INFORMATION (CONTINUED)

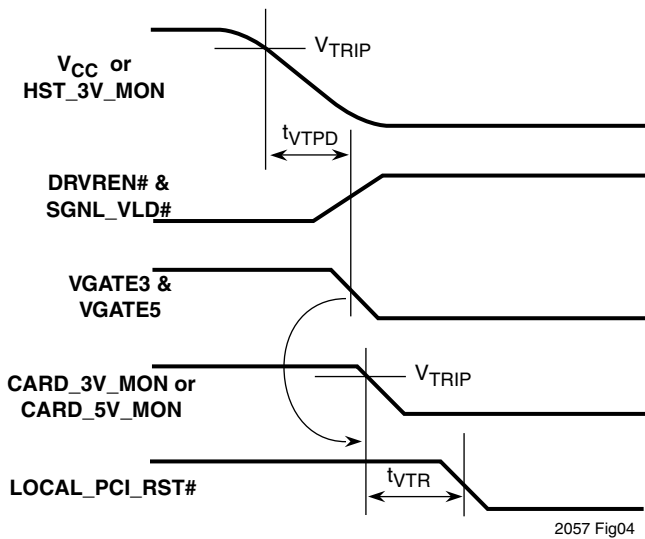


Figure 11. Loss-of-Voltage Timing Sequence

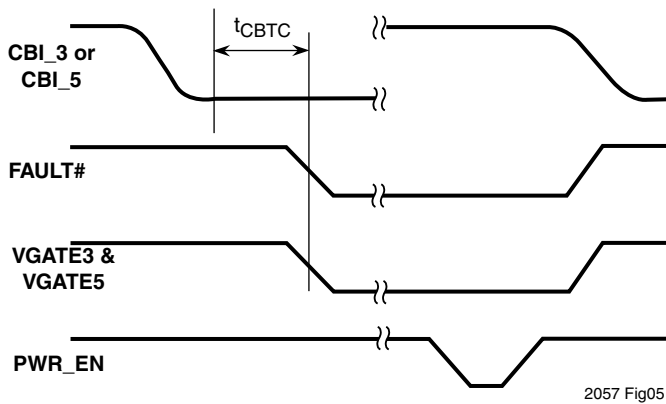


Figure 12. Circuit Breaker Timing Sequence

Programmable V_{TRIP} Thresholds

The Host voltage monitors and the backend voltage monitors are programmable (by the factory) and provide a number of options to the end user. The V_{CC} monitor V_{TRIP} level can be selected for either a 5% or 10% supply with default values of 4.375V or 4.625V. The HST_3V_MON V_{TRIP} level can be programmed to 2.65V, 2.8V, 2.95V or 3.1V.

The CARD_5V_MON and CARD_3V_MON thresholds are set in relation to their corresponding Host voltage monitor thresholds. Their offset can be either 50mV or -50mV. This allows the designer to select 50mV if they want a

collapse in the backend voltage to trigger a local reset condition prior to the Host supply collapsing and powering down the board without warning. Alternatively they can choose -50mV to trigger a board shutdown based on the Host power supply falling out of spec.

Also see Figure 11.

Over-current Circuit Breaker

The SMH4044 provides a circuit breaker function to protect against short circuit conditions or exceeding the supply limits. By placing a series resistor between the Host supply and the CBI pins, the breakers will trip whenever the voltage drop across the series resistor is greater than the programmed value (25, 50, 75 or 125mV) for more than 16µs.

Also see Figure 12.

Reset Control

While in the power sequencing mode, the reset outputs are the last to be released. When they are released all conditions of a successful power-up sequence must have been met:

- 1) V_{CC} and HST_3V_MON are at or above their respective V_{TRIP} levels (MONITOR1 and/or MONITOR2 are above 1.25 V if configured as Host Side monitors);
- 2) BD_SEL# inputs are low;
- 3) CARD_3V_MON and CARD_5V_MON are at or above their respective trip levels (MONITOR1 and/or MONITOR2 are above 1.25 V if configured as CARD Side monitors);
- 4) PWR_EN is high; and
- 5) PCI_RST# is high.

The PCI-RST# input must be high for the reset outputs to be released. Assuming all of the conditions listed above have been met and t_{PURST} has expired, a low input of greater than 40ns duration on the PCI_RST# input will initiate a reset cycle. The duration of the reset cycle will be determined by the PCI_RST# input. If PCI_RST# low is shorter than t_{PURST}, the reset outputs will be driven active for t_{PURST}. If PCI_RST# is longer than t_{PURST} the reset outputs will remain active until PCI_RST# is released.

Also see Figure 13.



APPLICATIONS INFORMATION (CONTINUED)

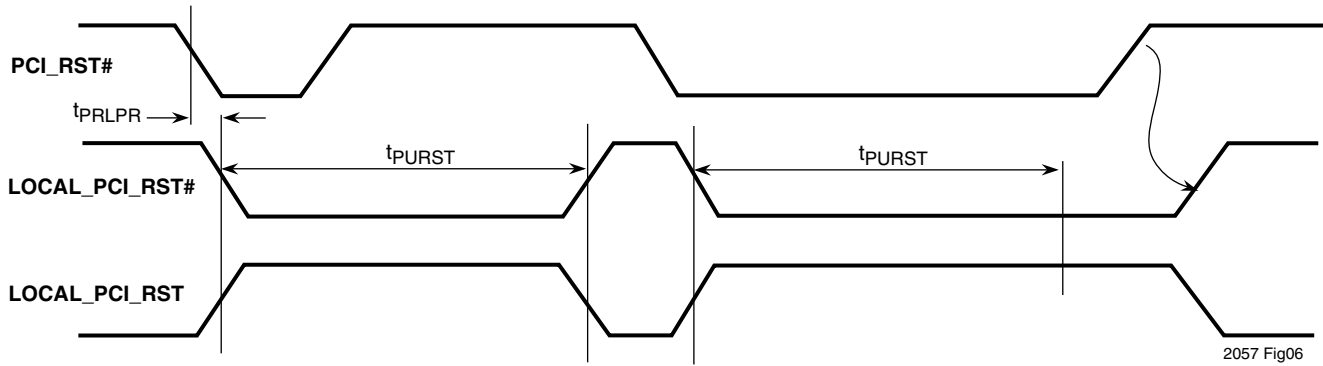


Figure 13 Host-initiated Reset Timing



CONFIGURATION REGISTER SETTINGS

Table 3 - Configuration register R00 description.

Register R00								
D7	D6	D5	D4	D3	D2	D1	D0	Action
1	x	x	x	x	x	x	x	Local_PCI_RST/RST# Set as an I/O pin
0	x	x	x	x	x	x	x	Local_PCI_RST/RST# Set as an Input pin
x	1	x	x	x	x	x	x	VO5/VO3 Threshold set 50mV above VC5/VC3
x	0	x	x	x	x	x	x	VO5/VO3 Threshold set 50mV below VC5/VC3
x	x	1	1	x	x	x	x	VC3/VO3 Trip Threshold set to 3.10V
x	x	1	0	x	x	x	x	VC3/VO3 Trip Threshold set to 2.95V
x	x	0	1	x	x	x	x	VC3/VO3 Trip Threshold set to 2.80V
x	x	0	0	x	x	x	x	VC3/VO3 Trip Threshold set to 2.65V
x	x	x	x	1	1	x	x	Watchdog Timeout Set to 3.2s
x	x	x	x	1	0	x	x	Watchdog Timeout Set to 1.6s
x	x	x	x	0	1	x	x	Watchdog Timeout Set to 0.8s
x	x	x	x	0	0	x	x	Watchdog Timeout Set to Off
x	x	x	x	x	x	1	1	Reset Timeout and BD_SEL# Delay Set to 200ms
x	x	x	x	x	x	1	0	Reset Timeout and BD_SEL# Delay Set to 100ms
x	x	x	x	x	x	0	1	Reset Timeout and BD_SEL# Delay Set to 50ms
x	x	x	x	x	x	0	0	Reset Timeout and BD_SEL# Delay Set to 25ms

Table 4 - Configuration register R01 description.

Register R01								
D7	D6	D5	D4	D3	D2	D1	D0	Action
1	x	x	x	x	x	x	x	Configuration Register Locked
0	x	x	x	x	x	x	x	Configuration Register Unlocked
x	1	x	x	x	x	x	x	V5 Trip Threshold set to 4.625V
x	0	x	x	x	x	x	x	V5 Trip Threshold set to 4.375V
x	x	1	1	x	x	x	x	Over Current CBI Trip Level set to 125mV
x	x	1	0	x	x	x	x	Over Current CBI Trip Level set to 75mV
x	x	0	1	x	x	x	x	Over Current CBI Trip Level set to 50mV
x	x	0	0	x	x	x	x	Over Current CBI Trip Level set to 25mV
x	x	x	x	1	x	x	x	Monitor 2 sensing set to Bus Side
x	x	x	x	0	x	x	x	Monitor 2 sensing set to Card Side
x	x	x	x	x	0	x	x	Monitor 2 Polarity set to OV above 1.25V
x	x	x	x	x	1	x	x	Monitor 2 Polarity set to UV below 1.25V
x	x	x	x	x	x	1	x	Monitor 1 sensing set to Bus Side
x	x	x	x	x	x	0	x	Monitor 1 sensing set to Card Side
x	x	x	x	x	x	x	0	Monitor 1 Polarity set to OV above 1.25V
x	x	x	x	x	x	x	1	Monitor 1 Polarity set to UV below 1.25V



CONFIGURATION REGISTER SETTINGS (CONTINUED)

SOFTWARE CONTROL AND STATUS REPORTING

The SMH4044 features advanced software control and status reporting over the serial interface. This is accomplished through writes and reads to a status register located at word address 02_{HEX}, device address 1001_{BIN}.

The status register can be read any time the SMH4044 is not in a nonvolatile write cycle. All of the bits in the register are read-only except for bit 5. When read this bit indicates the state of the VGATE5 and VGATE3 outputs. It can also be written to a “1” to turn on the VGATE5 and VGATE3 outputs if the PWR_EN pin is low. A write to the other bits in the status register is ignored.

The status register bit assignments are as follows:

Bit 7: Indicates the state of the HEALTHY# output. If HEALTHY# is low then this bit will be low. This bit is read-only.

Bit 6: Indicates the state of the SGNL_VLD# output. If SGNL_VLD# is low then this bit will be low. This bit is read-only.

Bit 5: Indicates whether VGATE5 and VGATE3 are on. If they are high then this bit will read high. If they are low and the PWR_EN pin is low then this bit can be written high to turn them on. The bit can also be written low to turn them off but only if the PWR_EN pin is low.

Bit 4: Indicates whether the SMH4044 is in reset. If the part is in reset then the bit will read high. This bit is read-only.

Bit 3: Indicates the state of MONITOR2. If it is out of range then the bit will read high. This bit is read-only.

Bit 2: Indicates the state of MONITOR1. If it is out of range then the bit will read high. This bit is read-only.

Bit 1: Indicates the state of CARD_5V_MON. If it is below the trip point then the bit will read low. This bit is read-only.

Bit 0: Indicates the state of CARD_3V_MON. If it is below the trip point then the bit will read low. This bit is read-only.

Table 5 - Configuration register R02 description.

Register R02								Action
D7	D6	D5	D4	D3	D2	D1	D0	
1	x	x	x	x	x	x	x	READ ONLY - State of HEALTHY# Output - High
0	x	x	x	x	x	x	x	READ ONLY - State of HEALTHY# Output - Low
x	1	x	x	x	x	x	x	READ ONLY - State of SIGNAL_VALID# Output - High
x	0	x	x	x	x	x	x	READ ONLY - State of SIGNAL_VALID# Output - Low
x	x	1	x	x	x	x	x	READ/WRITE Volatile - VGATE State - ON
x	x	0	x	x	x	x	x	READ/WRITE Volatile - VGATE State - OFF
x	x	x	1	x	x	x	x	READ ONLY - State of RESET - Active
x	x	x	0	x	x	x	x	READ ONLY - State of RESET - Not Active
x	x	x	x	1	x	x	x	READ ONLY - State of Monitor 2 sensing Fault
x	x	x	x	0	x	x	x	READ ONLY - State of Monitor 2 sensing No Fault - OK
x	x	x	x	x	1	x	x	READ ONLY - State of Monitor 1 sensing Fault
x	x	x	x	x	0	x	x	READ ONLY - State of Monitor 1 sensing No Fault - OK
x	x	x	x	x	x	1	x	READ ONLY - State of CARD_5V_MON - Above the programmed trip point
x	x	x	x	x	x	0	x	READ ONLY - State of CARD_5V_MON - Below the programmed trip point
x	x	x	x	x	x	x	1	READ ONLY - State of CARD_3V_MON - Above the programmed trip point
x	x	x	x	x	x	x	0	READ ONLY - State of CARD_3V_MON - Below the programmed trip point



I²C BUS INTERFACE

GENERAL DESCRIPTION

The I²C bus is a two-way, two-line serial communication between different integrated circuits. The two lines are: a serial Data line (SDA) and a serial Clock line (SCL). All Summit Microelectronics parts support a 100kHz clock rate, and some support the alternative 400kHz clock. Check Table 2 for the value of f_{SCL}. The SDA line must be connected to a positive supply by a pull-up resistor located on the bus. Summit parts have Schmitt Trigger inputs on both lines. See Figure 7 and Table 2 for waveforms and timing on the bus. One bit of Data is transferred during each Clock pulse. The Data must remain stable when the Clock is high.

Start and Stop Conditions

Both Data and Clock lines remain high when the bus is not busy. Data transfer between devices may be initiated with a Start condition only when SCL and SDA are high. A high-to-low transition of the Data line while the Clock line is high is defined as a Start condition. A low-to-high transition of the Data line while the Clock line is high is defined as a Stop condition. See Figure 14.

Protocol

The protocol defines any device that sends data onto the bus as a Transmitter, and any device that receives data as a Receiver. The device controlling data transmission is called the Master, and the controlled device is called the Slave. In all cases the Summit Microelectronic devices are Slave devices, since they never initiate any data transfers.

Acknowledge

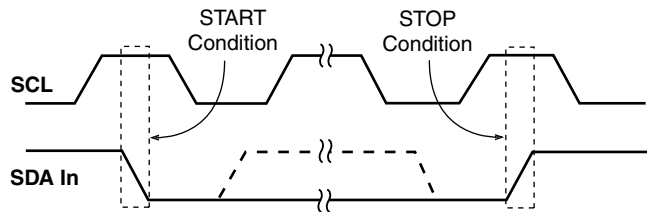
Data is always transferred in 8-Bit bytes. Acknowledge (ACK) is used to indicate a successful data transfer. The Transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the Receiver will pull the SDA line low to Acknowledge that it received the eight bits of data (See Figure 15). The termination of a Master Read sequence is indicated by a non-Acknowledge (NACK), where the Master will leave the Data line high.

In the case of a Read from a Summit part, when the last byte has been transferred to the Master, the Master will leave the Data line high for a NACK. This will cause the Summit part to stop sending data, and the Master will issue a Stop on the clock pulse following the NACK.

In the case of a Write to a Summit part the Master will send a Stop on the clock pulse after the last Acknowledge. This will indicate to the Summit part that it should begin its internal nonvolatile write cycle.

Basic Read and Write

The first byte from a Master is always made up of a seven bit Slave address and the Read/Write bit. The R/W bit tells the Slave whether the Master is reading data from the bus or writing data to the bus (1 = Read, 0 = Write). The first four of the seven address bits are called the Device Type Identifier (DTI). The DTI for the SMH4044 is 1010_{BIN}. The next two bits are used to select one-of-four possible



2057 Fig08

Figure 14. I²C Start and Stop Timing

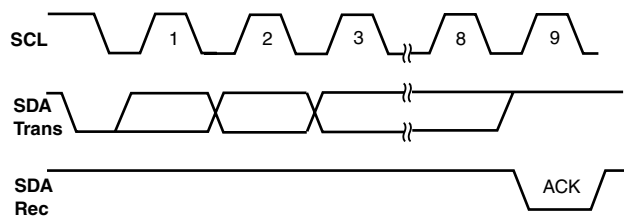
devices on the bus. The next bit is the block select bit. The SMH4044 will issue an Acknowledge after recognizing a Start condition and its DTI.

In the Read mode the SMH4044 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected, and no Stop condition is generated by the Master, the SMH4044 will continue to transmit data. If an Acknowledge is not detected (NACK), the SMH4044 will terminate further data transmission. See Figure 17.

In the Write mode the SMH4044 receives eight bits of data, then generates an Acknowledge signal. It will continue to generate ACKs until a Stop condition is generated by the Master. See Figure 18.

Random Address Read

Random address Read operations allow the Master to access any memory location in a random fashion. This operation involves a two-step process. First, the Master issues a Write command which includes the Start condition



2057 Fig09

Figure 15. Acknowledge Timing



I²C BUS INTERFACE (CONTINUED)

and the Slave address field (with the R/W bit set to Write) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMH4044 to the desired address. After the word address Acknowledge is received by the Master, it immediately reissues a Start condition followed by another Slave address field with the R/W bit set to Read. The SMH4044 will respond with an Acknowledge and then transmit the 8 data bits stored at the addressed location. At this point the Master sets SDA high (NACK) and generates a Stop condition. The SMH4044 discontinues data transmission and reverts to its standby power mode.

address byte Read or random address byte Read). However, the Master now responds with an Acknowledge, indicating that it requires additional data from the SMH4044. The SMH4044 continues to output data for each Acknowledge received. The Master terminates the sequential Read operation with a NACK and issues a Stop condition.

During a sequential Read operation the internal address counter is automatically incremented with each Acknowledge signal. For Read operations all address bits are incremented, allowing the entire array to be read using a single Read command. After a count of the last memory address the address counter will rollover and the memory will continue to output data.

Sequential Read

Sequential Reads can be initiated as either a current address Read or a random access Read. The first word is transmitted as with the other byte Read modes (current

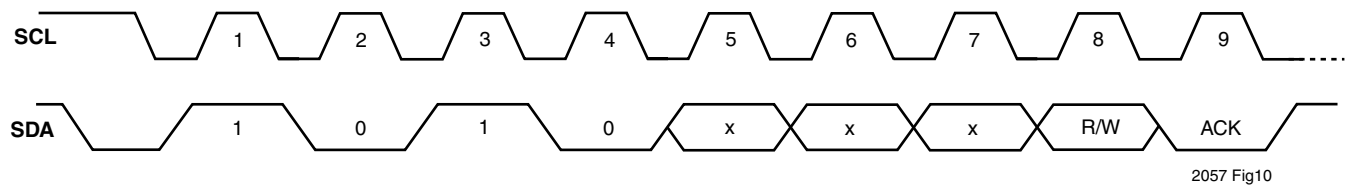


Figure 16. Typical Master Address Byte Transmission

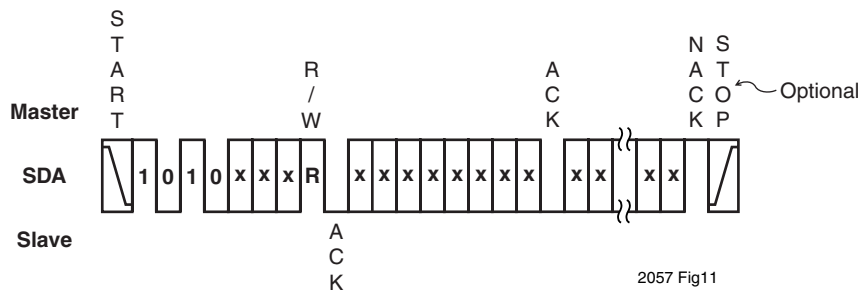


Figure 17. Basic Read

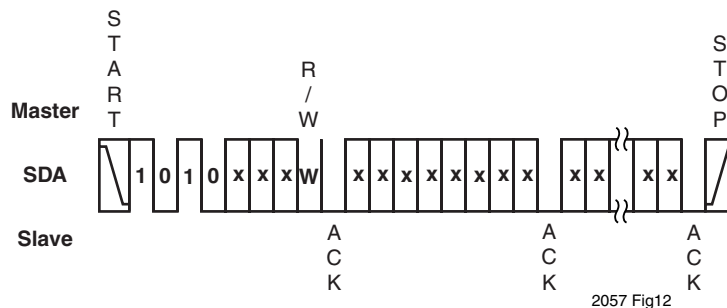


Figure 18. Basic Write



DEVELOPMENT HARDWARE & SOFTWARE

Programming the SMH4044

The end user can obtain the Summit SMX3200 programming system for device prototype development. The SMX3200 system consists of a programming Dongle, cable and Windows GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 is available from the website (www.summitmicro.com).

An example of the connection interface is shown in Figure 19. When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus. The Windows GUI software will generate the data and send it in I2C serial bus format so that it can be directly downloaded to the SMH4044 via the programming Dongle and cable.

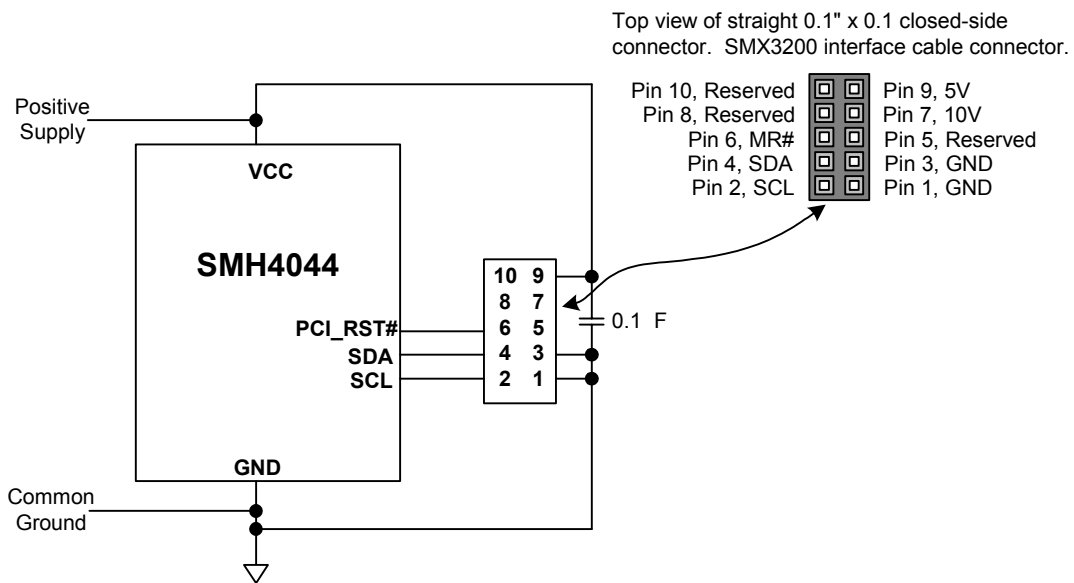


Figure 19. SMX3200 Programmer connections for the SMH4044.

**DEFAULT CONFIGURATION REGISTER SETTINGS – SMH4044F-183**

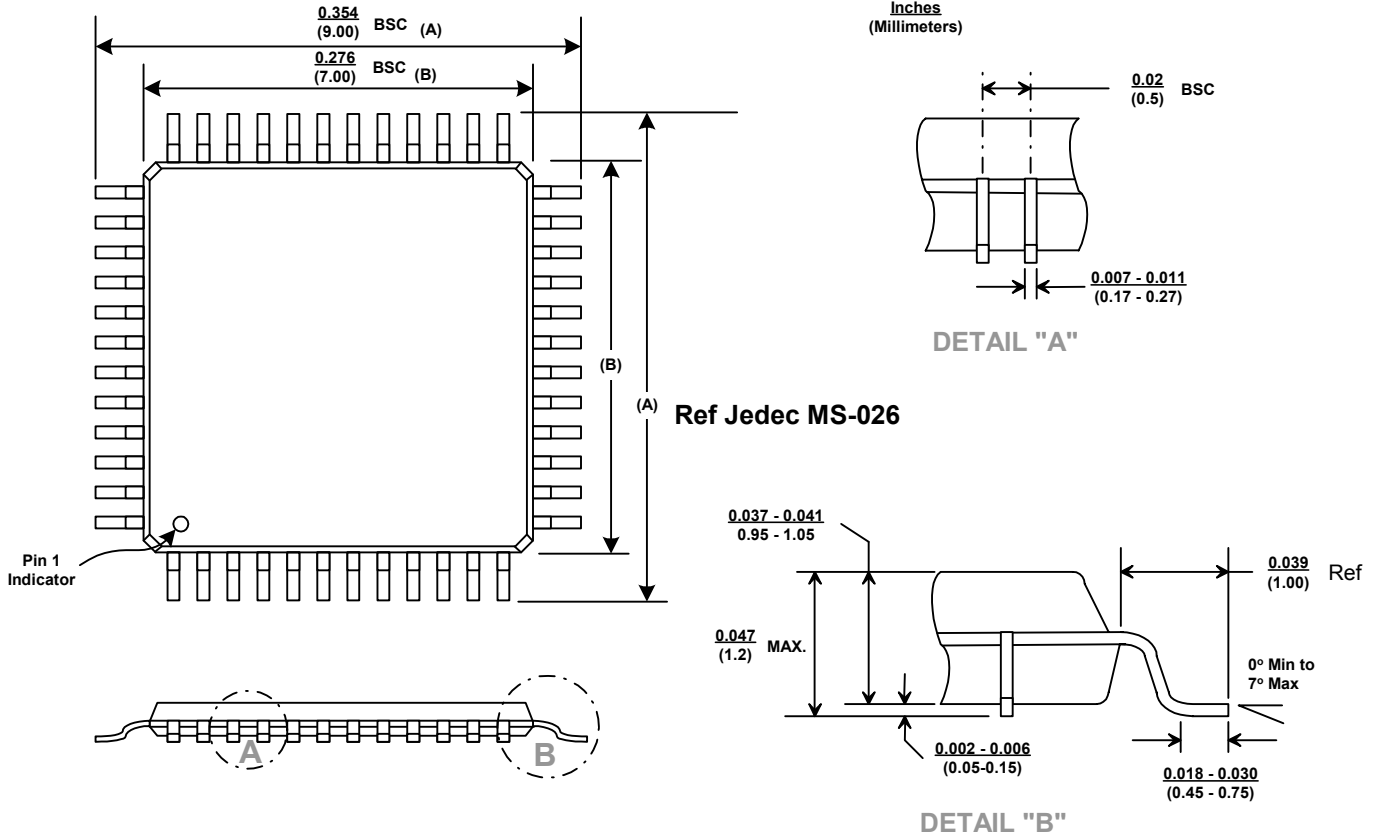
Register	Contents	Function
R00	A3	V3 Trip = 2.95V, VO5/VO3 threshold = 50mV below VC5/VC3, Watchdog Timeout = OFF, Reset and BD_SEL# = 200ms, Local PCI RST/RST# pins = I/O
R01	5F	Config Lockout = Unlocked, V5 Trip = 4.625V, CBI Threshold = 50mV, Monitor 1 and Monitor 2 = Bus Side Sensing and UV Polarity
R02	00	Healthy = Low, Signal Valid# Output = Low, Reset = Not Active, VGATE State = Off, Monitor 1 and Monitor 2 = OK (Low), CARD_5V_MON = Below Trip Point, CARD_3V_MON = Below Trip Point

The default device ordering number is SMH4044F-183, is programmed as described above and tested over the commercial temperature range. The three configuration registers are described on pages 18 and 19.



PACKAGE

48 PIN TQFP PACKAGE



ORDERING INFORMATION

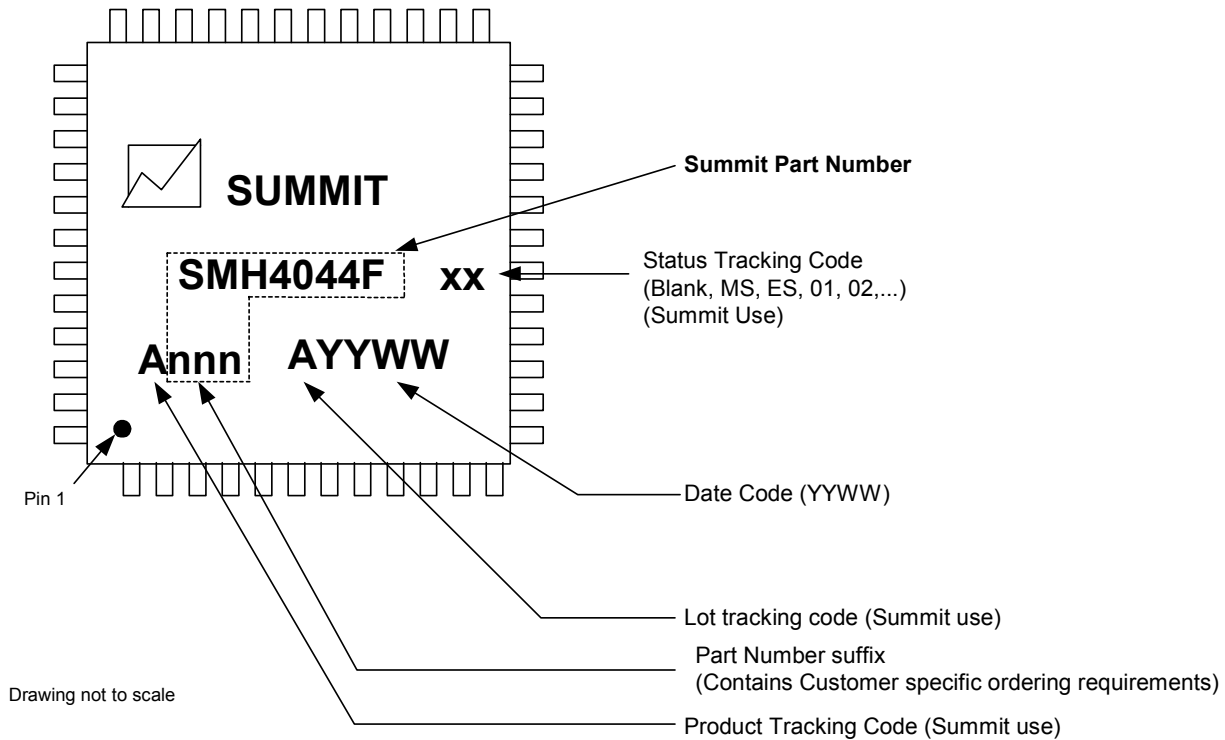
Summit Part Number **SMH4044** **F** **nnn**

Package
F=48 Lead TQFP

Part Number Suffix (see page 23)
Specific requirements are contained in the suffix such as Commercial or Industrial Temp Range, Hex code, Hex code revision, etc.



PART MARKING



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