

Nonvolatile DACPOT™ Electronic Potentiometer With Up/Down Counter Interface

FEATURES

- Digitally Controlled Electronic Potentiometer
- 8-Bit Digital-to-Analog Converter (DAC)
 - Independent Reference Inputs
 - Differential Non-Linearity - $\pm 0.5\text{LSB}$ max
 - Integral Non-Linearity - $\pm 1\text{LSB}$ max
- V_{OUT} Value in E²PROM for Power-On Recall
 - Equivalent to 256-Step Potentiometer
- Unity Gain Op Amp Drives up to 1mA
- Simple Trimming Adjustment
 - Up/Down Counter Style Operation
- Low Noise Operation
- “Clickless” Transitions between DAC Steps
- No Mechanical Wearout Problem
 - 1,000,000 Stores (typical)
 - 100 Year Data Retention
- Operation from +2.7V to +5.5V Supply
- Low Power, 1mW max at +5V

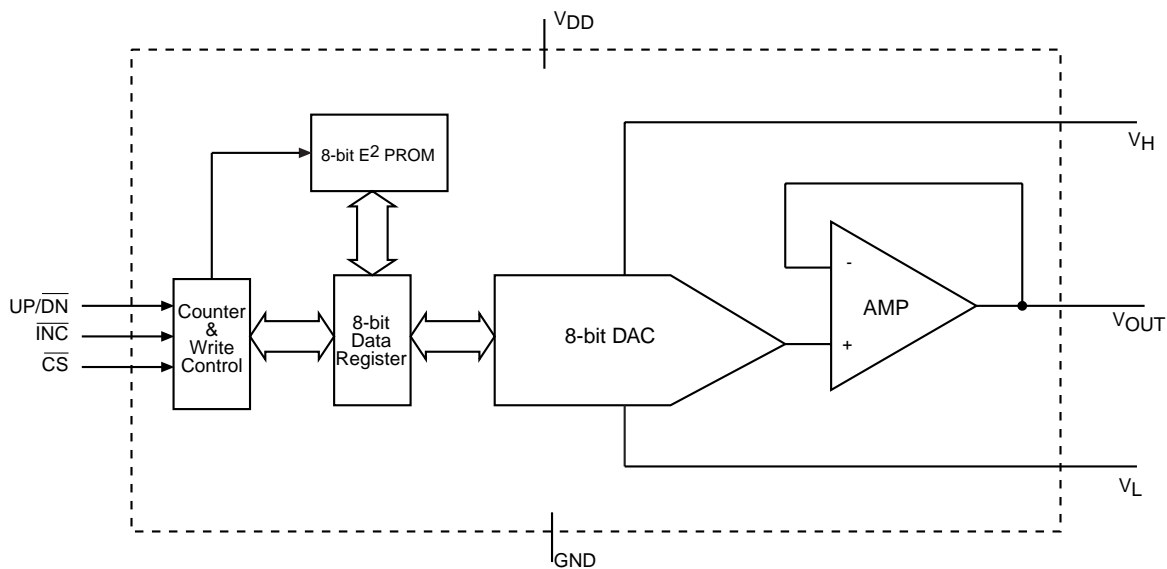
OVERVIEW

The S9318 DACPOT™ trimmer is an 8-bit nonvolatile DAC designed to replace mechanical potentiometers. The S9318 includes a unity-gain amplifier to buffer the DAC output and enables V_{OUT} to swing from rail to rail. The DACPOT trimmer operates over a supply voltage range of 2.7V to 5.5V.

The S9318's simple up/down counter input provides an ideal interface for automatic test equipment to dither and monitor the V_{OUT} voltage. This interface allows for quick and consistent calibration of even the most sophisticated systems.

The S9318 is a pin-compatible performance upgrade for other industry nonvolatile potentiometers. The S9318 offers double the resolution of these devices and provides 'clickless' transitions of V_{OUT} .

FUNCTIONAL BLOCK DIAGRAM



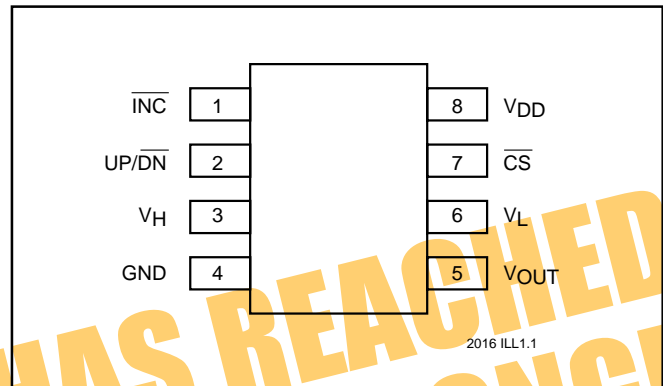
2016 ILL2.1



PIN NAMES

| Symbol | Description |
|---------------------|---|
| \overline{INC} | Increment Input, High to Low Edge Trigger |
| UP/ \overline{DN} | Up/Down Input controlling relative V_{OUT} movement |
| V_H | V+ reference input |
| GND | Analog and Digital Ground |
| V_{OUT} | Trimmed Voltage Output |
| V_L | V- reference input |
| \overline{CS} | Active low chip select input |
| V_{DD} | Supply Voltage (2.7V to 5.5V) |

PINOUT



Analog Section

The S9318 is an 8-bit, voltage output digital-to-analog converter (DAC). The DAC consists of a resistor network that converts an 8-bit value into equivalent analog output voltages in proportion to the applied reference voltage.

Reference Inputs

The voltage differential between the V_L and V_H inputs sets the full-scale output voltage range. V_L must be equal to or greater than ground (i.e. a positive voltage). V_H must be greater than V_L and less than or equal to V_{DD} . See table on page 3 for guaranteed operating limits.

Output Buffer Amplifier

The voltage output is a precision unity-gain follower that can slew up to $1V/\mu s$.

Digital Interface

The interface is designed to emulate a simple up/down counter, but instead of a parallel count output, a ratiometric voltage output is provided.

Chip Select (\overline{CS}) is an active low input. Whenever \overline{CS} is high the S9318 is in standby mode and consumes the least power. This mode is equivalent to a potentiometer that is adjusted to the required setting. When \overline{CS} is low the S9318 will recognize transitions on the \overline{INC} input and will move the V_{OUT} either toward the V_H reference or toward the V_L reference depending upon the state of the UP/ \overline{DN} input.

The host may exit an adjustment routine in two ways: deselecting the S9318 while \overline{INC} is low will not perform a store operation (a subsequent power cycle will recall the original data); deselecting the S9318 while \overline{INC} is high will store the current V_{OUT} setting into nonvolatile memory.

Increment (\overline{INC}) is an edge triggered input. Whenever \overline{CS} is low and a high to low transition occurs on the \overline{INC} input, the V_{OUT} voltage will either move toward V_H or V_L depending upon the state of the UP/ \overline{DN} input.

UP/Down (UP/ \overline{DN}) is an input that will determine the V_{OUT} movement relative to V_H and V_L . When \overline{CS} is low, UP/ \overline{DN} is high and there is a high to low transition on \overline{INC} , the V_{OUT} voltage will move $(1/256^{th} \times V_H - V_L)$ toward V_H . When \overline{CS} and UP/ \overline{DN} are low, and there is a high to low transition on \overline{INC} , the V_{OUT} will move $(1/256^{th} \times V_H - V_L)$ toward V_L .



ABSOLUTE MAXIMUM RATINGS*

| | |
|--|--------------------------------|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on pins with reference to GND: | |
| Analog Inputs | -0.5V to V _{DD} +0.5V |
| Digital Inputs | -0.5V to V _{DD} +0.5V |
| Analog Outputs | -0.5V to V _{DD} +0.5V |
| Digital Outputs | -0.5V to V _{DD} +0.5V |
| Lead Solder Temperature (10 secs) | 300°C |

***COMMENT**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operation sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

| Condition | Min | Max |
|-----------------|-------|-------|
| Temperature | -40°C | +85°C |
| V _{DD} | +2.7V | +5.5V |

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DAC DC ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, V_{refH} = V_{DD}, V_{refL} = 0V, T_A = -40°C to +85°C, unless specified otherwise

| | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------------------|--------------------|---|---|-------------------|----------|-------------------|--------|
| Accuracy | INL | Integral Non-Linearity | I _{LOAD} = 100µA, | - | 0.5 | ±1 | LSB |
| | DNL | Differential Non-Linearity | I _{LOAD} = 100µA, Guaranteed but not tested | - | 0.1 | ±0.5 | LSB |
| References | V _H | V _{refH} Input Voltage | | V _{refL} | - | V _{DD} | V |
| | V _L | V _{refL} Input Voltage | | Gnd | - | V _{refH} | V |
| | R _{IN} | V _{refH} to V _{refL} Resistance | | - | 38K | - | Ω |
| | TCR _{IN} | Temperature Coefficient of R _{IN} | V _{refH} to V _{refL} | - | 600 | - | ppm/°C |
| Analog Output | GEFS | Full-Scale Gain Error | DATA = FF | - | - | ±1 | LSB |
| | V _{OUTZS} | Zero-Scale Output Voltage | DATA = 00 | 0 | | 20 | mV |
| | TCV _{OUT} | V _{OUT} Temperature Coefficient | V _{DD} = +5, I _{LOAD} = 50µA, V _{refH} = +5V, V _{refL} = 0V Guaranteed but not tested | - | - | 50 | µV/°C |
| | I _L | Amplifier Output Load Current | | -200 | | +1000 | µA |
| | R _{OUT} | Amplifier Output Resistance | I _L = 100µA V _{DD} = +5V V _{DD} = +3V | - | 10 20 | | Ω Ω |
| | PSRR | Power Supply Rejection | I _{LOAD} = 10µA | - | - | 1 | LSB/V |
| | e _N | Amplifier Output Noise | f = 1KHz, V _{DD} = +5V | - | 90 | - | nV/√Hz |
| | THD | Total Harmonic Distortion | V _{IN} = 1V rms, f = 1KHz | - | 0.08 | - | % |
| BW | Bandwidth - 3dB | V _{IN} = 100mV rms | - | 300 | - | kHz | |

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**RELIABILITY CHARACTERISTICS**

| Symbol | Parameter | Min | Max | Unit | Test Method |
|------------------|--------------------|-----------|-----|--------|-------------------|
| V _{ZAP} | ESD Susceptibility | 2000 | | V | MS-883, TM 3015 |
| I _{LTH} | Latch-Up | 100 | | mA | JEDEC Standard 17 |
| T _{DR} | Data Retention | 100 | | Years | MS-883, TM 1008 |
| N _{END} | Endurance | 1,000,000 | | Stores | MS-883, TM 1033 |

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DC ELECTRICAL CHARACTERISTICS V_{DD} = +2.7V to +5.5V, V_H = V_{DD}, V_L = 0V, Unless otherwise specified

| Symbol | Parameter | Conditions | Min | Max | Units |
|-----------------|-------------------------------------|-----------------------------------|-----|-----------------|-------|
| I _{DD} | Supply Current during store, note 1 | CS = V _{IL} | | 1.2 | mA |
| I _{SB} | Supply Standby Current | CS = V _{IH} | | 200 | μA |
| I _{IH} | Input Leakage Current | V _{IN} = V _{DD} | | 10 | μA |
| I _{IL} | Input Leakage Current, note 2 | V _{IN} = 0V | | -25 | μA |
| V _{IH} | High Level Input Voltage | | 2 | V _{DD} | V |
| V _{IL} | Low Level Input Voltage | | 0 | 0.8 | V |

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Notes:

- I_{DD} is the supply current drawn while the EEPROM is being updated. I_{DD} does not include the current that flows through the Reference resistor chain.
- CS, UP/DN and INC have internal pull-up resistors of approximately 200kΩ. When the input is pulled to ground the resulting output current will be V_{DD}/200kΩ.



OPERATIONAL TRUTH TABLE

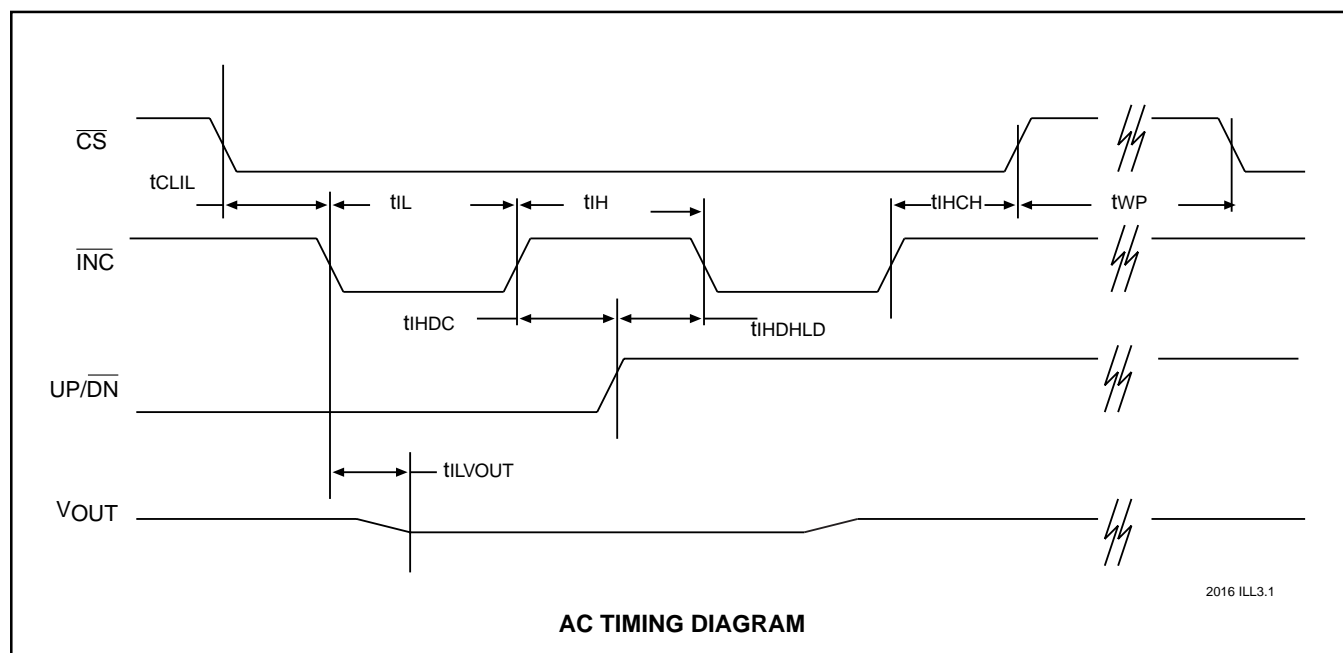
| \overline{INC} | \overline{CS} | UP/DN | Operation |
|---------------------|---------------------|-----------------|--|
| HI _{TO} LO | L | H | V _{OUT} toward V _H |
| HI _{TO} LO | L | L | V _{OUT} toward V _L |
| H | LO _{TO} HI | X | Store Setting |
| L | LO _{TO} HI | X | Maintain Setting, NO Store |
| V _{DD} | V _{DD} | V _{DD} | Standby |

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AC TIMING CHARACTERISTICS V_{DD} = +4.5V to +5.5V

| Symbol | Parameter | Min | Max | Units |
|---------------------|---|-----|-----|-------|
| t _{CLIL} | \overline{CS} to \overline{INC} Setup | 100 | | ns |
| t _{IHDC} | \overline{INC} High to UP/DN Change | 100 | | ns |
| t _{DCIL} | UP/DN to \overline{INC} Setup | 100 | | ns |
| t _{IL} | \overline{INC} Low Period | 200 | | ns |
| t _{IH} | \overline{INC} High Period | 200 | | ns |
| t _{IHCH} | \overline{INC} Inactive to \overline{CS} Inactive | 100 | | ns |
| t _{WP} | Write Cycle Time | | 5 | ms |
| t _{ILVOUT} | \overline{INC} to V _{OUT} Delay | | 5 | μs |

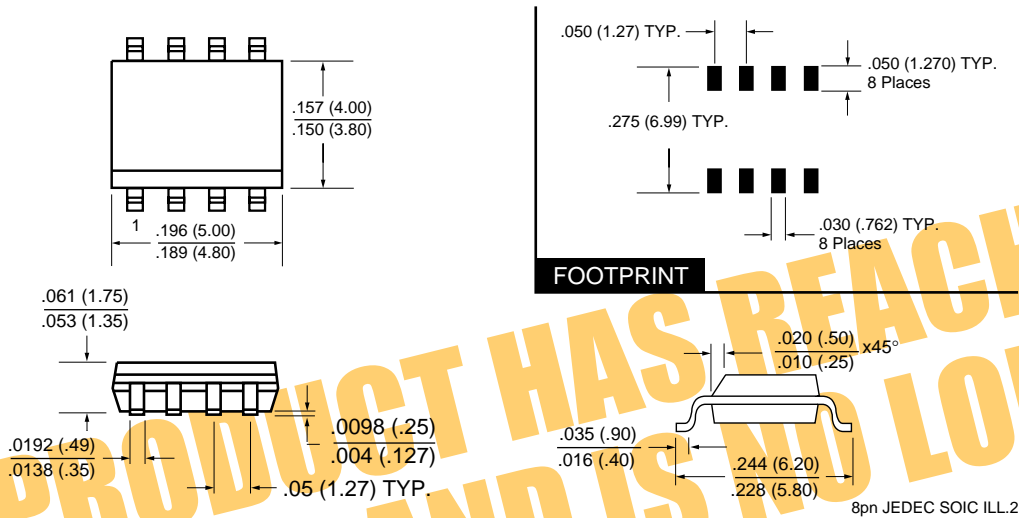
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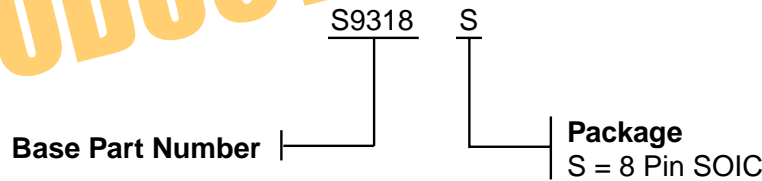


8 Pin SOIC (Type S) Package JEDEC (150 mil body width)



THIS PRODUCT HAS REACHED END OF LIFE AND IS NO LONGER IN PRODUCTION

ORDERING INFORMATION



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